DATA SHEET

TEA1211HN
High efficiency auto-up/down DC/DC converter

Preliminary specification
Supersedes data of 2003 Aug 06

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Philips
Semiconductors

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CONTENTS

High efficiency auto-up/down DC/DC converter

TEA1211HN

1 FEATURES

- I²C-bus programmable output voltage range of 1.5 V to 5.5 V
- Single inductor topology
- High efficiency up to 94 % over wide load range
- Wide input range; functional from 2.55 V up to 5.5 V
- 1.7 A maximum input and output current
- Low quiescent power consumption
- 600 kHz switching frequency
- Four integrated very low $R_{DS(on)}$ power MOSFETs
- Synchronizable to external clock
- Externally adjustable current limit for protection and efficient battery use in case of dynamic loads
- Under voltage lockout
- PWM-only option
- Shut-down current less than 1 μA
- 32-pin small body HVQFN package.

2 APPLICATIONS

- Stable output voltage from Lithium-Ion batteries
- Variable voltage source for PAs (Power Amplifiers) in cellular phones
- Wireless handsets
- Hand-held instruments
- Portable computers.

3 GENERAL DESCRIPTION

The TEA1211HN is a fully integrated auto-up/down DC/DC converter circuit with I²C-bus interface. Efficient, compact and dynamic power conversion is achieved using a digitally controlled pulse width and frequency modulation like control concept, four integrated low $R_{DS(on)}$ power switches with low parasitic capacitances and fully synchronous rectification.

The combination of auto-up/down DC/DC conversion, high efficiency and low switching noise makes the TEA1211HN well suited to supply a power amplifier in a cellular phone.

The output voltage can be I²C-bus programmed to the exact voltage needed to achieve a certain output power level with optimal system efficiency, thus enlarging battery lifetime.

The TEA1211HN operates at 600 kHz switching frequency which enables the use of small size external components. The switching frequency can be locked to an external high frequency clock. Deadlock is prevented by an on-chip under voltage lockout circuit. An adjustable current limit enables efficient battery use even at high dynamic loads. Optionally, the device can be kept in pulse width modulation mode regardless of the load applied.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1211HN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

5 BLOCK DIAGRAM

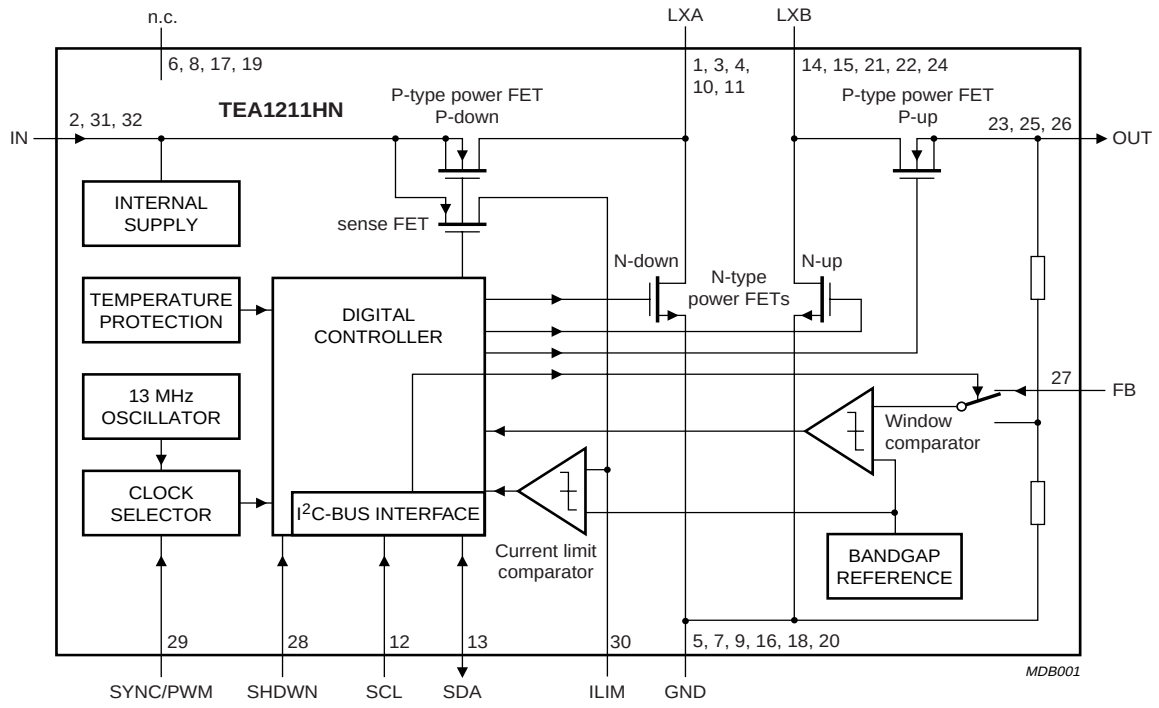
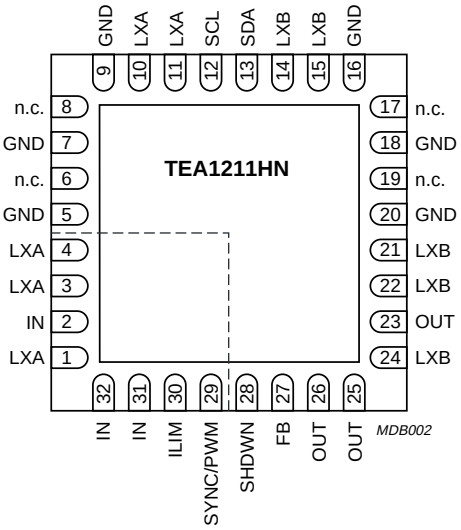


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
LXA	1	inductor connection 1
IN	2	input voltage
LXA	3	inductor connection 1
LXA	4	inductor connection 1
GND	5	ground
n.c.	6	not connected
GND	7	ground
n.c.	8	not connected
GND	9	ground
LXA	10	inductor connection 1
LXA	11	inductor connection 1
SCL	12	serial clock input line I^2C-bus
SDA	13	serial data input/output line I^2C-bus
LXB	14	inductor connection 2
LXB	15	inductor connection 2
GND	16	ground
n.c.	17	not connected
GND	18	ground
n.c.	19	not connected
GND	20	ground
LXB	21	inductor connection 2
LXB	22	inductor connection 2
OUT	23	output voltage
LXB	24	inductor connection 2
OUT	25	output voltage
OUT	26	output voltage
FB	27	feedback input
SHDWN	28	shut-down input
SYNC/PWM	29	synchronization clock input, PWM-only input
ILIM	30	current limit resistor connection
IN	31	input voltage
IN	32	input voltage



This diagram is a bottom side view.
Pin 1 is indicated with a dot on the top side of the package.
For mechanical details of HVQFN32 package, see Chapter 12.

Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Introduction

The TEA1211HN is able to operate in Pulse Frequency Modulation (PFM) or discontinuous conduction mode as well as in Pulse Width Modulation (PWM) or continuous conduction mode. All switching actions are completely determined by a digital control circuit which uses the output voltage level as control input. This digital approach enables the use of a new pulse width and frequency modulation scheme, which ensures optimum power efficiency over the complete range of operation of the converter.

7.2 Control mechanism

Depending on load current I_{load} and V_{IN} to V_{OUT} ratio, the controller chooses a mode of operation. When high output power is requested, the device will operate in PWM (continuous conduction) mode, which is a 2-phase cycle in up- as well as in down mode. For small load currents the controller will switch over to PFM (discontinuous mode), which is either a 3- or 4-phase cycle depending on the input to output ratio, see Fig.3.

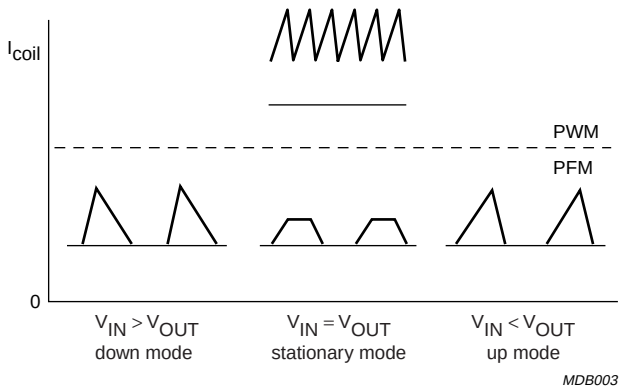


Fig.3 Waveform of coil current as function of I_{load} and V_{IN} to V_{OUT} ratio.

7.2.1 PWM

PWM results in minimum AC currents in the circuit components and hence optimum efficiency, cost and EMC. In this mode the output voltage is allowed to vary between two predefined voltage levels. When the output voltage stays within this so called window, switching continues in a fixed pattern. When the output voltage reaches one of the window borders, the digital controller immediately reacts by adjusting the duty cycle and inserting a current step in such a way that the output voltage stays within the window with higher or lower current capability. This approach enables very fast reaction to load variations.

Figure 4 shows the TEA1211HN's response to a sudden load increase in case of up conversion. The upper trace shows the output voltage. The ripple on top of the DC level is a result of the current in the output capacitor, which changes in sign twice per cycle, multiplied by the capacitor's internal Equivalent Series Resistance (ESR). After each ramp-down of the inductor current, or when the ESR effect increases the output voltage, the TEA1211HN determines what to do in the next cycle. As soon as more load current is taken from the output the output voltage starts to decay. When the output voltage becomes lower than the low limit of the window, corrective action is taken by a ramp-up of the inductor current during a much longer time. As a result, the DC current level is increased and normal PWM control can continue. The output voltage (including ESR effect) is again within the predefined window.

Figure 5 depicts the spread of the output voltage window. The absolute value is most dependent on spread, while the actual window size is not affected. For one specific device, the output voltage will not vary more than 2 % typically.

7.2.2 PFM

In low output power situations, TEA1211HN will switch over to PFM mode operation in case PWM-only mode is not activated. In this mode charge is transferred from battery to output in single pulses with a wait phase in between. Regulation information from earlier PWM mode operation is used. This results in optimum inductor peak current levels in PFM mode, which are slightly larger than the inductor ripple current in PWM mode. As a result, the transition between PFM and PWM mode is optimal under all circumstances. In PFM mode, the TEA1211HN regulates the output voltage to the limits shown in Fig.5. Depending on the V_{IN} to V_{OUT} ratio the TEA1211HN decides for a 3- or 4-phase cycle, where the last phase is the wait phase. When the input voltage almost equals the output voltage, one of the slopes of a 3-phase cycle becomes weak. Then the charge, or the integral of its pulse, is near to zero and no charge is transferred. In this region the 4-phase cycle is used, (see Fig.3).

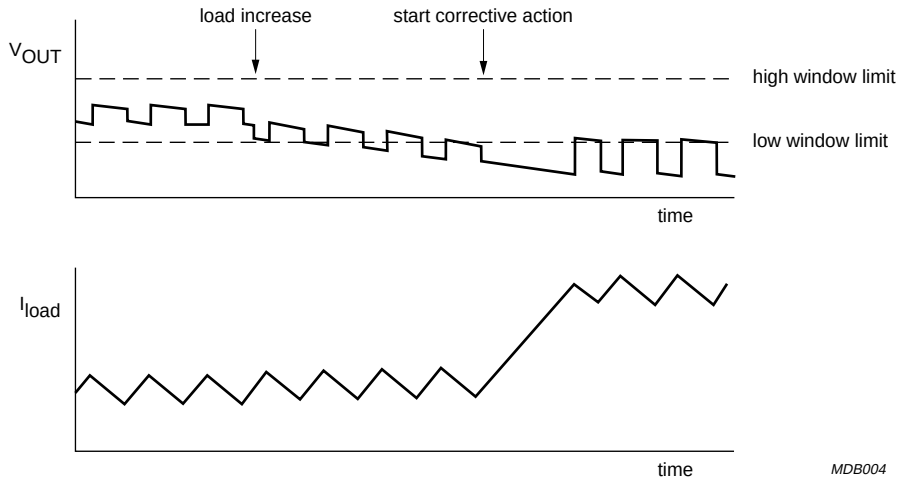
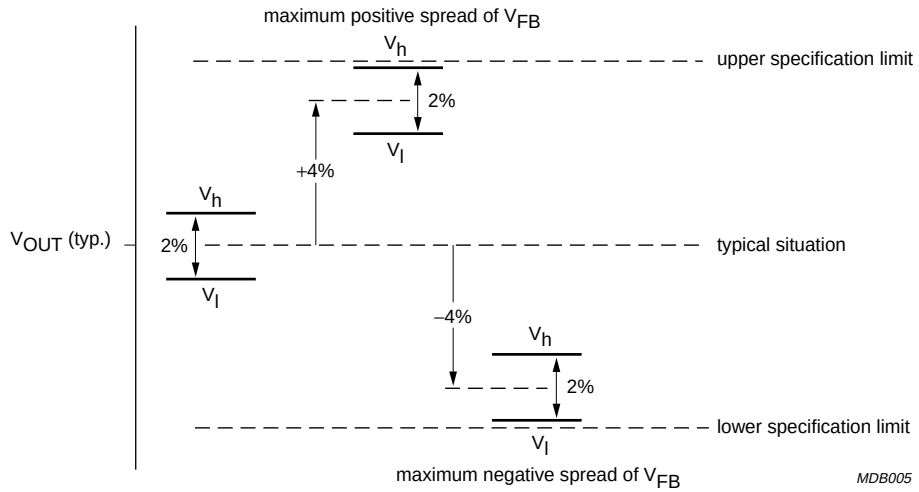


Fig.4 Response to load increase in up-mode.



V_h = High window limit
V_l = Low window limit

Fig.5 Spread of location of output voltage window.

7.2.3 SWITCHING SEQUENCE

Refer to Figures 1 and 3. In up-mode the cycle starts by making P-down and N-up conducting in the first phase. The second phase N-up opens and P-up starts conducting. In down-mode the cycle starts with in the first phase P-up and P-down conducting. The second phase P-down opens and N-down starts conducting. In PFM these two phases are followed by a third or wait phase that opens all switches except for N-down, which is closed to prevent the coil from floating.

The stationary mode or 4-phase cycle, which only occurs in PFM, starts with in the first phase P-down and N-up conducting. In the second phase P-down and P-up conduct forming a short-cut from battery to output capacitor. In the third phase P-up and N-down conduct. The fourth or wait-phase again opens all switches except for N-down which is closed to prevent the coil from floating.

7.3 Adjustable output voltage

The output voltage of the TEA1211HN can be set to a fixed value by means of an external resistive divider. After start-up through this divider, dynamic control of the output voltage is made possible by use of an I^2C-bus. The output voltage can be programmed from 1.5 V to 5.5 V in 40 steps of 0.1 V each. In case of Power Amplifiers (PAs) for example the output voltage of the TEA1211HN can be adjusted to the output power to be transmitted by the PA, in order to obtain maximum system efficiency.

7.4 Start-up

If the input voltage exceeds the start voltage, the TEA1211HN starts ramping up the voltage at the output capacitor. Ramping stops when the target level, set by the external resistors, is reached.

7.5 Under voltage lockout

As a result of too high load or disconnection of the input power source, the input voltage can drop too low to guarantee normal regulation. In that case, the device switches to a shut-down mode stopping the switching completely. Start-up is possible by crossing the start-up level again.

7.6 Shut-down

When pin SHDWN is made HIGH, the converter disables all switches except for N-down (see Fig.1) and power consumption is reduced to a few μA. N-down is kept conducting to prevent the coil from floating.

7.7 Power switches

The power switches in the IC are two N-type and two P-type MOSFETs, having a typical pin-to-pin resistance of 85 mΩ. The maximum continuous input/output current in the switches is 1.7 A at 70 °C ambient temperature.

7.8 Synchronous rectification

For optimal efficiency over the whole load range, synchronous rectifiers inside the TEA1211HN ensure that in PFM mode during the phase where the coil current is decreasing, all inductor current will flow through the low ohmic power MOSFETs. Special circuitry is included which detects that the inductor current reaches zero. Following this detection, the digital controller switches off the power MOSFET and proceeds regulation. Negative currents are thus prevented.

7.9 PWM-only mode

When pin SYNC/PWM is HIGH, the TEA1211HN will use PWM regulation independent of the load applied. As a result, the switching frequency does not vary over the whole load range.

7.10 External synchronisation

If a high frequency clock is applied to pin SYNC/PWM, the switching frequency in PWM mode will be exactly that frequency divided by 22. PFM mode is not possible if an external clock is applied. The quiescent current of the device increases when an external clock is applied.
In case no external synchronisation is necessary and the PWM-only option is not used, pin SYNC/PWM must be connected to ground.

7.11 Current limiter

If the peak input current of the TEA1211HN exceeds its limit in PWM mode, current ramping is stopped immediately, and the next switching phase is entered. The current limitation protects the IC against overload conditions, inductor saturation, etc. The current limit level is user defined by the external resistor which must be connected between pin ILIM and pin GND.

7.12 I²C-bus serial interface

The serial interface of the TEA1211HN is the I²C-bus. A detailed description of the I²C-bus specification, including applications, is given in the brochure: *"The I²C-bus and how to use it"*, order no. 9398 393 40011.

7.12.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor (for best efficiency it is advised to use the input voltage of the convertor). Data transfer may be initiated only when the bus is not busy. In bus configurations with ICs on different supply voltages, the pull-up resistors shall be connected to the highest supply voltage. The I²C-bus supports incremental addressing. This enables the system controller to read or write multiple registers in only one I²C-bus action. The TEA1211HN supports the I²C-bus up to 400 kbit/s.

The I²C-bus system configuration is shown in Fig.6.
A device generating a message is a transmitter, a device receiving a message is a receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The TEA1211HN is a slave only device.

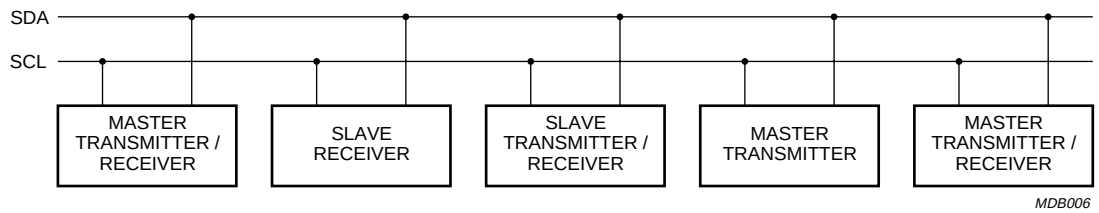


Fig.6 I²C-bus system configuration.

7.12.2 START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Fig.7).

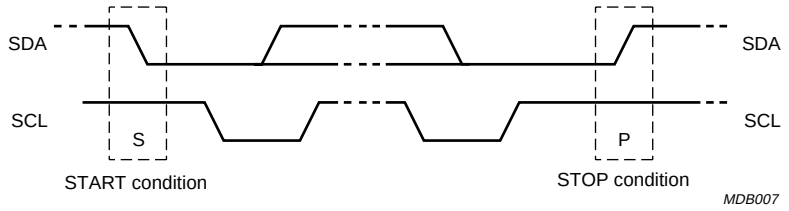


Fig.7 START and STOP conditions on the I^2C-bus.

7.12.3 BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Fig.8).

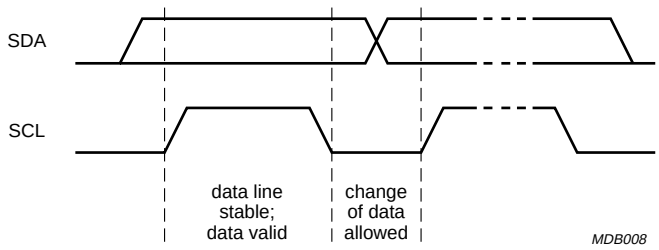


Fig.8 Bit transfer on the I^2C-bus.

7.12.4 ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the receiver generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter (see Fig.9).

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

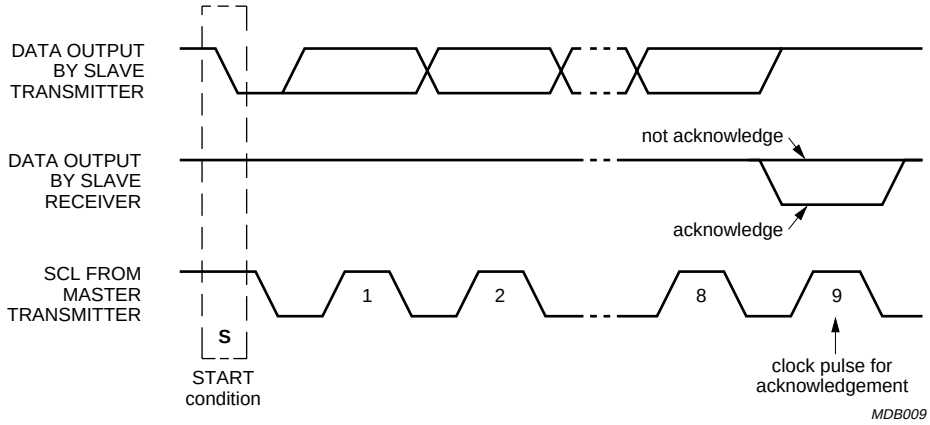


Fig.9 Acknowledge on the I²C-bus.

7.12.5 I²C-BUS PROTOCOL

7.12.5.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The (slave) address of the TEA1211HN is 0001 0000 (10h). The subaddress (or word address) is 0000 0000 (00h).

The TEA1211HN acts as a slave receiver only. Therefore the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line, enabling the TEA1211HN to send an acknowledge.

7.12.5.2 Data

The data consists of one byte, addressing the 40 voltage steps as explained in Tables 1 and 2.

Table 1 Data byte

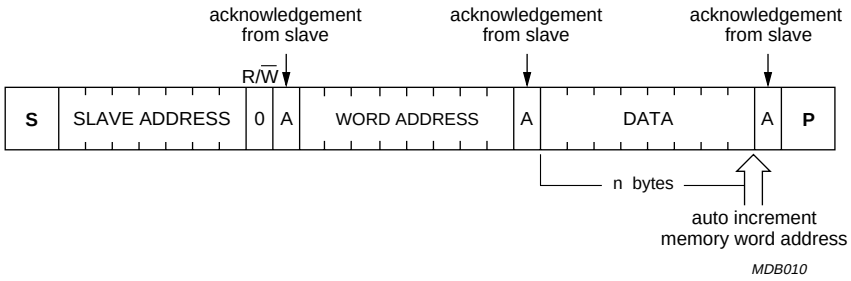
SUBADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 2	BIT 0
00h	0	0	CVLVL5	CVLVL4	CVLVL3	CVLVL2	CVLVL1	CVLVL0

Table 2 Translation data byte to voltage level

SUBADDRESS	NAME	SIZE (BIT)	STEP NUMBER		MIN. (V)	STEP (V)	MAX. (V)
			MIN.	MAX.			
00h	CVLVL	6	0	40	1.5	0.1	5.5

7.12.5.3 Write Cycle

The I²C-bus configuration for the different TEA1211HN write cycles is shown in Fig.10. The word address is an eight bit value that defines which register is to be accessed next.



S = START condition.
P = STOP condition.

Fig.10 Master transmits to slave receiver (write mode).

8 LIMITING VALUES

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_n	voltage on any pin with respect to GND	shut-down mode	–0.5	+6.0	V
		operational mode	–0.5	+5.5	V
P_{tot}	total internal power dissipation		–	1000	mW
T_j	junction temperature		–40	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–40	+125	°C
V_{esd}	electrostatic discharge voltage				
	pins LXA	note 1	–	±800	V
		note 2	–	±200	V
	all other pins	JEDEC Class II; note 1	–	±2000	V
		JEDEC Class II; note 2	–	±200	V

Notes

1. Human Body Model: equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor.
2. Machine Model: equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor.

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on dedicated PCB in free air	35	K/W

10 CHARACTERISTICS

T_{amb} = –40 to +85 °C; all voltages with respect to ground; positive currents flow into the IC; unless otherwise specified.

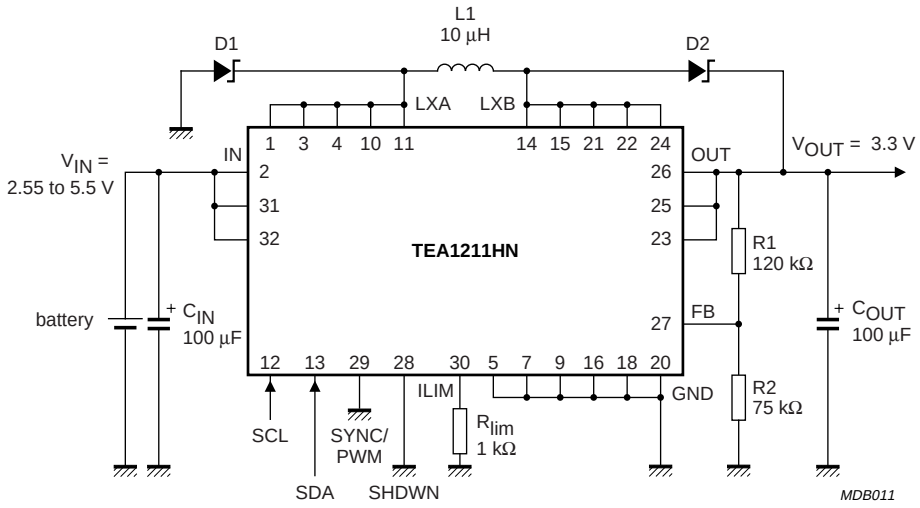
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage levels						
V_{OUT}	output voltage		1.50	–	5.50	V
$V_{IN(start)}$	start voltage	V_{OUT} = 3.5 V; I_{load} < 100 mA	2.45	2.55	2.65	V
V_{IN}	input voltage		$V_{IN(start)}$	–	5.50	V
$V_{IN(uvlo)}$	under voltage lockout level		–	$V_{IN(start)}$ – 0.15	–	V
V_{FB}	feedback voltage level		1.20	1.25	1.30	V
$V_{OUT(wdw)}$	output voltage window as percentage of V_{OUT}	PWM mode	1.5	2.0	3.0	%
Current levels						
I_q	quiescent current	no load	–	100	–	µA
I_{shdwn}	current in shut-down mode		–	< 1	2	µA
ΔI_{lim}	current limit deviation	I_{lim} = 1 A; note 1	–30	–	+30	%
I_{max}	maximum continuous input/output current	T_{amb} < 70 °C	–	–	1.7	A
Power MOSFETs; note 2						
$R_{DS(on)(N)}$	pin-to-pin resistance NFETs	V_{IN} = 3.5 V	–	65	85	mΩ
$R_{DS(on)(P)}$	pin-to-pin resistance PFETs	V_{IN} = 3.5 V	–	65	85	mΩ
$R_{DS(on)(P\text{-}up)}$	pin-to-pin resistance P-up FET between pins LXB and OUT	V_{OUT} = 1.5 V	–	100	135	mΩ
Timing						
f_{sw}	switching frequency	PWM mode	450	600	750	kHz
f_{sync}	synchronization input frequency		4.5	13	20	MHz
Digital levels: pins SYNC/PWM, SHDWN, SCL and SDA						
V_{IL}	LOW-level input voltage		0	–	0.4	V
V_{IH}	HIGH-level input voltage	note 3	$0.6 \times V_{IN}$	–	V_{IN} + 0.3	V
Temperature						
T_{amb}	ambient temperature		–40	+25	+85	°C
T_{max}	internal cut-off temperature		120	135	150	°C

Notes

1. Current limit level is defined by the external R_{lim} resistor, see Chapter 11.
2. Measured at T_{amb} = 25 °C.
3. To avoid additional supply current, it is advised to use HIGH levels not lower than V_{IN} – 0.5 V.

11 APPLICATION INFORMATION

11.1 Typical Li-Ion, 2- or 3-cell application with I²C-bus programming



The combination of the feedback resistors R1 and R2 in parallel should be approximately 50 kΩ.

D1 and D2 are Schottky diodes

The battery can be a one cell Li-Ion, two cell Alkaline or three cell NiCd/NiMH/Alkaline.

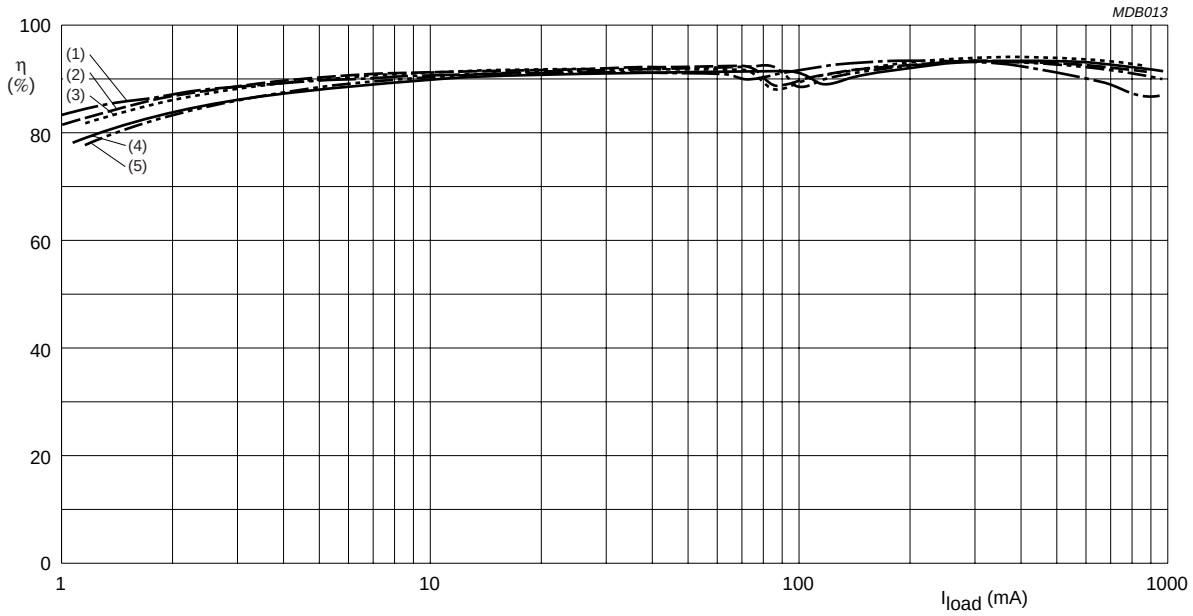
If the I²C-bus interface is used for programming the output voltage, the SCL and SDA lines must be connected to a positive supply via pull-up resistors (see Section 7.12.1). If the I²C-bus interface is not used, connect pins SCL and SDA to ground.

Note the V_{IH}-level (see Chapter 10).

Pins should never be left open-circuit.

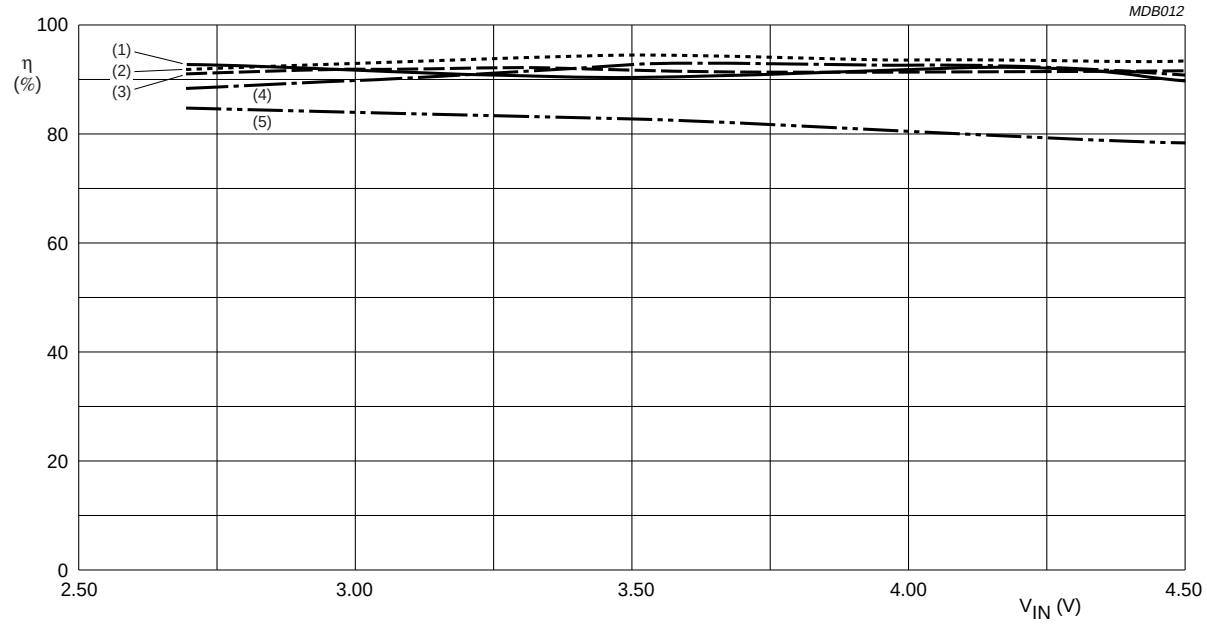
No external clock is applied.

Fig.11 The TEA1211HN in a typical auto-up/down converter application.



V_{OUT} = 3.3 V.
L1 = 10µH, TDK SLF7032 series.
(1) V_{IN} = 2.7 V.
(2) V_{IN} = 3.3 V.
(3) V_{IN} = 3.6 V.
(4) V_{IN} = 4.2 V
(5) V_{IN} = 4.5 V.

Fig.12 Efficiency as a function of load current.



V_{OUT} = 3.3 V.
L1 = 10µH, TDK SLF7032 series.
(1) I_{OUT} = 1000 mA.
(2) I_{OUT} = 500 mA.
(3) I_{OUT} = 100 mA.
(4) I_{OUT} = 10 mA.
(5) I_{OUT} = 1 mA.

Fig.13 Efficiency as a function of input voltage.

11.2 Component selection

11.2.1 INDUCTOR

The inductor should have a low Equivalent Series Resistance (ESR) to reduce losses and the inductor must be able to handle the peak currents without saturating.

Table 3 Inductor selection information

COMPONENT	VALUE	TYPE	SUPPLIER
L1	6.8 μH	DO3316-682	Coilcraft
L1	10 μH	SLF7032T-100M1R4	TDK

11.2.2 CAPACITORS

For the output capacitor the ESR is critical. The output voltage ripple is determined by the product of the current through the output capacitor and its ESR. The lower the ESR, the smaller the ripple. However, an ESR less than 80 mΩ could result in unstable operation.

Table 4 Input and output capacitor selection information

COMPONENT	VALUE	TYPE	SUPPLIER
C_{IN}, C_{OUT}	100 μF/10 V	TPS-series	AVX
		594D-series	Vishay/Sprague

If the I^2C-bus interface is used to program the output voltage, use a larger input capacitor to prevent the under voltage lockout level being triggered by large current peaks drawn from this capacitor.

Table 5 Input capacitor selection information, when I^2C-bus is used

COMPONENT	VALUE	TYPE	SUPPLIER
C_{IN} (I^2C-bus used)	220 to 470 μF/10 V	TPS-series	AVX
		594D-series	Vishay/Sprague

11.2.3 SCHOTTKY DIODES

The Schottky diodes provide a lower voltage drop during the break-before-make time of the internal power FETs. It is advised to use Schottky diodes with fast recovery times.

Table 6 Schottky selection information

COMPONENT	TYPE	SUPPLIER
D1, D2	PRLL5819	Philips

11.2.4 Feedback resistors

The fixed output voltage can be set with the feedback resistors R1 and R2 (see Fig.11). Even in case I^2C-bus is used for programming the output voltage, these external resistors are required for start-up. The ratio of the resistors can be calculated by: $\frac{R1}{R2} = \frac{V_{OUT}}{V_{ref}} - 1$, with $V_{ref} = V_{FB}$ (see Chapter 10).

The two resistors in parallel should have a value of approximately 50 kΩ:

$$\frac{1}{R1} + \frac{1}{R2} \approx \frac{1}{50\ k\Omega}$$

11.2.5 Current Limiter

The maximum input peak current can be set by the current limiter as follows:

$$R_{lim} = \frac{1250}{I_{IN(peak)(max)}}\ \Omega$$

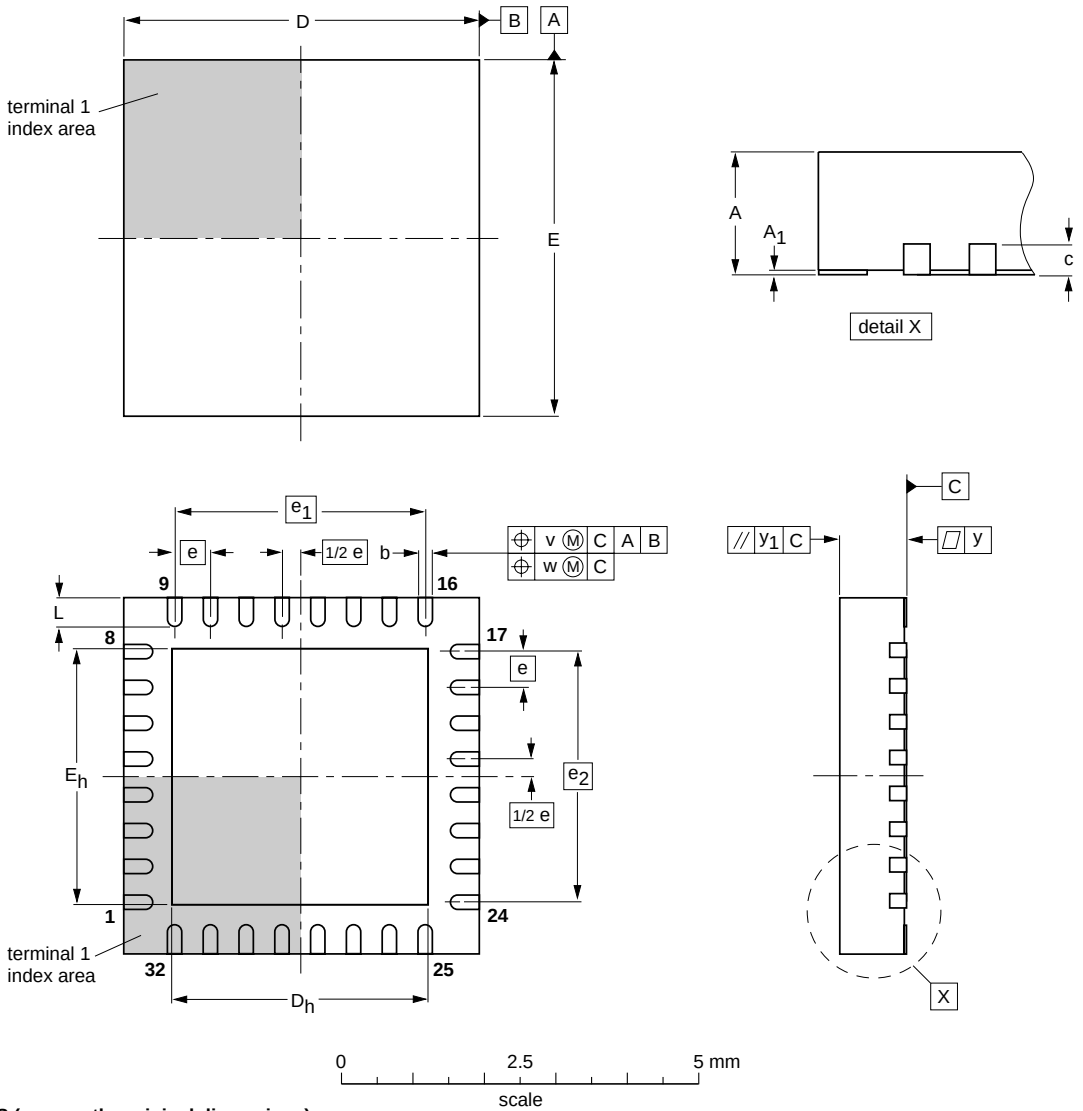
Remark. The output current is not limited: in down conversion, the output current will be higher than the input current, but the maximum continuous output current is not allowed to exceed 1.7 A (RMS) at 70 °C.

Table 7 Resistor selection information

COMPONENT	VALUE	TYPE	TOLERANCE
R1, R2	V_{OUT} dependent	SMD	1 %
R_{lim}	I_{lim} dependent	SMD	1 %

12 PACKAGE OUTLINE

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.75 3.45	5.1 4.9	3.75 3.45	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEIA			
SOT617-3	- - -	MO-220	- - -			~~02-04-18~~ 02-10-22

13 SOLDERING

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
PMFP[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Hot bar or manual soldering is suitable for PMFP packages.

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