

# SYNC separator IC with AFC

## BA7071F

The BA7071F contains a video synchronization separation circuit, a vertical video synchronization separation circuit, a horizontal oscillation circuit, and a phase comparator. It separates and outputs the horizontal and vertical synchronization signals (HD and VD), and the composite synchronization signal (Sync-out) from input video or composite synchronization signals. The phase difference between HD and VD is guaranteed for both the rising and falling edges of VD.

### ●Applications

TVs, VCRs and camcorders

### ●Features

- 1) Built in AFC circuit.
- 2) HD and VD phase difference guaranteed.
- 3) Wide supply voltage range (3V to 7V).
- 4) Horizontal free-run frequency does not require adjustment.
- 5) Low external parts count.
- 6) SOP 8-pin package.

### ●Absolute maximum ratings (Ta = 25°C)

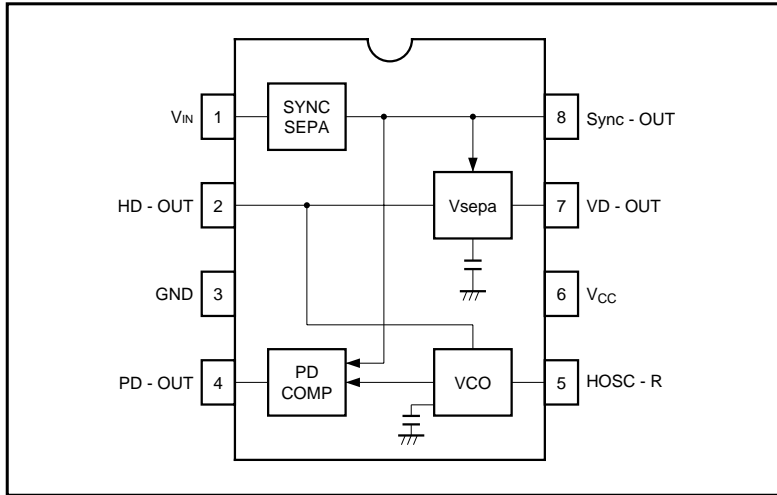
Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>CC</sub>	8.0	V
Power dissipation	P <sub>d</sub>	350*	mW
Operating temperature	T <sub>opr</sub>	- 20 ~ + 75	°C
Storage temperature	T <sub>stg</sub>	- 55 ~ + 125	°C

\* Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

### ●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V <sub>CC</sub>	2.85	—	7.5	V

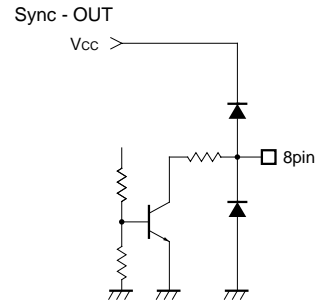
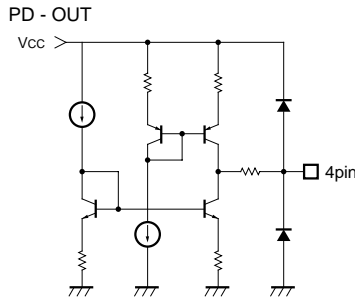
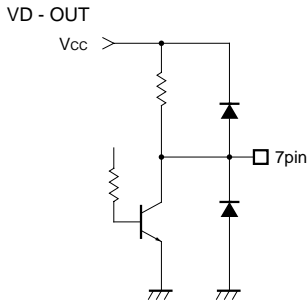
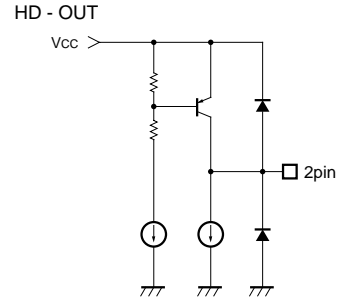
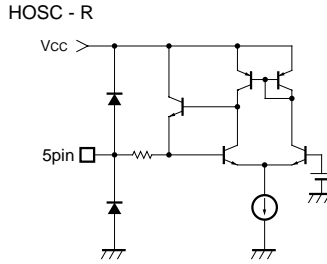
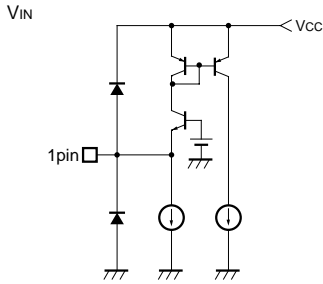
●Block diagram



●Pin descriptions

Pin No.	Pin name	Function
1	V <sub>IN</sub>	Video input
2	HD - OUT	HD output
3	GND	GND
4	PD - OUT	Phase comparator output
5	HOSC - R	Horizontal oscillator resistor
6	V <sub>CC</sub>	Power supply (V <sub>CC</sub> )
7	VD - OUT	VD output
8	Sync - OUT	Synchronization signal output

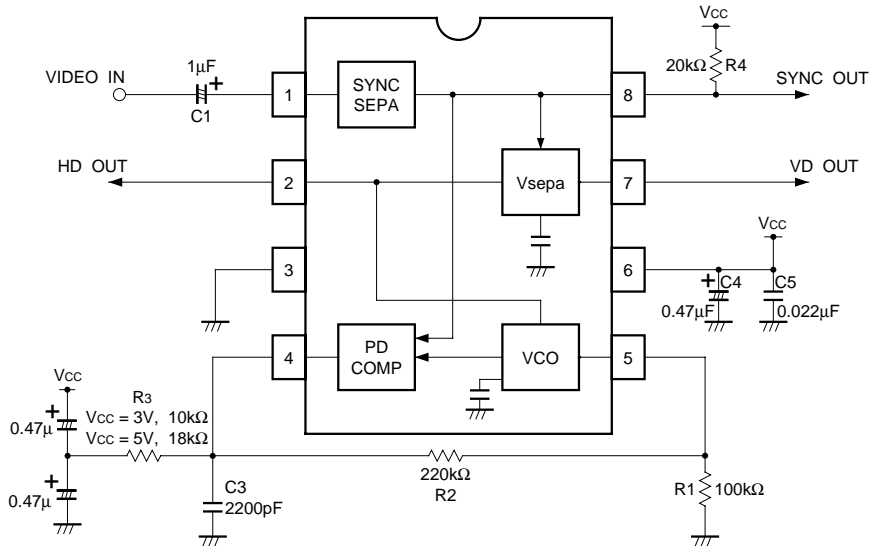
● Input / output circuits



● Electrical characteristics (unless otherwise noted  $T_a = 25^\circ\text{C}$  and  $V_{cc} = 5.0\text{V}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	$I_Q$	3.0	5.8	8.6	mA	pin 8 open
Minimum SYNC separation level	$V_{\text{syn-min}}$	—	0.08	0.15	$V_{\text{P-P}}$	pin 1 terminated with $75\Omega$ resistor
Pulse voltage low	$V_{\text{p-L}}$	—	0.1	0.3	V	pins 2, 7
Pulse voltage high	$V_{\text{p-H}}$	4.7	5.0	—	V	pins 2, 7
(Horizontal) free-running frequency	$f_{\text{H.O}}$	13.5	15.7	17.9	kHz	No input signal
Capture range	$\Delta f_{\text{CAP}}$	2.3	2.7	—	kHz	—
Lock-in phase	$T_{\text{HPH}}$	0.6	1.6	2.6	$\mu\text{s}$	pin 2  pin - 1
HD, VD phase deviation 1	$T_{\text{HVD1}}$	19.0	24.0	29.0	$\mu\text{s}$	pin 7  pin - 2  (FLD1)
HD, VD phase deviation 2	$T_{\text{HVD2}}$	19.0	24.0	29.0	$\mu\text{s}$	pin 7  pin - 2  (FLD1)
HD pulse width	$T_{\text{HD}}$	9.0	10.0	11.0	$\mu\text{s}$	pin 2
VD pulse width	$T_{\text{VD}}$	249	254	259	$\mu\text{s}$	pin 7
$V_{\text{IN}}$ , VD phase difference	$T_{\text{INVD}}$	41.0	48.0	55.0	$\mu\text{s}$	pin 1  pin - 7

● Measurement circuit (application example)



When SYNC SEPA output only is used. HD and VD unused.

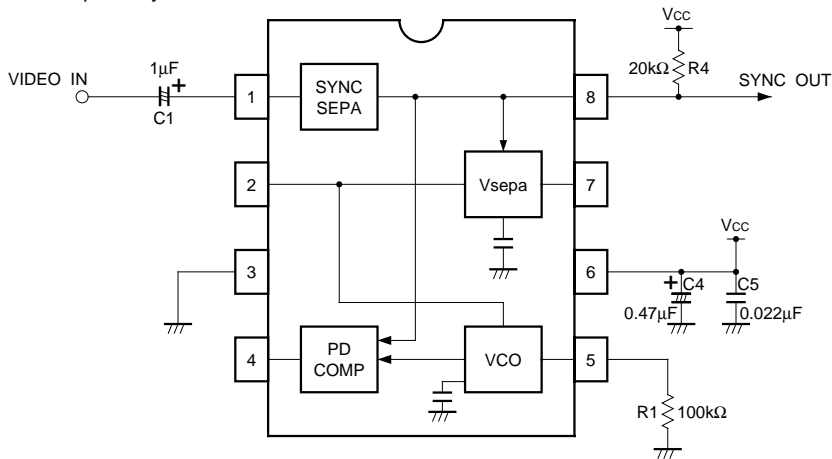


Fig. 1

- (1) Connect a 100kΩ resistor between pin 5 and ground. Leave pins 2, 4 and 7 open.
- (2) SYNC OUT (pin 8) has positive output.
- (3) The SYNC OUT (pin 8) output rise delay times in relation to the VIDEO IN (pin 1) input signal Sync fall are as follows:
  - 830 ns (reference value) ,when Vcc = 5V
  - 880 ns (reference value) ,when Vcc = 3V
- (4) The SYNC OUT (pin 8) output fall delay times in relation to the VIDEO IN (pin 1) input signal Sync rise are as follows:
  - 150 ns (reference value) ,when Vcc = 5V
  - 220 ns (reference value) ,when Vcc = 3V

●Circuit operation

(1) Synchronization separation circuit

Detects the charging current to a externally-connected capacitor, and performs synchronization separation.

(2) Horizontal oscillation circuit

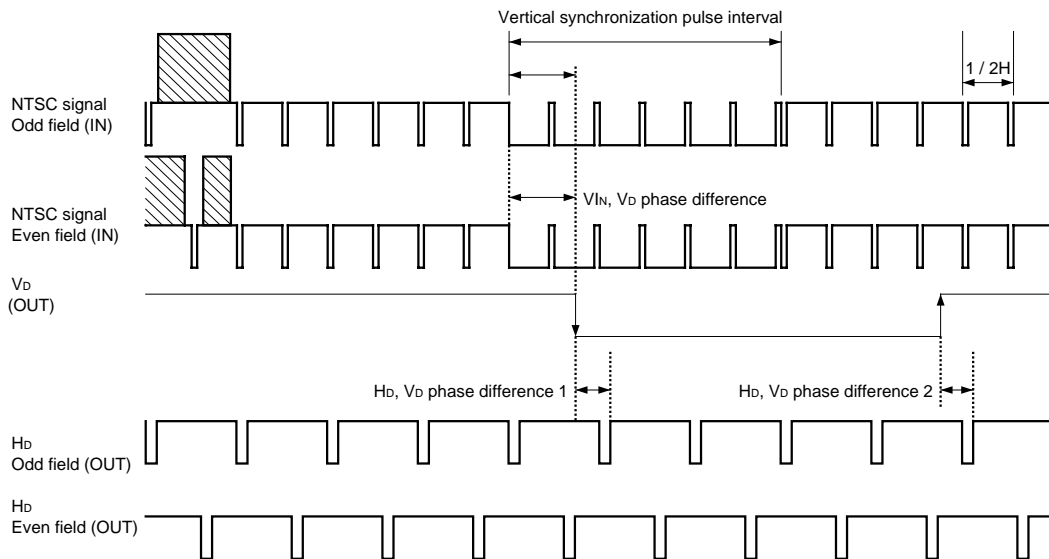
When a video signal is input, it is synchronized with Hsync by the PLL. The horizontal free-running frequency is determined by external resistor R<sub>1</sub>.

$$f_{H \cdot O} = \frac{1.57E6}{R_1} \text{ [kHz]}$$

(3) Vertical synchronization separation circuit

When a video signal is input, synchronization signal separation is done over the vertical synchronization pulse interval.

(4) V<sub>IN</sub>, H<sub>b</sub>, and V<sub>D</sub> timing charts



1. The rise and fall positions for V<sub>D</sub> are basically the same for both odd and even fields.
2. H<sub>b</sub> shifts by 1 / 2H during the odd and even field interval.
3. Only the odd field is given for the specification.

Fig. 2

●Attached components

Resistor R<sub>1</sub> should have a tolerance of ± 2%, and a temperature coefficient of 100ppm or lower.

● Electrical characteristic curves

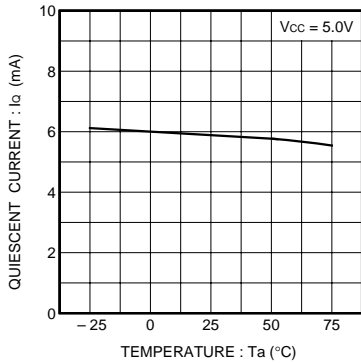


Fig. 3 Quiescent current vs. temperature

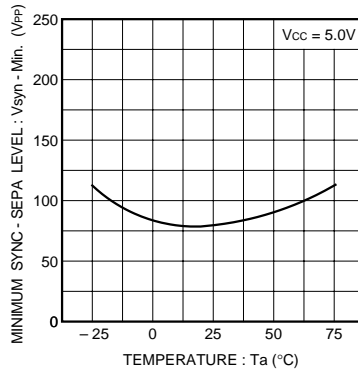


Fig. 4 Minimum synchronization separation level vs. temperature

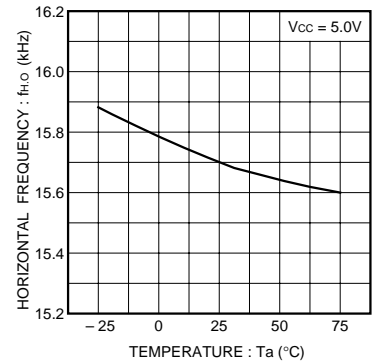


Fig. 5 Horizontal free-running frequency vs. temperature

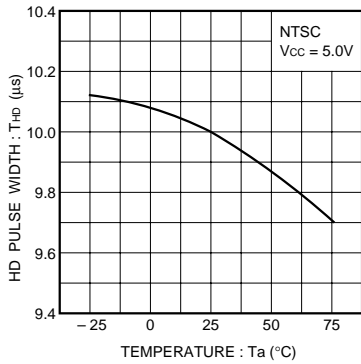


Fig. 6 Hd pulse width vs. temperature

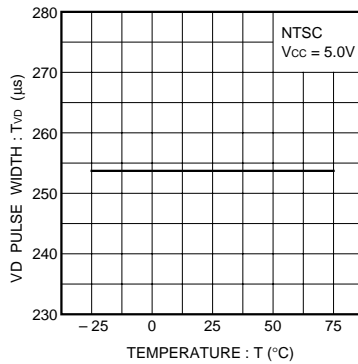


Fig. 7 Vd pulse width vs. temperature

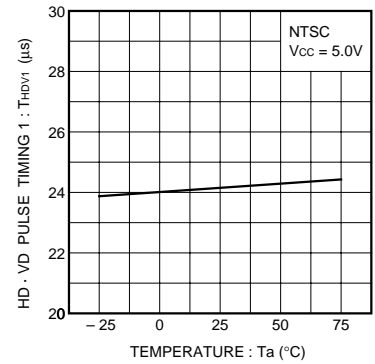


Fig. 8 Hd, Vd phase difference 1 vs. temperature

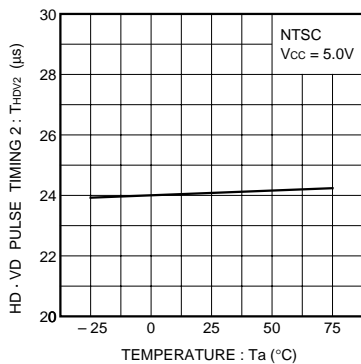


Fig. 9 Hd, Vd phase difference 2 vs. temperature

●External dimensions (Units: mm)

