SONY

CXD2437TQ

Timing Generator for Progressive Scan CCD Image Sensor

Description

The CXD2437TQ is an IC developed to generate the timing pulses required by the Progressive Scan CCD image sensors as well as signal processing circuits.

Features

- External trigger function
- Electronic shutter function
- Supports non-interlaced operation
- 12 frames/s. Double-speed readout (24 frames/s) is also possible by mixing two vertical pixels.
- Base oscillation 40.490496MHz

Applications

Progressive Scan CCD cameras

Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

ICX085AK, ICX085AL

64 pin TQFP (Plastic)
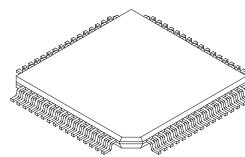
Absolute Maximum Ratings

- Supply voltage V_{DD} $V_{SS} - 0.5$ to $+7.0$ V
- Input voltage V_I $V_{SS} - 0.5$ to $V_{DD} + 0.5$ V
- Output voltage V_O $V_{SS} - 0.5$ to $V_{DD} + 0.5$ V
- Operating temperature
           T_{opr} -20 to $+75$ °C
- Storage temperature
 T_{stg} -55 to $+150$ °C

Recommended Operating Conditions

- Supply voltage V_{DD} 4.75 to 5.25   V
- Operating temperature
           T_{opr} -20 to $+75$ °C

E96319A95-PS

Block Diagram
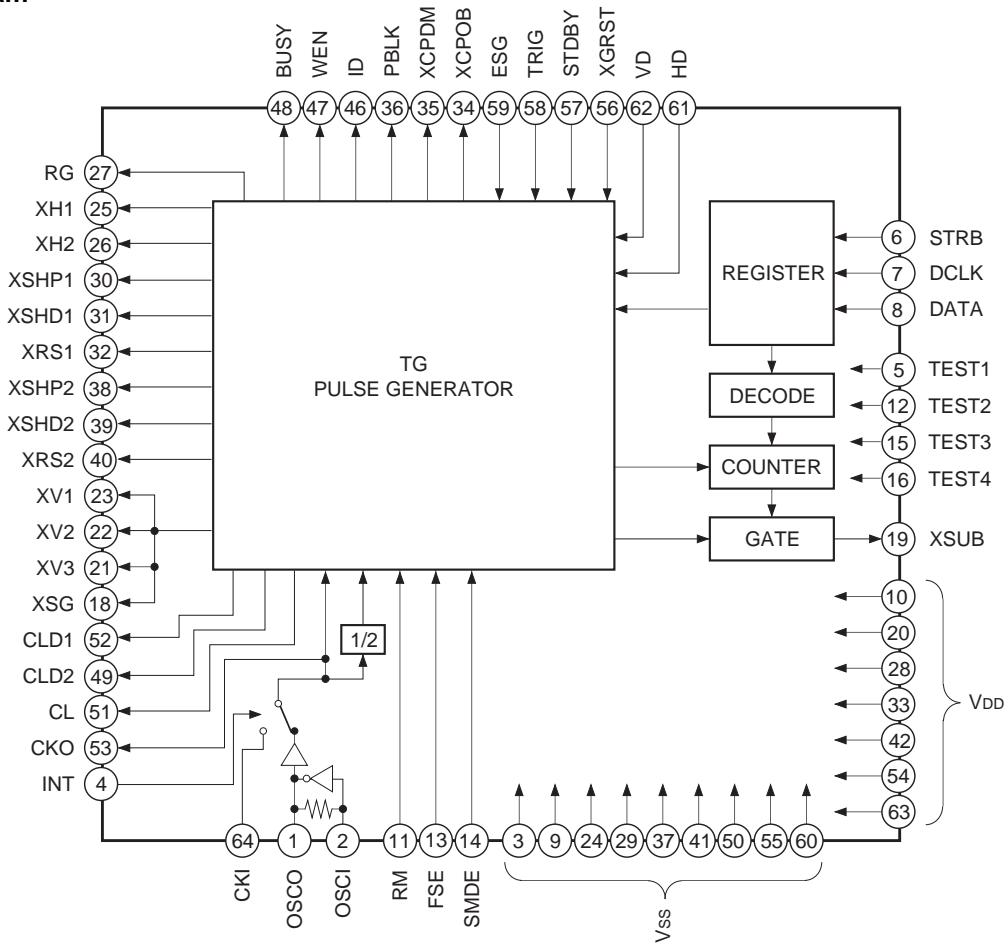
Pin Configuration (Top View)
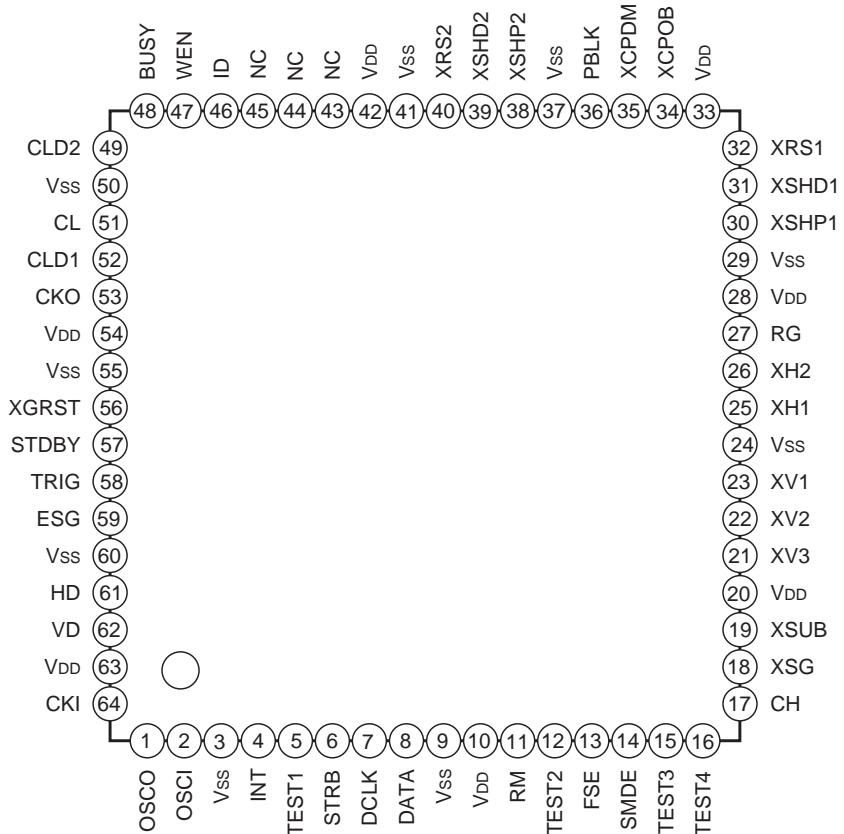
Pin Description

Pin No.	Symbol	I/O	Description
1	OSCO	O	Inverter output for oscillation.
2	OSCI	I	Inverter input for oscillation.
3	Vss	—	GND
4	INT	I	Switching for base oscillation input (with pull-up resistor). High: Oscillation provided by the internal oscillation cell, Low: CKI input valid
5	TEST1	I	Test (with pull-up resistor). Fix to high.
6	STRB	I	Shutter speed setting (with pull-up resistor).
7	DCLK	I	Shutter speed setting (with pull-up resistor).
8	DATA	I	Shutter speed setting (with pull-up resistor).
9	Vss	—	GND
10	VDD	—	Power supply.
11	RM	I	Switching for frame rate (with pull-up resistor). High: Normal readout mode, Low: Double-speed readout mode
12	TEST2	I	Test (with pull-up resistor). Fix to high.
13	FSE	I	Switching for external trigger discharge operation (with pull-up resistor). High: High-speed discharge, Low: No high-speed discharge
14	SMDE	I	Switching for readout timing (with pull-up resistor). High: ESG setting invalid, Low: ESG input valid
15	TEST3	I	Test (with pull-up resistor). Fix to high.
16	TEST4	I	Test (with pull-up resistor). Fix to high.
17	CH	—	Switching for color separated pulse output (with pull-up resistor). High: Normal pulse output mode, Low: Color separated pulse output mode
18	XSG	O	Sensor charge readout pulse output.
19	XSUB	O	CCD discharge pulse output.
20	VDD	—	Power supply.
21	XV3	O	Clock output for vertical CCD drive.
22	XV2	O	Clock output for vertical CCD drive.
23	XV1	O	Clock output for vertical CCD drive.
24	Vss	—	GND
25	XH1	O	Clock output for horizontal CCD drive.
26	XH2	O	Clock output for horizontal CCD drive.
27	RG	O	Reset gate pulse output.
28	VDD	—	Power supply.
29	Vss	—	GND
30	XSHP1	O	Sample-and-hold pulse output.
31	XSHD1	O	Sample-and-hold pulse output.
32	XRS1	O	Sample-and-hold pulse output.
33	VDD	—	Power supply.
34	XCPOB	O	Clamp pulse output.

Pin No.	Symbol	I/O	Description
35	XCPDM	O	Clamp pulse output.
36	PBLK	O	Blanking cleaning pulse output.
37	Vss	—	GND
38	XSHP2	O	Sample-and-hold pulse output.
39	XSHD2	O	Sample-and-hold pulse output.
40	XRS2	O	Sample-and-hold pulse output.
41	Vss	—	GND
42	VDD	—	Power supply.
43	NC		
44	NC		
45	NC		
46	ID	O	Line identification output.
47	WEN	O	Write enable output.
48	BUSY	O	Trigger mode flag.
49	CLD2	O	AD conversion pulse output.
50	Vss	—	GND
51	CL	O	Clock output (1616f$_H$).
52	CLD1	O	AD conversion pulse output.
53	CKO	O	Clock output (3232f$_H$).
54	VDD	—	Power supply.
55	Vss	—	GND
56	XGRST	I	Resets all internal FF. Low: Reset (with pull-up resistor). Always input one reset pulse after power–on.
57	STDBY	I	Standby (with pull-up resistor). High: Normal, Low: Internal clock supply stopped
58	TRIG	I	External trigger input (with pull-up resistor).
59	ESG	I	External readout input (with pull-up resistor).
60	Vss	—	GND
61	HD	I	Horizontal sync signal input.
62	VD	I	Vertical sync signal input.
63	VDD	—	Power supply.
64	CKI	I	Clock input (valid when INT = low).

Electrical Characteristics

1. DC Characteristics   (V_{DD} = 4.75 to 5.25V, Topr = −20 to +75°C)

| Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Input voltage 1 (Input pins other than those listed below)	V_{IH1}		$0.7V_{DD}$			V
	V_{IL1}				$0.3V_{DD}$	V
Input voltage 2 (Pin 2)	V_{IH2}		$0.7V_{DD}$			V
	V_{IL2}				$0.3V_{DD}$	V
Output voltage 1 (Output pins other than those listed below)	V_{OH1}	I_{OH} = −2.5mA	V_{DD} − 0.4			V
	V_{OL1}	I_{OL} = 4.5mA			0.4	V
Output voltage 2 (Pins 30, 31, 32, 38, 39, 40, 49, 51, 52 and 53)	V_{OH2}	I_{OH} = −5.0mA	V_{DD} − 0.4			V
	V_{OL2}	I_{OL} = 9.0mA			0.4	V
Output voltage 3 (Pins 25, 26 and 27)	V_{OH3}	I_{OH} = −7.5mA	V_{DD} − 0.4			V
	V_{OL3}	I_{OL} = 13.5mA			0.4	V
Output voltage 4 (Pin 1)	V_{OH4}		V_{DD}/2			V
	V_{OL4}				V_{DD}/2	V
Feedback resistor	R_{FB}	V_{IN} = V_{SS} or V_{DD}		1M		Ω
Pull-up resistor	R_{PU}	V_{IL} = 0V		50k	100k	Ω
Pull-down resistor	R_{PD}	V_{IH} = V_{DD}		50k	100k	Ω
Current consumption	I_{DD}	V_{DD} = 5V		60		mA

2. AC Characteristics

1) Waveform characteristics of XH1, XH2 and RG
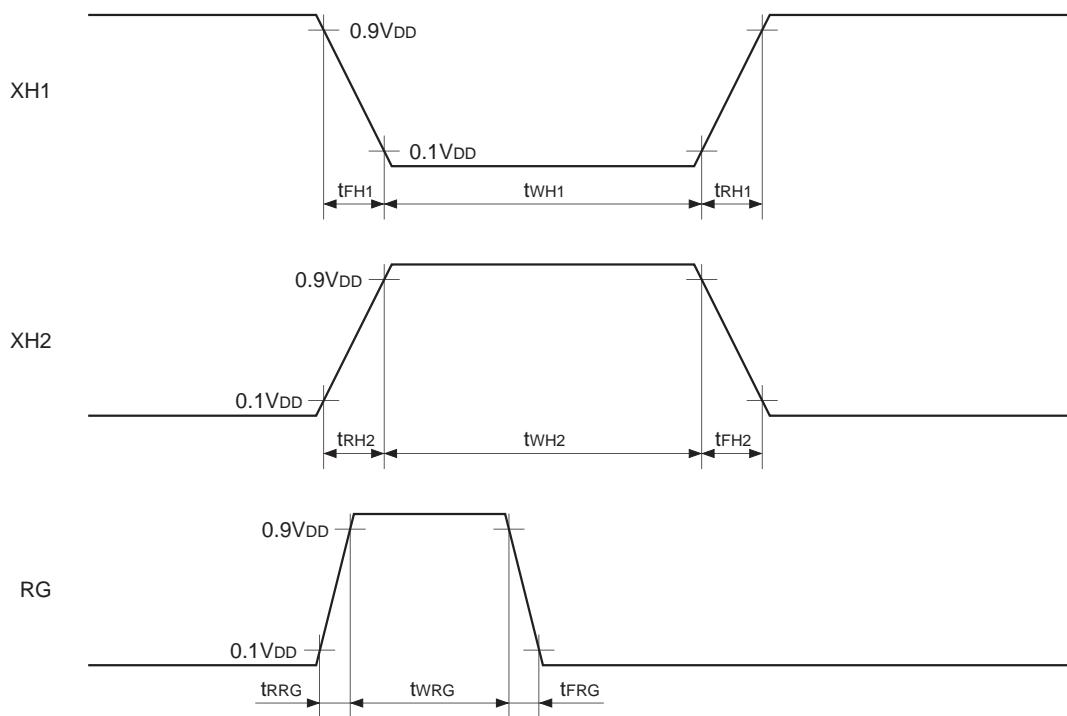
(V_{DD} = 5.0V, Topr = 25°C, load capacitance of XH1 and XH2 = 30pF, load capacitance of RG = 10pF)

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{RH1}	XH1 rise time		3		ns
t_{FH1}	XH1 fall time		3		ns
t_{WH1}	XH1 low level time		25		ns
t_{RH2}	XH2 rise time		3		ns
t_{FH2}	XH2 fall time		3		ns
t_{WH2}	XH2 high level time		25		ns
t_{RRG}	RG rise time		2		ns
t_{FRG}	RG fall time		2		ns
t_{WRG}	RG high level time		12		ns

2) Phase characteristics of XH1, XH2, RG, XSHP, XSHD, XRS, CL, CLD and CKO
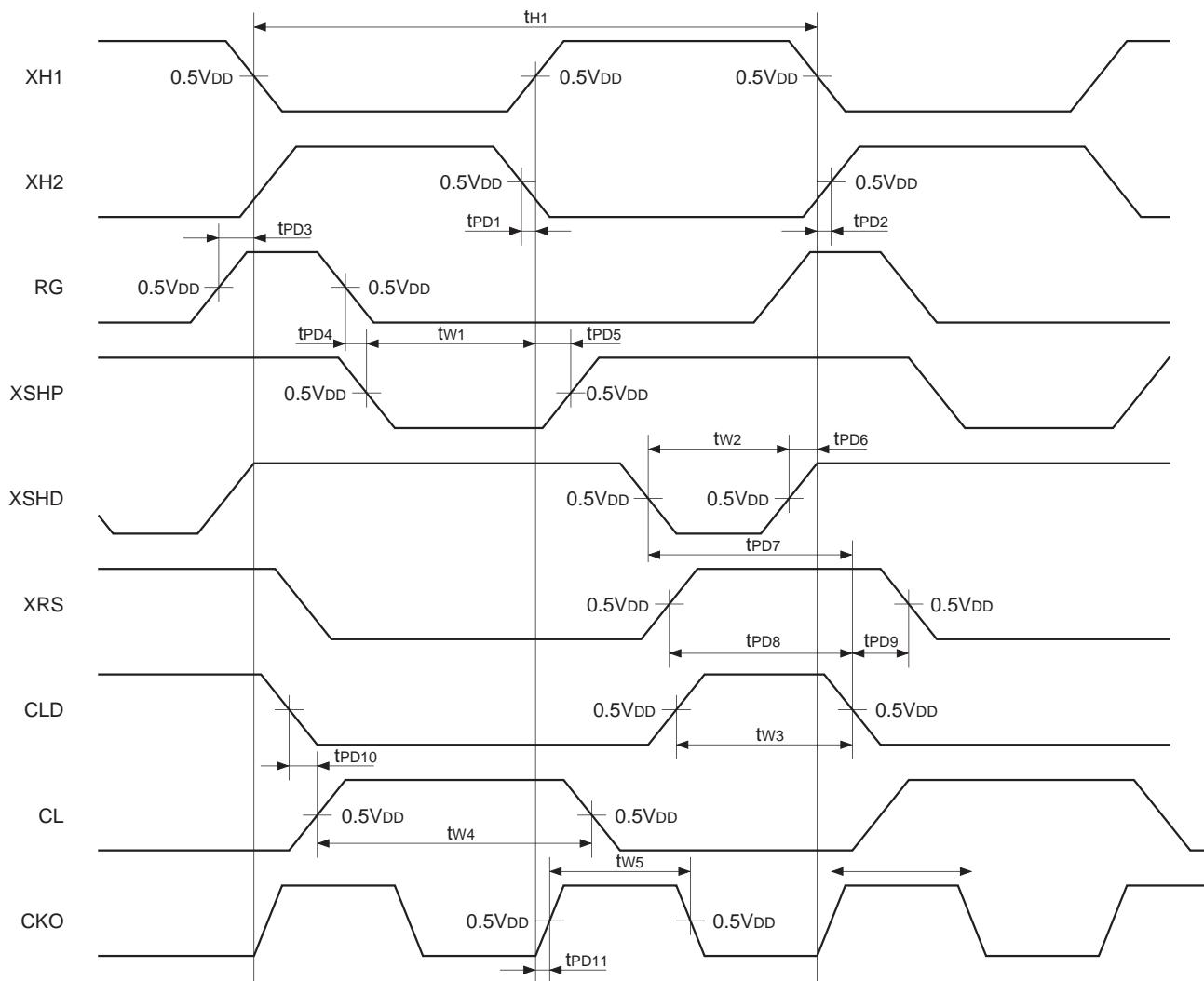

(V_{DD} = 5.0V, Topr = 25°C, load capacitance of CL and CKO = 30pF, load capacitance of CLD, XSHP, XSHD, XRS and RG = 10pF)

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{H1}	XH1 cycle		49.4		ns
t_{PD1}	XH2 falling delay, activated by the rising edge of XH1		0		ns
t_{PD2}	XH2 rising delay, activated by the falling edge of XH1		0		ns
t_{PD3}	XH1 falling delay, activated by the rising edge of RG		4		ns
t_{PD4}	XSHP falling delay, activated by the falling edge of RG		4.5		ns
t_{PD5}	XSHP rising delay, activated by the rising edge of XH1		9		ns
t_{PD6}	XH1 falling delay, activated by the rising edge of XSHD		3		ns
t_{PD7}	CLD falling delay, activated by the falling edge of XSHD		23		ns
t_{PD8}	CLD falling delay, activated by the rising edge of XRS		21.5		ns
t_{PD9}	XRS falling delay, activated by the falling edge of CLD		9		ns
t_{PD10}	CL rising delay, activated by the falling edge of CLD		2.5		ns

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{PD11}	CKO rising delay, activated by the falling (rising) edge of XH1		2.5		ns
t_{W1}	XSHP pulse width		21		ns
t_{W2}	XSHD pulse width		20		ns
t_{W3}	CLD pulse width		21		ns
t_{W4}	CL pulse width		25		ns
t_{W5}	CKO pulse width		11.5		ns

## 3) Phase conditions of HD, VD, TRIG and ESG
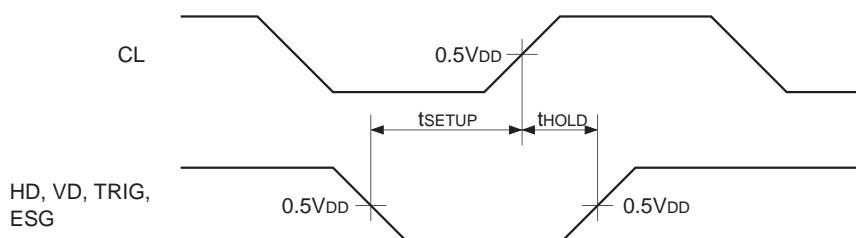
(V_{DD} = 5.0V, Topr = 25°C, load capacitance of CL = 30pF)

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{SETUP}	HD, VD, TRIG and ESG setup time, activated by CL	6			ns
t_{HOLD}	HD, VD, TRIG and ESG hold time, activated by CL	6			ns

3) Phase conditions of HD, VD, TRIG and ESG
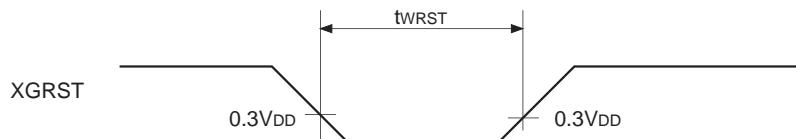
(Within the recommended operating condition)

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{WRST}	XGRST pulse width	50			ns

5) Phase characteristics of XV1, XV2, XV3, XSG, XSUB, PBLK, XCPDM, XCPOB, BUSY, WEN and ID
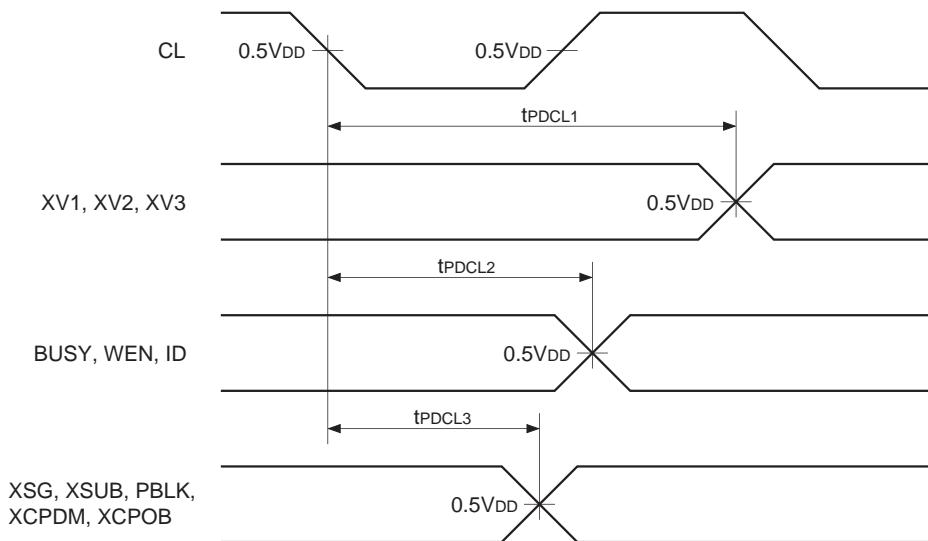
(V_{DD} = 5.0V, Topr = 25°C, load capacitance of CL = 30pF,
load capacitance of XV1, XV2, XV3, XSG, XSUB, PBLK, XCPDM, XCPOB, BUSY, WEN and ID = 10pF)

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{PDCL1}	XV1, XV2 and XV3 delay, activated by the falling edge of CL	20		30	ns
t_{PDCL2}	BUSY, WEN and ID delay, activated by the rising edge of CL	20		35	ns
t_{PDCL3}	XSG, XSUB, PBLK, XCPDM and XCPOB delay, activated by the rising edge of CL	15		30	ns

Description of Functions

1. Progressive Scan CCD drive pulse generation

- Combining this IC with a crystal oscillator generates a fundamental frequency of 40.49MHz.
- CCD drive pulse generation is synchronized with the HD and VD inputs.
- Setting the RM pin to low sets the frame rate to double-speed readout mode (24 frames/s). However, the CCD vertical resolution is halved.
- $f_{CL} = 1616f_{HD}$, $f_{HD} = 1044f_{VD}$ (normal readout mode: RM = high)
- $f_{CL} = 1616f_{HD}$, $f_{HD} = 522f_{VD}$ (double-speed readout mode: RM = low)
- The various operations are performed by the TRIG and ESG inputs. (See the following items.)

<Detection timing for VD, RM, TRIG and ESG>
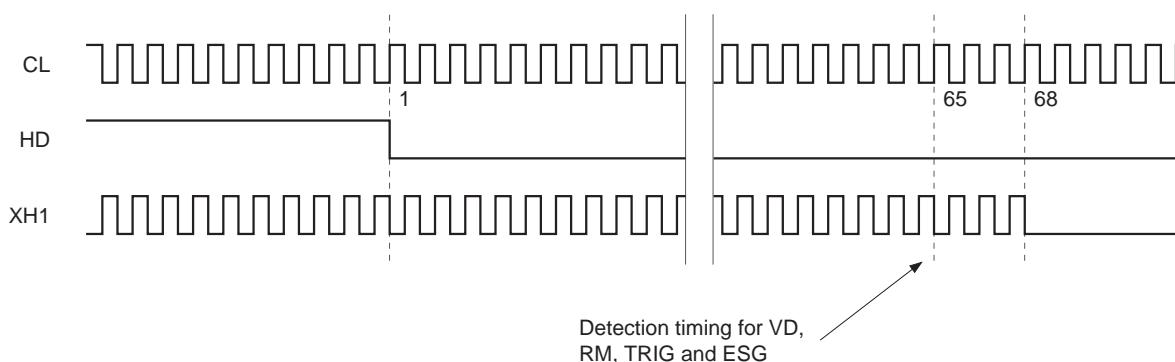
After HD input is detected, VD, RM, TRIG and ESG are detected at the rising edge of the 65th CL pulse. However, the low level period for each pulse should be set to 1H or longer to prevent misoperation.

2. Electronic shutter

<Shutter modes>
The electronic shutter has the following four shutter modes.
- Electronic shutter off: Exposure time is 1/12s (RM = high) or 1/24s (RM = low)
- High-speed electronic shutter: Exposure time is shorter than 1/12s (RM = high) or 1/24s (RM = low)
- Low-speed electronic shutter: Exposure time is longer than 1/12s (RM = high) or 1/24s (RM = low)

<Shutter mode and speed setting methods>
The shutter speed is set serially using the STRB, DCLK and DATA pins. The electronic shutter mode and the meanings of the numbers indicated by D0 to 10 vary according to the SMD1 and SMD2 settings of the internal register.
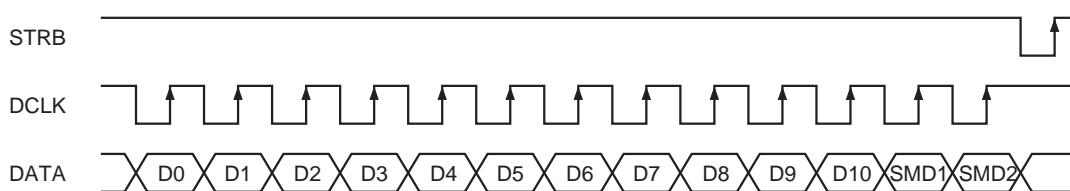
SMD1	SMD2	Mode	D0 to 10
H	H	Electronic shutter off (1/12s accumulation[*1])	—
L	H	High-speed electronic shutter	Number of exposed lines[*2]
H	L	Low-speed electronic shutter	Number of exposed frames[*3]
L	L	Electronic shutter off (1/12s accumulation[*1])	—

[*1] When RM = high. 1/24s accumulation when RM = low.

[*2] Relationship between the number of exposed lines and the exposure time

The relationship between the number of exposed lines and the exposure time is as follows.

(Exposure time) = (Number of exposed lines) $\times$ (One horizontal scan period) + (Accumulation time for the readout lines)

In this formula, one horizontal scan period equals the HD falling interval, and the accumulation time for the readout lines is the time from the rising edge of XSUB to the falling edge of XSG (510 bits). Also, the number of exposed lines should be set to greater than 1 but less than 1043.

[*3] The number of exposed frames should be set to greater than 1 but less than 120. During external trigger mode, the number of exposed frames should be set to greater than 2.

Timing Chart
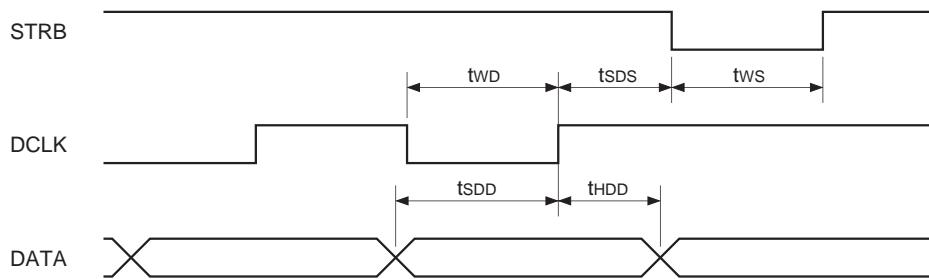
AC characteristics for serial input

Symbol	Definition	Min.	Max.	Unit
t_{SDD}	DATA setup time, activated by the rising edge of DCLK	10	—	ns
t_{HDD}	DATA hold time, activated by the rising edge of DCLK	10	—	ns
t_{SDS}	DCLK setup time, activated by the falling edge of STRB	30	—	ns
t_{WS}	STRB pulse width	82	—	ns
t_{WD}	DCLK pulse width	82	—	ns

3. External trigger mode

External trigger mode starts exposure in sync with the external trigger input. No special pins are required to set this mode. Note that during external trigger mode, normal readout mode results regardless of the RM status. The IC prepares to shift to external trigger mode with the rising edge of the TRIG pin.[1] The timing to shift to external trigger mode varies according to the mode setting. (See the table.) The BUSY pin maintains high status during external trigger mode. Whether or not to discharge the vertical CCD charge is set by FSE just after shifting to external trigger mode.

[1] See the detection timing for VD, TRIG and ESG.

Mode settings during external trigger

SMD1	SMD2	Description of operation
L	L	Trigger input is not accepted. Fix SMDE to high.
L	H	The IC is shifted to external trigger mode by HD, exposure is finished after the set time, and XSG is output.[2]
H	L	The IC is shifted to external trigger mode by VD and exposure is finished in sync with VD after the set time.[2]
H	H	Trigger input is not accepted. Fix SMDE to high

[2] The exposure time setting method is the same as the exposure time setting for the electronic shutter.

<FSE and discharge operation>
During external trigger mode, the previously exposed signal charge sometimes remains in the vertical CCD when exposure finishes. In this case, the image shot with external trigger mode is output overlapped with the previously shot image.

Setting FSE to high performs discharge operation for signal charges remaining in the vertical CCD after trigger input. Discharge operation is not performed when FSE is low. This setting is only valid when using the high-speed shutter.

<Finishing the exposure period with ESG>
During external trigger mode, exposure can be finished in sync with the falling edge of ESG.[3] If SMDE is set to low, the XSG pulse is output regardless of the electronic shutter setting, when the falling edge of ESG is detected. ESG should be fixed to high status at all times other than during external trigger mode.

[3] See the detection timing for VD, TRIG and ESG.

<Signal after external trigger mode>
After high-speed external trigger mode is finished, the exposure time differs from that performed by the electronic shutter setting. This is because the start and finish of external trigger mode are not synchronized to VD input.

4. Internal logic stop (standby mode)

When the STDBY pin is set to low, clock supply is stopped to a part of the internal logic. However, output from the oscillation cell (OSCI and OSCO pins) as well as the CL and CKO pins does not stop. The status of each output pin when STDBY is low is shown below.

    High: XSUB, XSG

    Low: RG, XH1, XH2, XV1, XV2, XV3, XSHP, XSHD, XRS, XCPOB, XCPDM, PBLK, ID, WEN, BUSY, CLD

    Not stopped: OSCO, CL, CKO

5. Color separated pulse output mode

• CDS/AGC can be supported to the system which performs with 2-channel by setting CH pin to low. When using CH pin at high, leave XSHP2, XSHD2, XRS2 and CLD2 pins open, respectively.

• XSHP, XSHD, XRS and CLD pins operate as shown in the figure below.

Note) XSHP = XSHP1 and XSHP2, XSHD = XSHD1 and XSHD2
XRS = XRS1 and XRS2, CLD = CLD1 and CLD2

High-speed pulse when CH = low
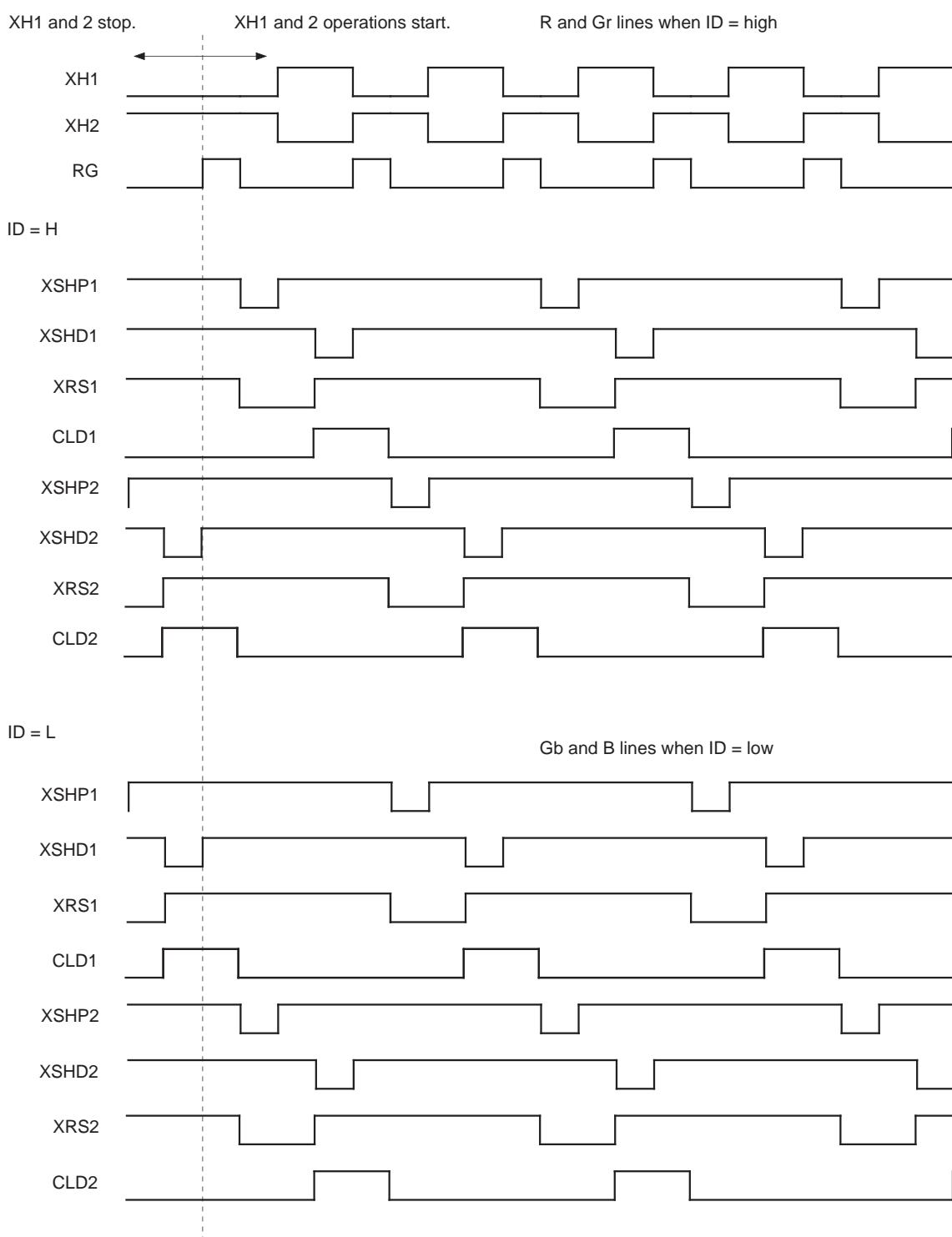
6. Mode settings

6-1. VD input-related

BUSY	SMD1	SMD2	SMDE	VD input	
H	L	H	X	Invalid	
	H	L	L	Exposure is started from the first VD input.	
			H	Readout operation or the number of accumulated frames is counted.	
L	L	H	X	Readout operation is performed.	
	H	H			
	L	L			

Notes) 1. SMD1 and SMD2 indicate the corresponding internal register values.
2. See "2. Electronic shutter".

6-2. TRIG and ESG input-related

BUSY		SMDE	TRIG*4	ESG
H	Discharge period*1	X	Prohibited	Prohibited*5
	Exposure period	H		
		L		Readout operation*5
	Signal output period	X		Prohibited*5
L	Before TRIG input	H	IC shifted to external trigger mode*3	Prohibited*6
		L		
	After TRIG input*2,*3	H	Prohibited	
		L		

*1 Only when FSE is high.

*2 Valid only during low-speed shutter.

*3 See "3. External trigger mode".

*4 Do not re-input the TRIG pulse until BUSY goes low.

*5 ESG input is valid only one time after TRIG input. Do not input ESG two times or more.

*6 Lock ESG to high status when BUSY is low.

6-3. List of Timing Charts

SMD1	SMD2	RM	FSE	SMDE	BUSY	Timing chart	Vertical/ Horizontal	Operation
X	X	H	X	X	L	Chart-1	Vertical	Normal readout
					X	Chart-2	Horizontal	Normal readout
		L			L	Chart-3	Vertical	Double-speed readout
					X	Chart-4	Horizontal	Double-speed readout
		X				Chart-5	Horizontal	Readout operation
		L → H			L	Chart-6	Vertical	Shifting from normal readout to double-speed readout
		H → L				Chart-7	Vertical	Shifting from double-speed readout to normal readout
L	H	H	H	H	H	Chart-8	Vertical	During external trigger input, discharge
		L				Chart-9	Vertical	During external trigger input, discharge, double-speed
		X				Chart-10	Horizontal	During external trigger input, (discharge operation)
		H	L			Chart-11	Vertical	During external trigger input, no discharge
		L				Chart-12	Vertical	During external trigger input, no discharge, double-speed
H	L	H	X			Chart-13	Vertical	During external trigger input, low-speed shutter
		L				Chart-14	Vertical	During external trigger input, low-speed shutter, double-speed
L	H	H	H	L		Chart-15	Vertical	During external trigger input, ESG

Chart-1 **Normal Operation: Vertical synchronization**

VD
HD
OUT
XV1
XV2
XV3
XSG
XSUB
PBLK
XCPOB
XCPDM
ID
WEN
BUSY

1030
1037
1036

1 2 3 4 5 6 7 8

6
3
1

See "2. Electronic shutter" for the number of XSUB pulses.
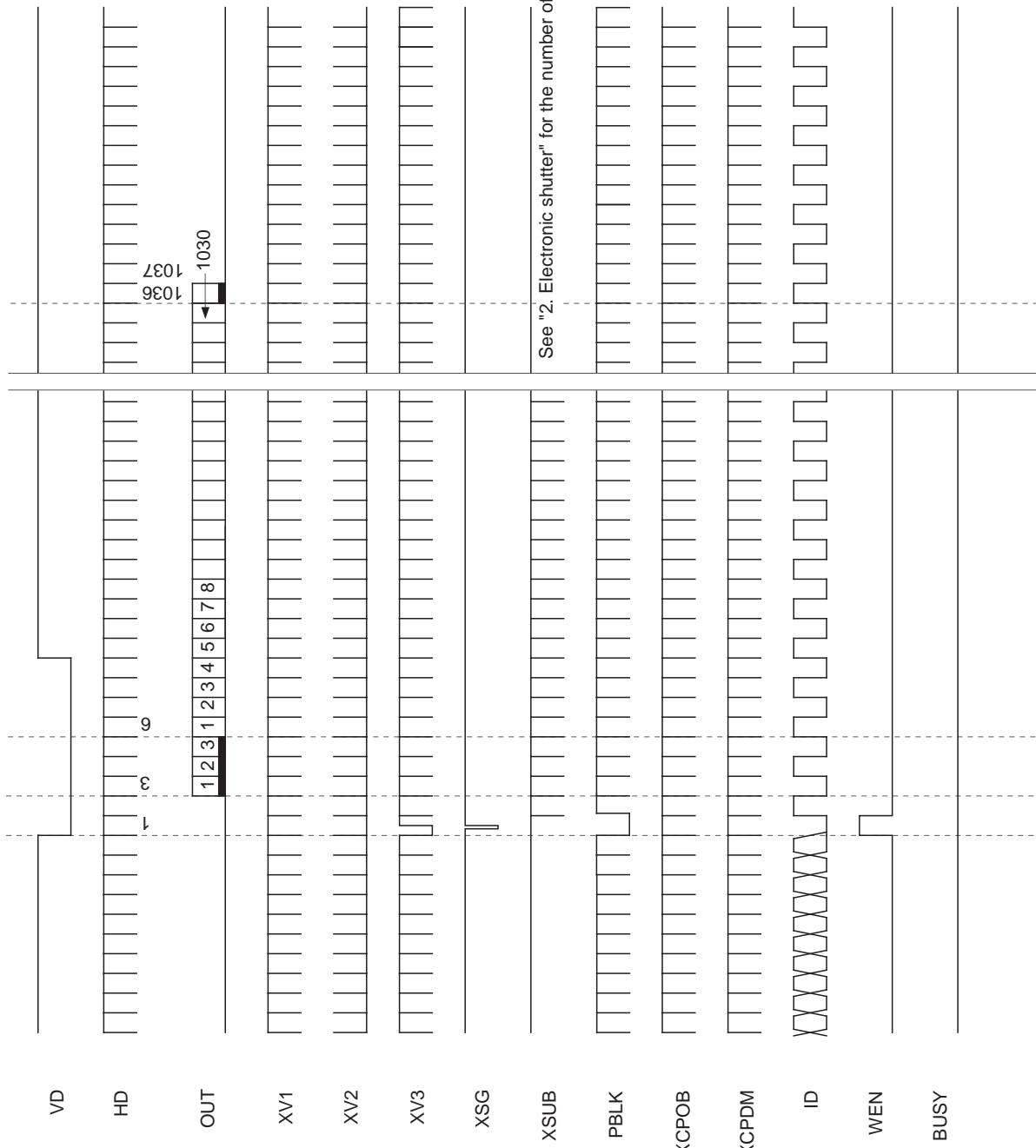
Chart-2 Normal Operation: Horizontal synchronization
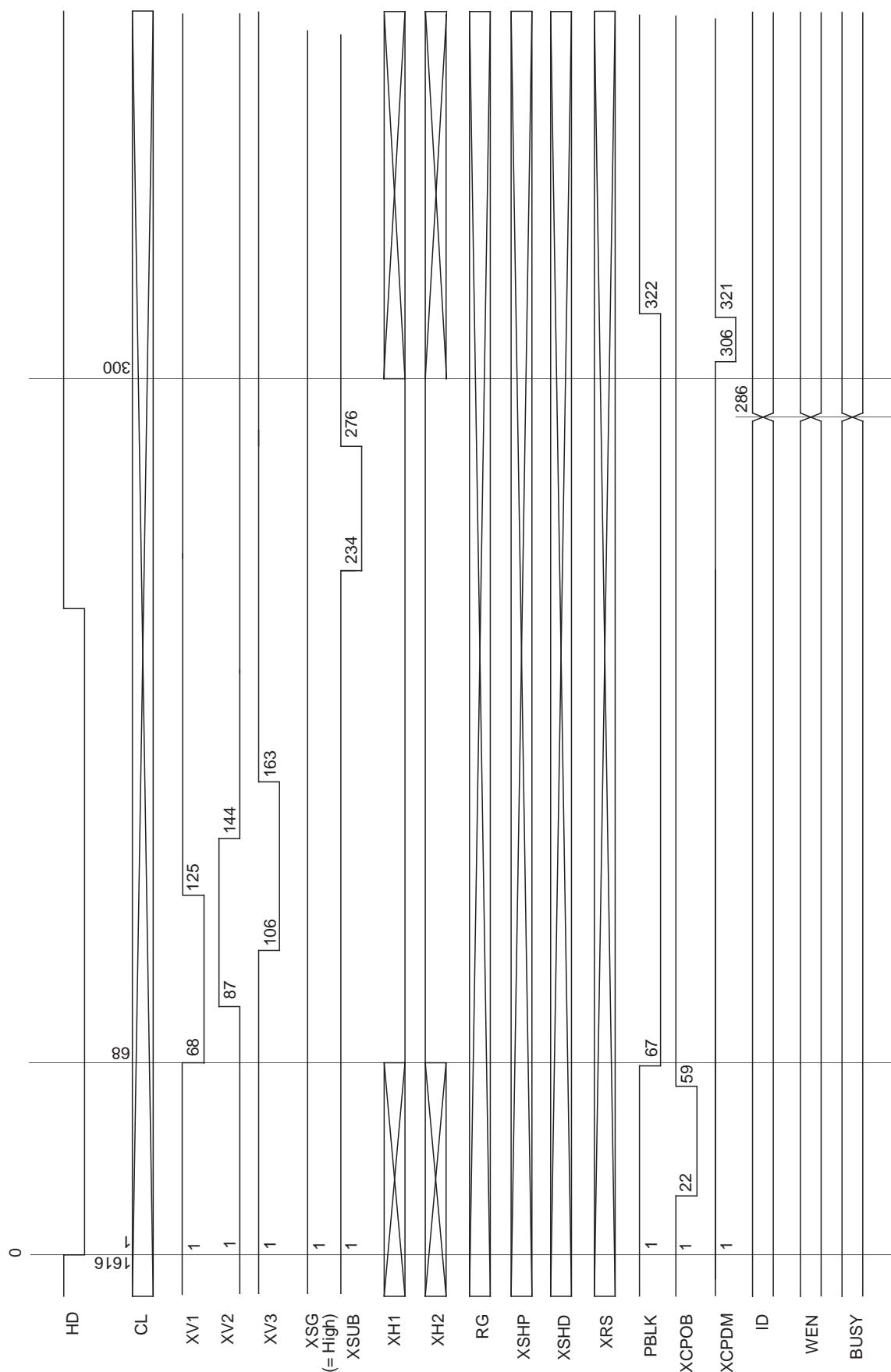
Chart-3   Normal Operation, Double-speed Mode (RM = low): Vertical synchronization

See "2. Electronic shutter" for the number of XSUB pulses.

VD
HD
OUT
XV1
XV2
XV3
XSG
XSUB
PBLK
XCPOB
XCPDM
ID
WEN
BUSY
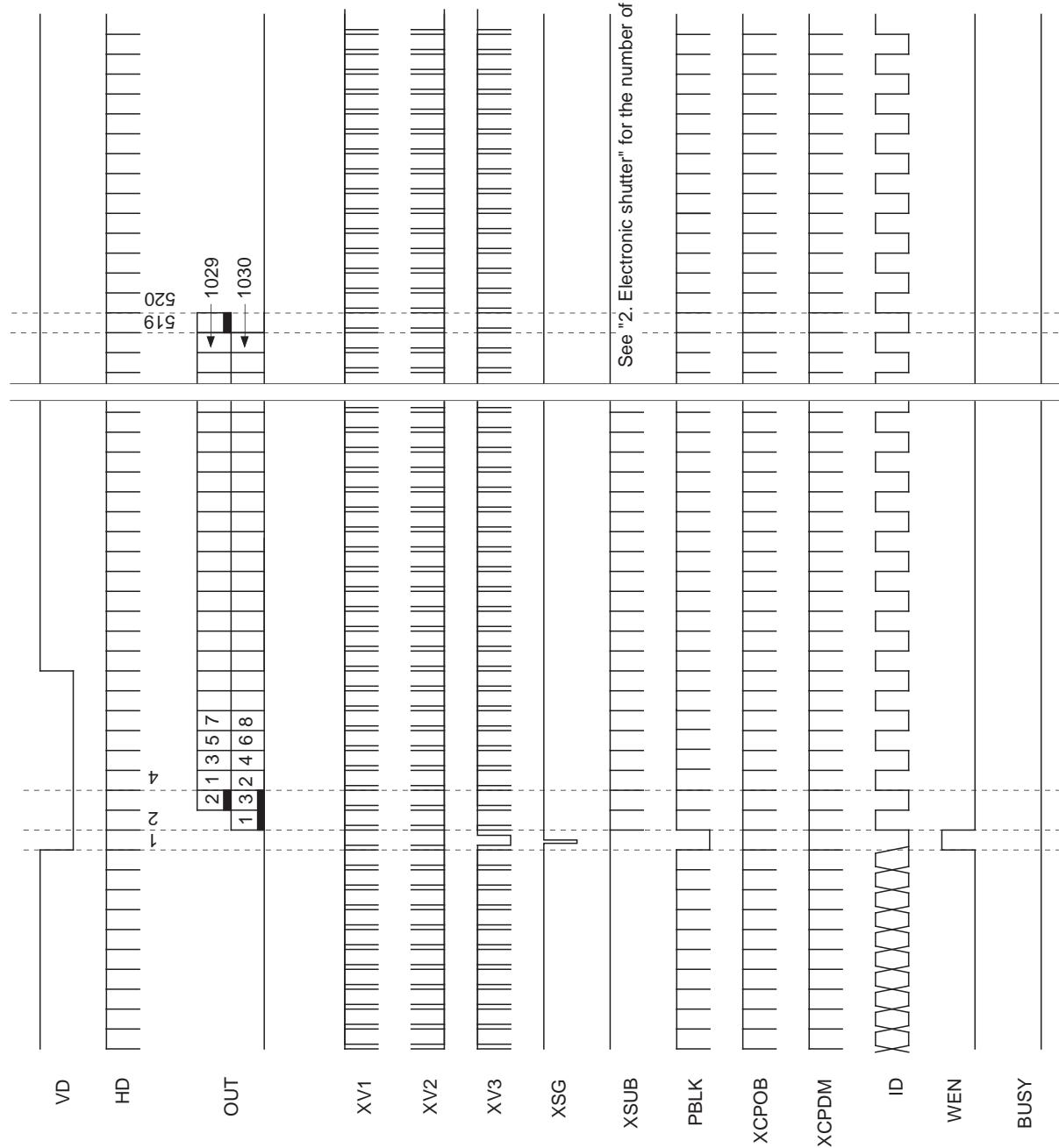
Chart-4   Normal Operation, Double-speed Mode (RM = low): Horizontal synchronization
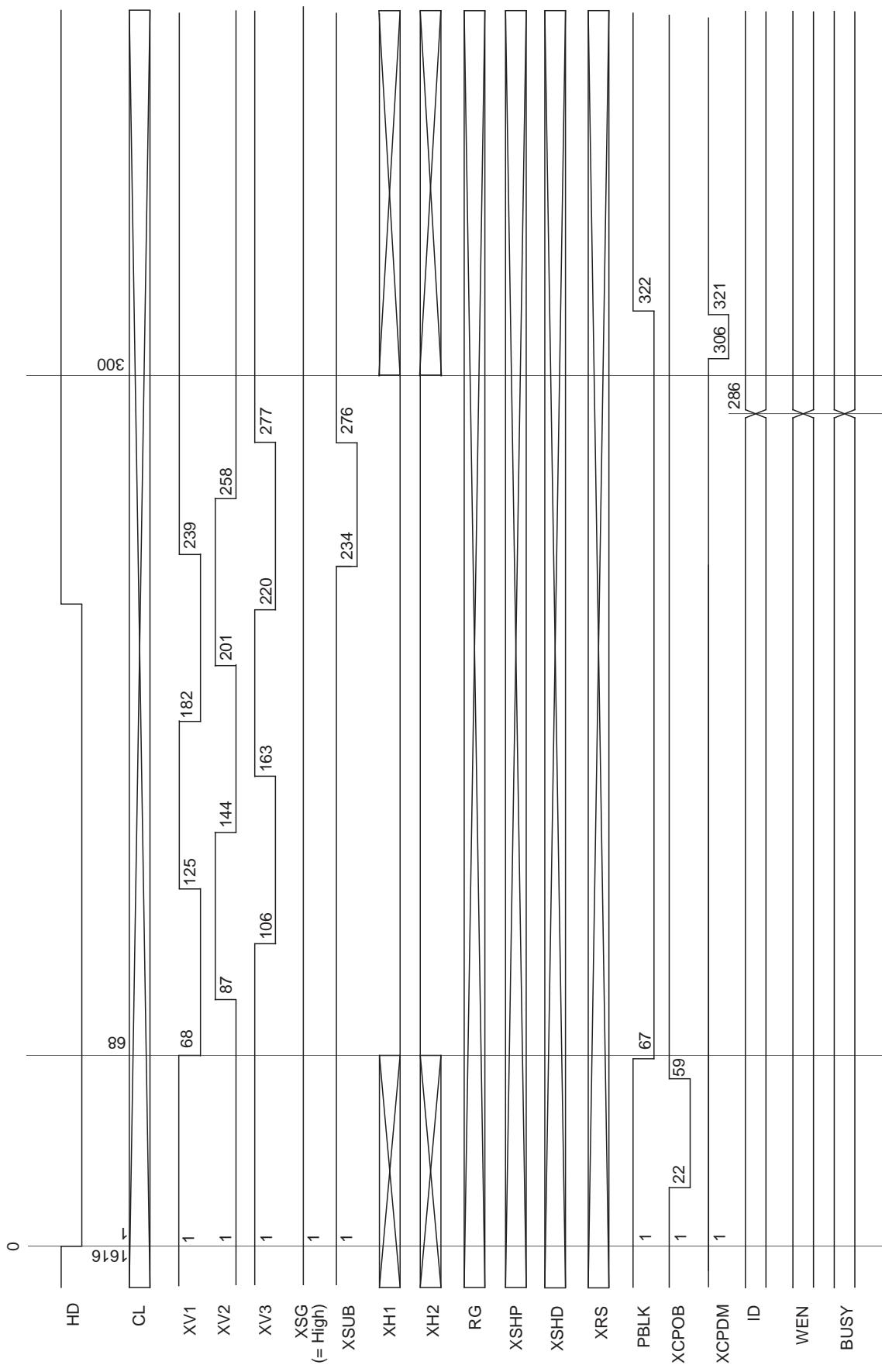
Chart-5 Readout Operation: Horizontal synchronization

HD

CL

89

1

Normal readout

XSG   684   786   1

XV1   68   125   1

XV2   87   144   1

XV3   106   163   868   106   1

PBLK   67   322   1

Double-speed readout

XSG   684   786   1

XV1   68   125   182   239   68   125   182   239   1

XV2   87   144   201   258   87   144   201   258   1

XV3   106   163   220   868   106   163   220   277   1

PBLK   67   322   1
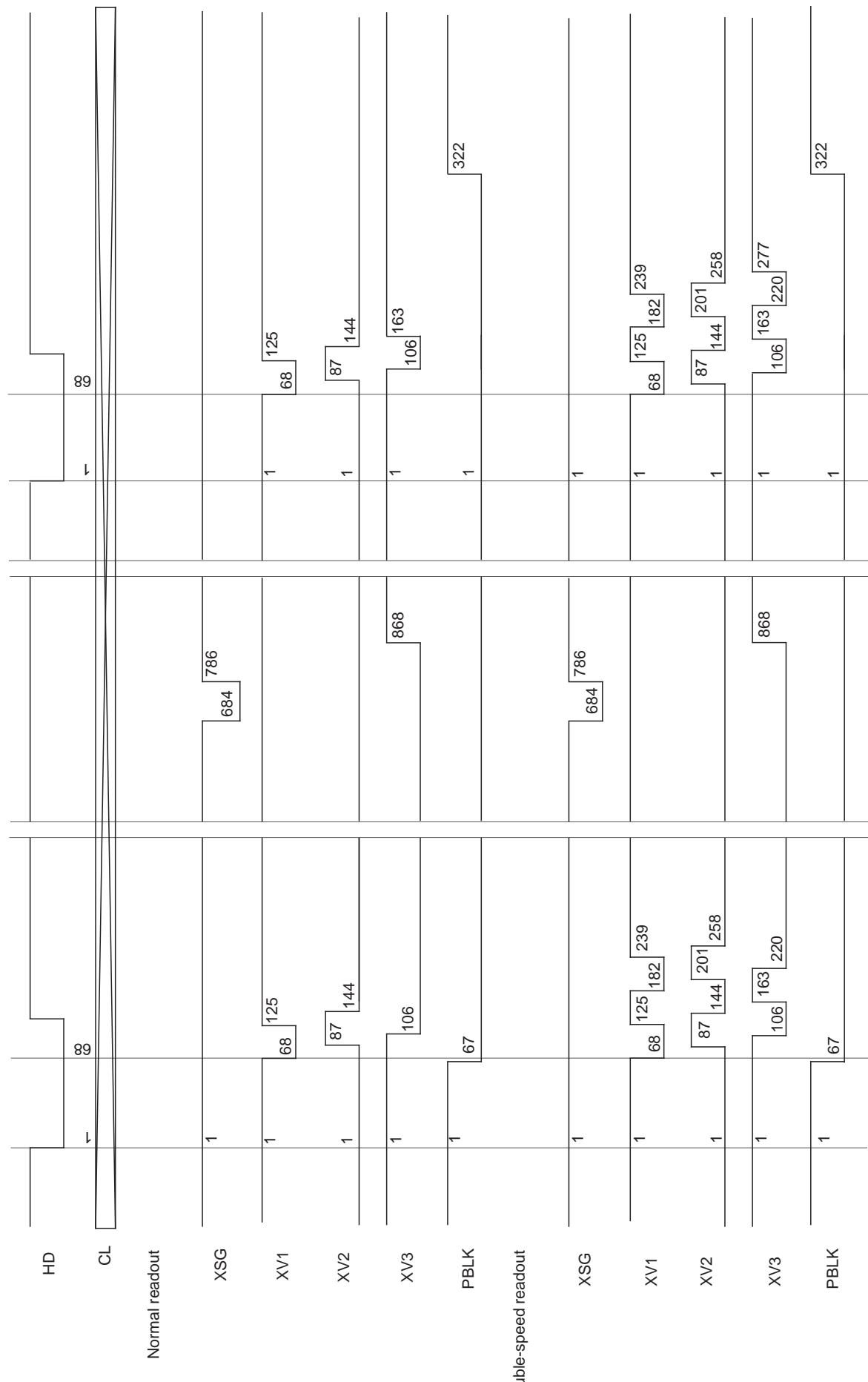
Chart-6   Switching from Normal Mode (RM = high) to Double-speed Mode (RM = low)

RM is reflected from the next VD.

See "2. Electronic shutter" for the number of XSUB pulses.

RM

VD

HD

OUT

XV1

XV2

XV3

XSG

XSUB

PBLK

XCPOB

XCPDM

ID

WEN

BUSY
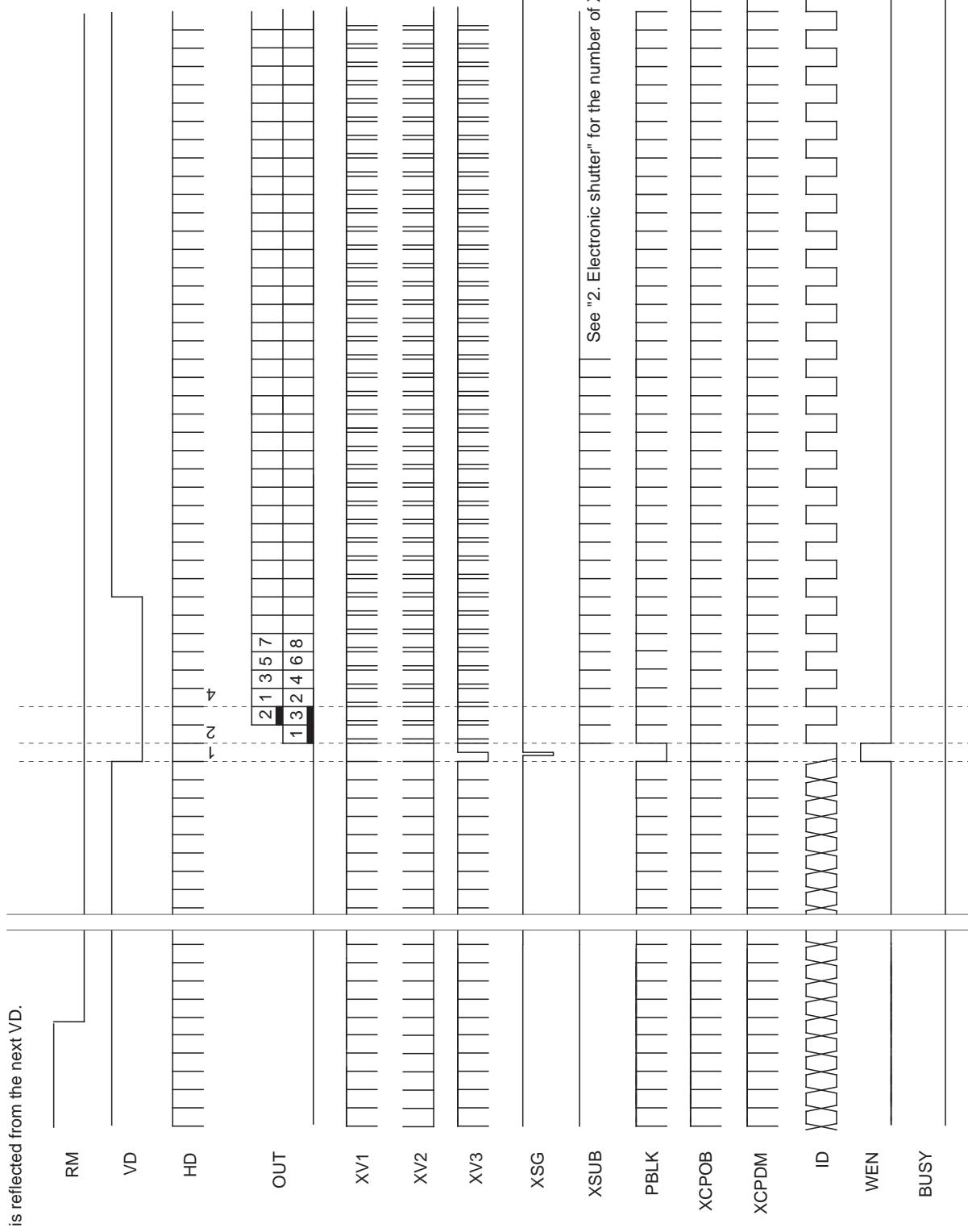
Chart-7   Switching from Double-speed Mode (RM = low) to Normal Mode (RM = high)

RM is reflected from the next VD.

See "2. Electronic shutter" for the number of XSUB pulses.

OUT: 1 2 3 1 2 3 4 5 6 7 8

9 3 1

RM
VD
HD
OUT
XV1
XV2
XV3
XSG
XSUB
PBLK
XCPOB
XCPDM
ID
WEN
BUSY
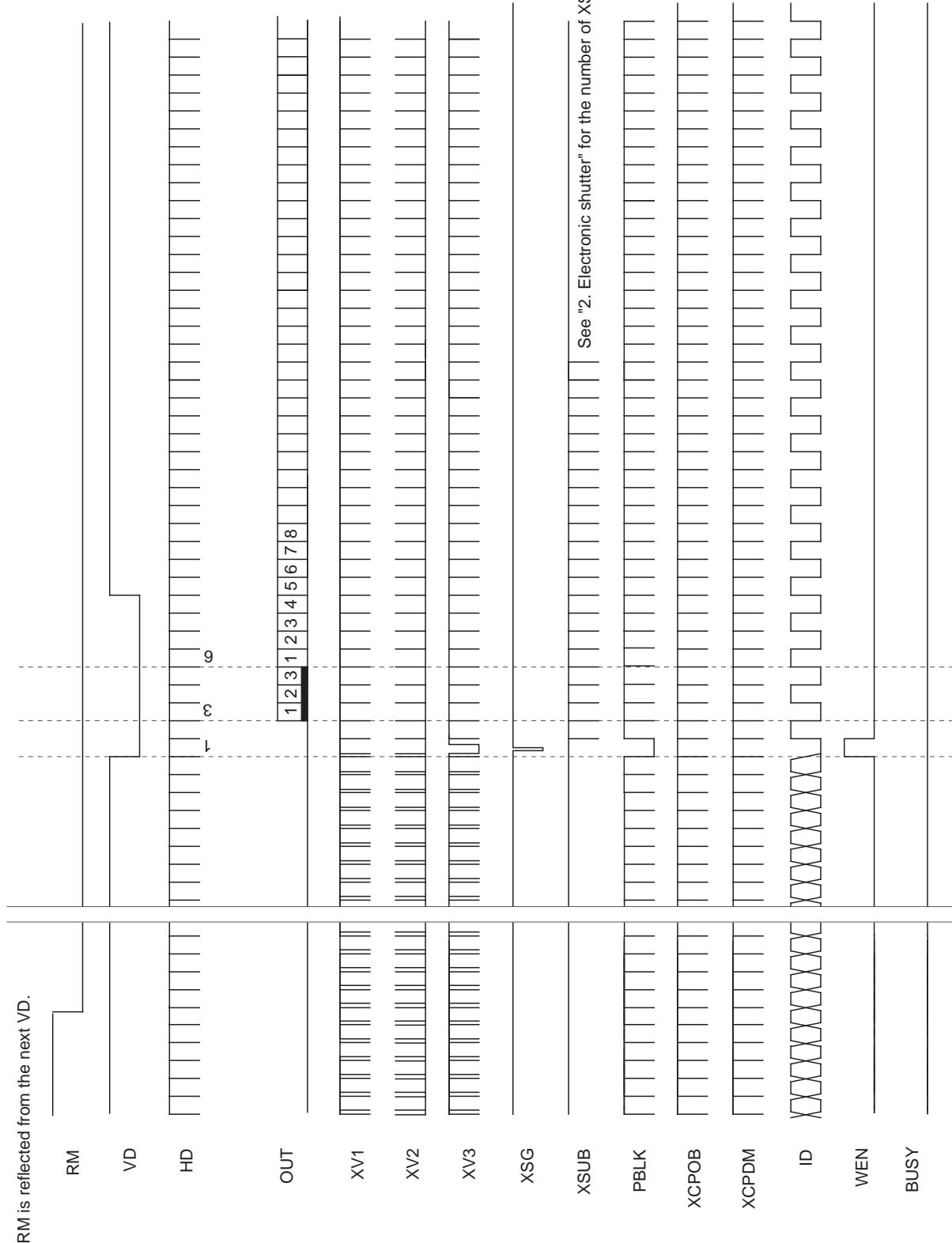
Chart-8 External Trigger Mode: High-speed electronic shutter, discharge, normal readout (FSE = high, SMDE = high, RM = high)

This VD is ignored.

See "2. Electronic shutter" for the XSG output position.

The number of XSUB pulses here conforms to normal operation.

TRIG
VD
HD
OUT
RG
XV1
XV2
XV3
XSG
XSUB
PBLK
XCPOB
XCPDM
ID
WEN
BUSY
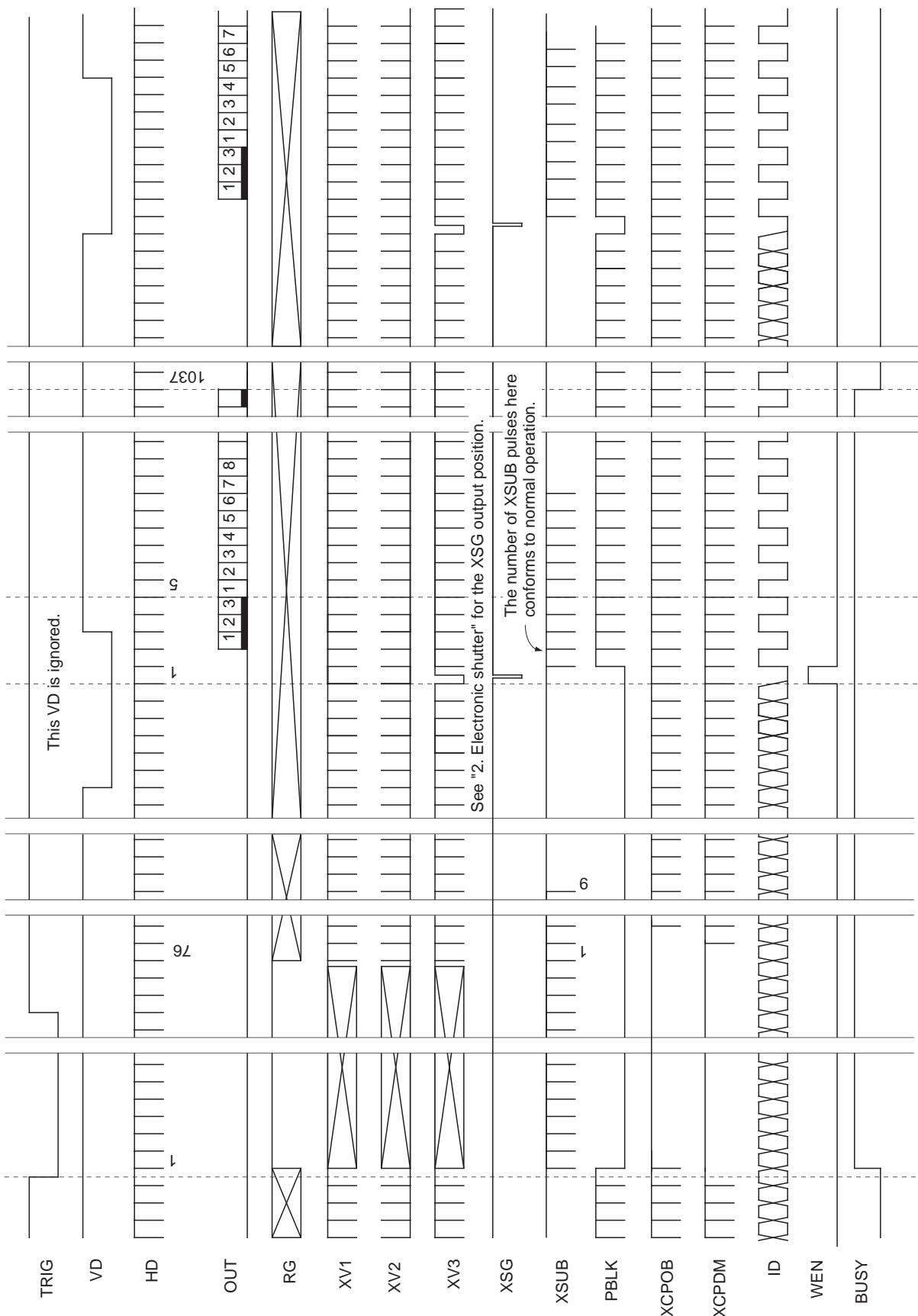
Chart-9 **External Trigger Mode: High-speed electronic shutter, discharge, double-speed mode (FSE = high, SMDE = high, RM = low)**

This VD is ignored.

See "2. Electronic shutter" for the XSG output position.

The number of XSUB pulses here conforms to normal operation.

Signal labels:

TRIG
VD
HD
OUT
RG
XV1
XV2
XV3
XSG
XSUB
PBLK
XCPOB
XCPDM
ID
WEN
BUSY
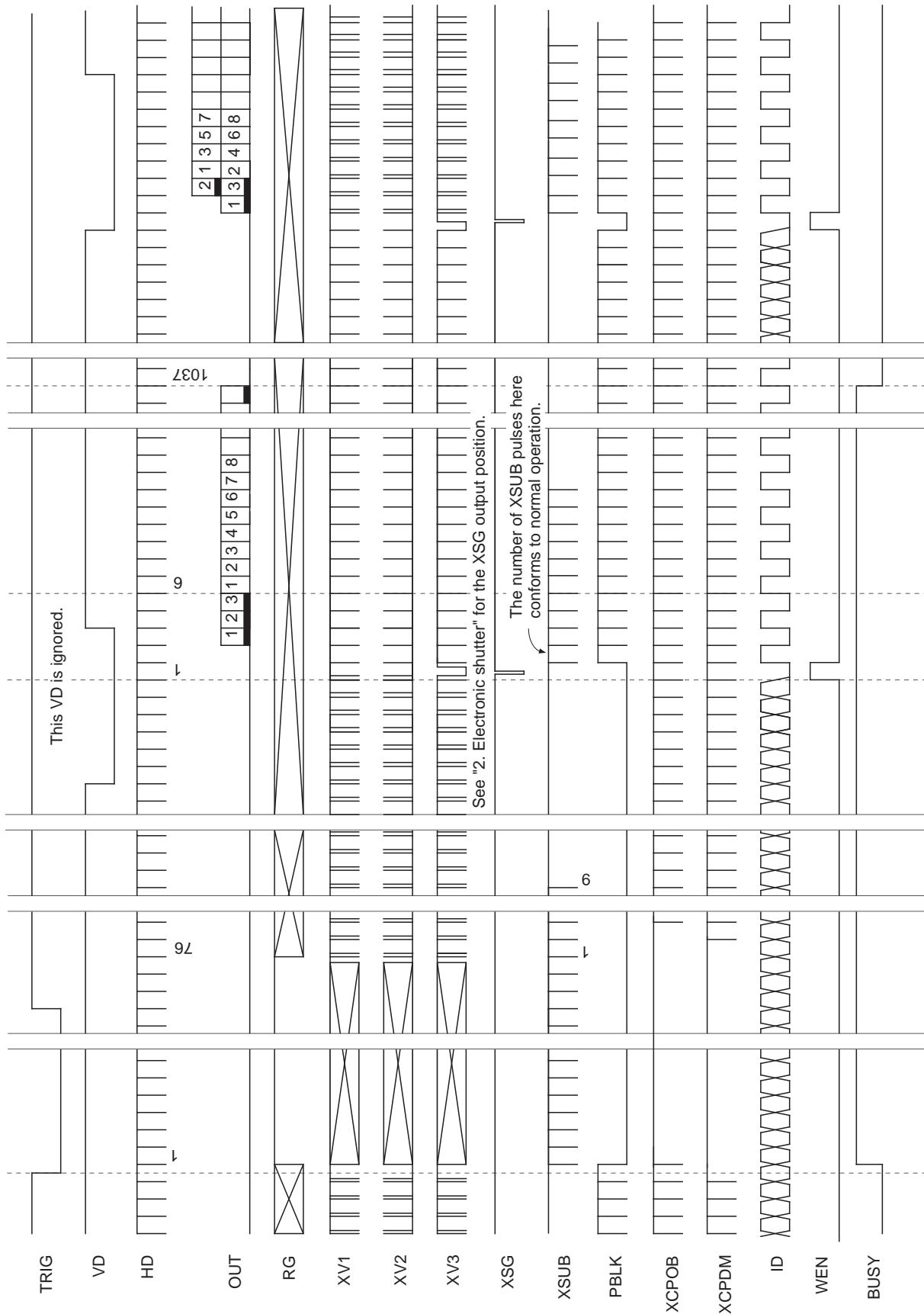
Chart-10   External Trigger Mode: High-speed electronic shutter, when discharge starts (FSE = high)
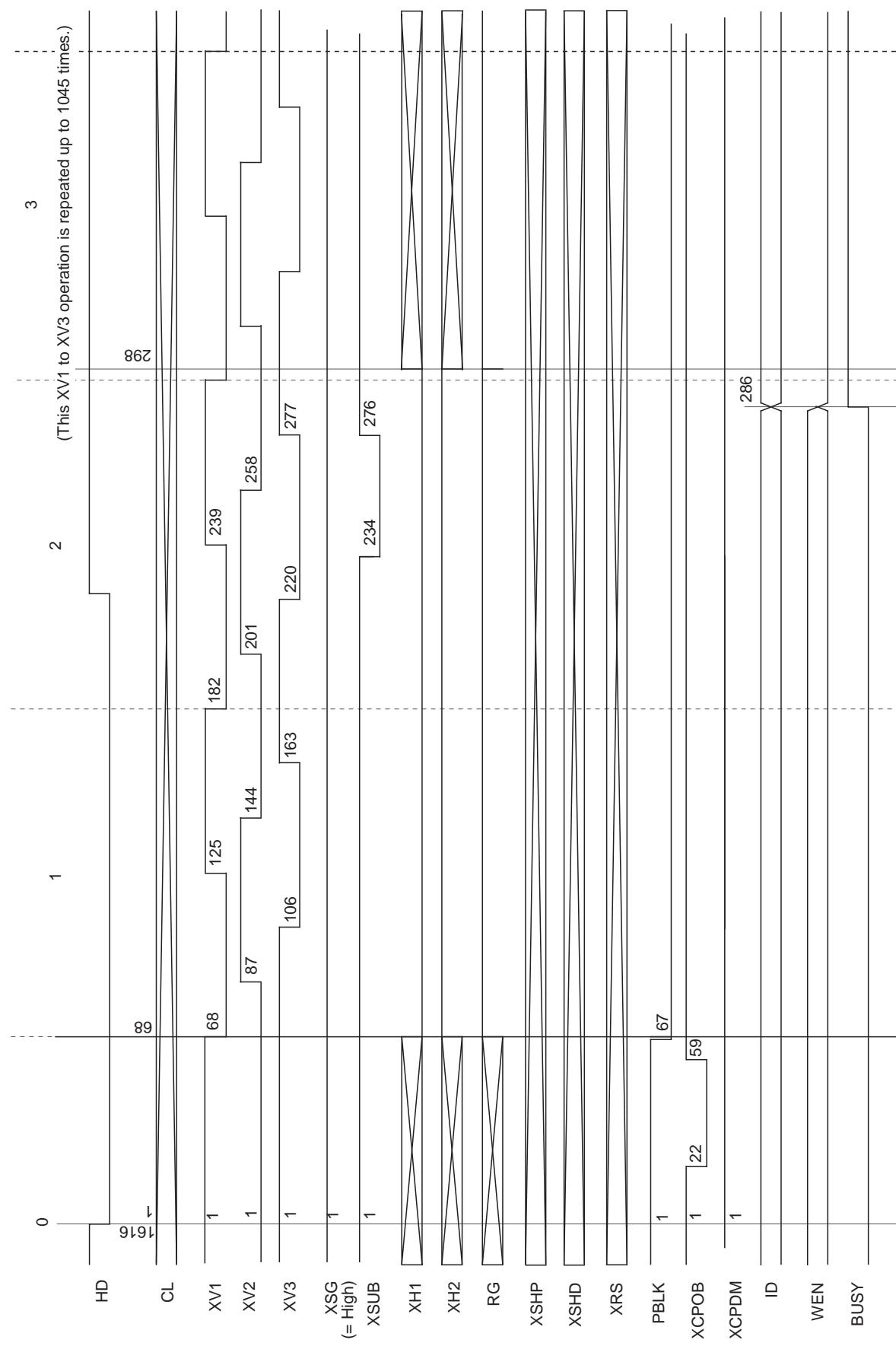
**Chart-11   External Trigger Mode: High-speed electronic shutter, no discharge (FSE = low, SMDE = high)**

TRIG

VD

This VD is ignored.

HD

OUT

RG

XV1

XV2

XV3

XSG

See "2. Electronic shutter" for the XSG output position.

XSUB

The number of XSUB pulses here conforms to normal operation.

PBLK

XCPOB

XCPDM

ID

WEN

BUSY
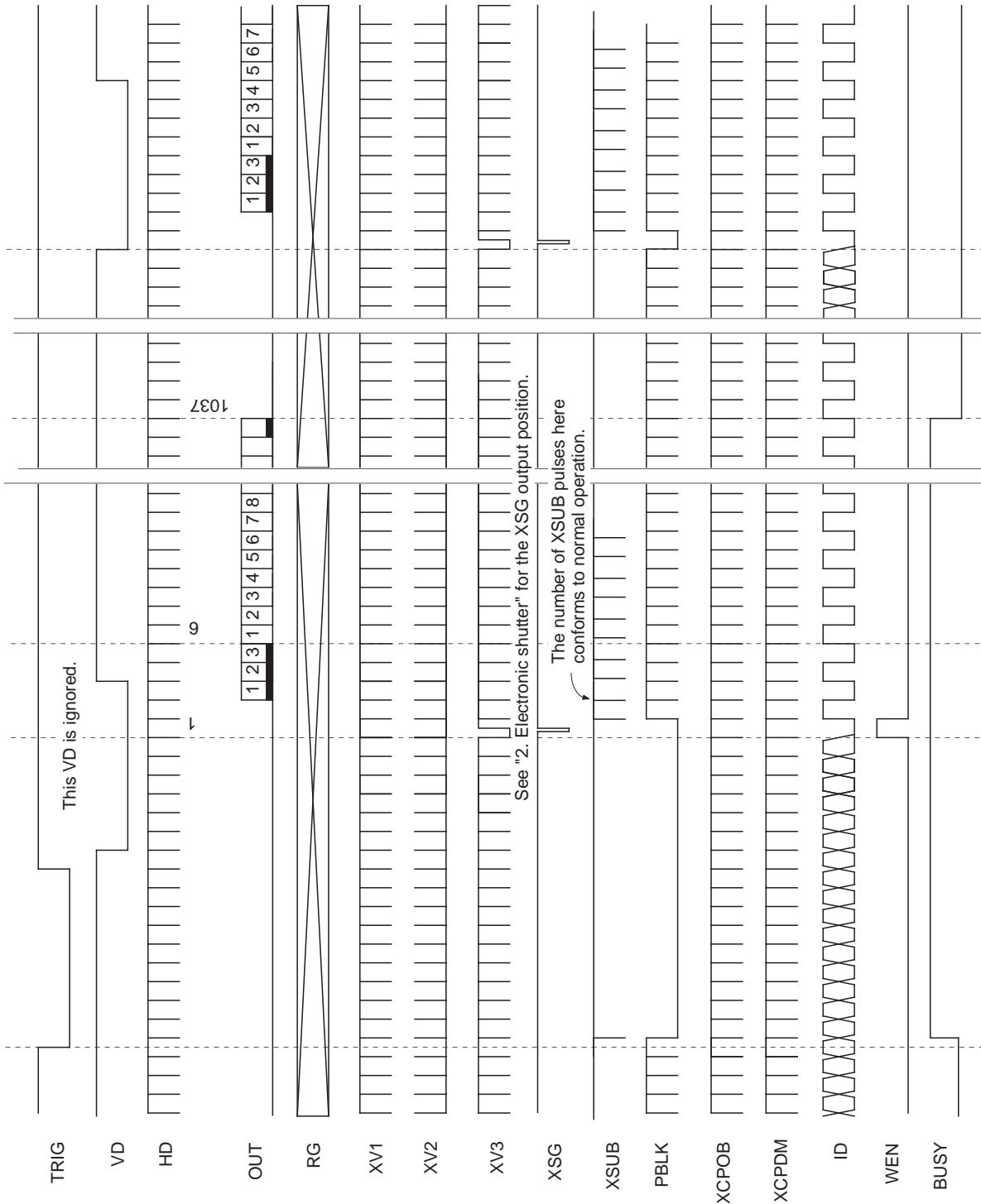
Chart-12 External Trigger Mode: High-speed electronic shutter, no discharge, double-speed mode (FSE = low, SMDE = high, RM = low)

TRIG

VD — This VD is ignored.

HD

OUT 1 2 3 1 2 3 4 5 6 7 8 6 1 1037 2 1 3 5 7 1 3 2 4 6 8

RG

XV1

XV2

XV3

XSG — See "2. Electronic shutter" for the XSG output position.

XSUB — The number of XSUB pulses here conforms to normal operation.

PBLK

XCPOB

XCPDM

ID

WEN

BUSY
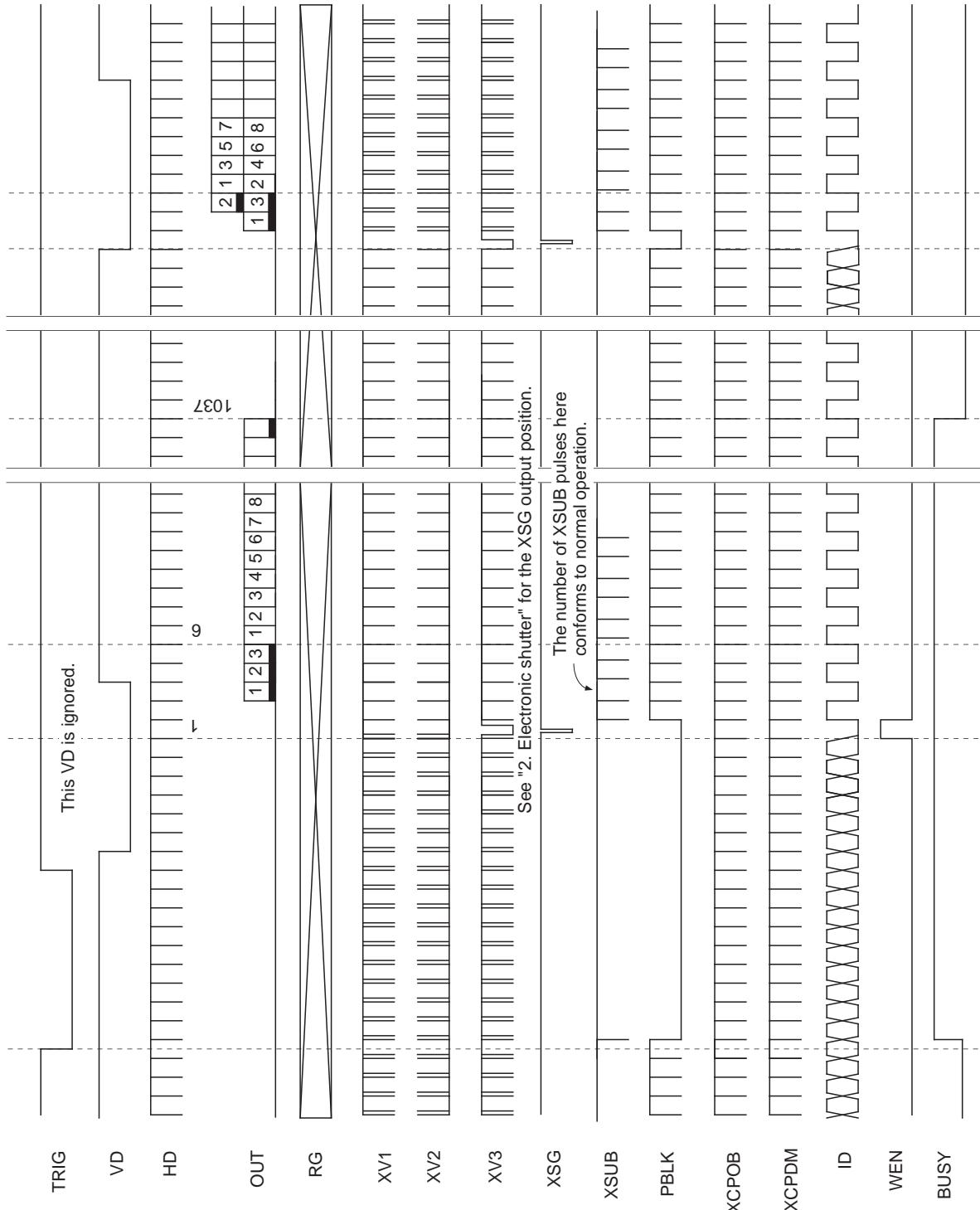
Chart-13   External Trigger Mode: Low-speed electronic shutter (SMDE = high, RM = high)

See "2. Electronic shutter" for the time from the XSG output after TRIG input until the next XSG output.
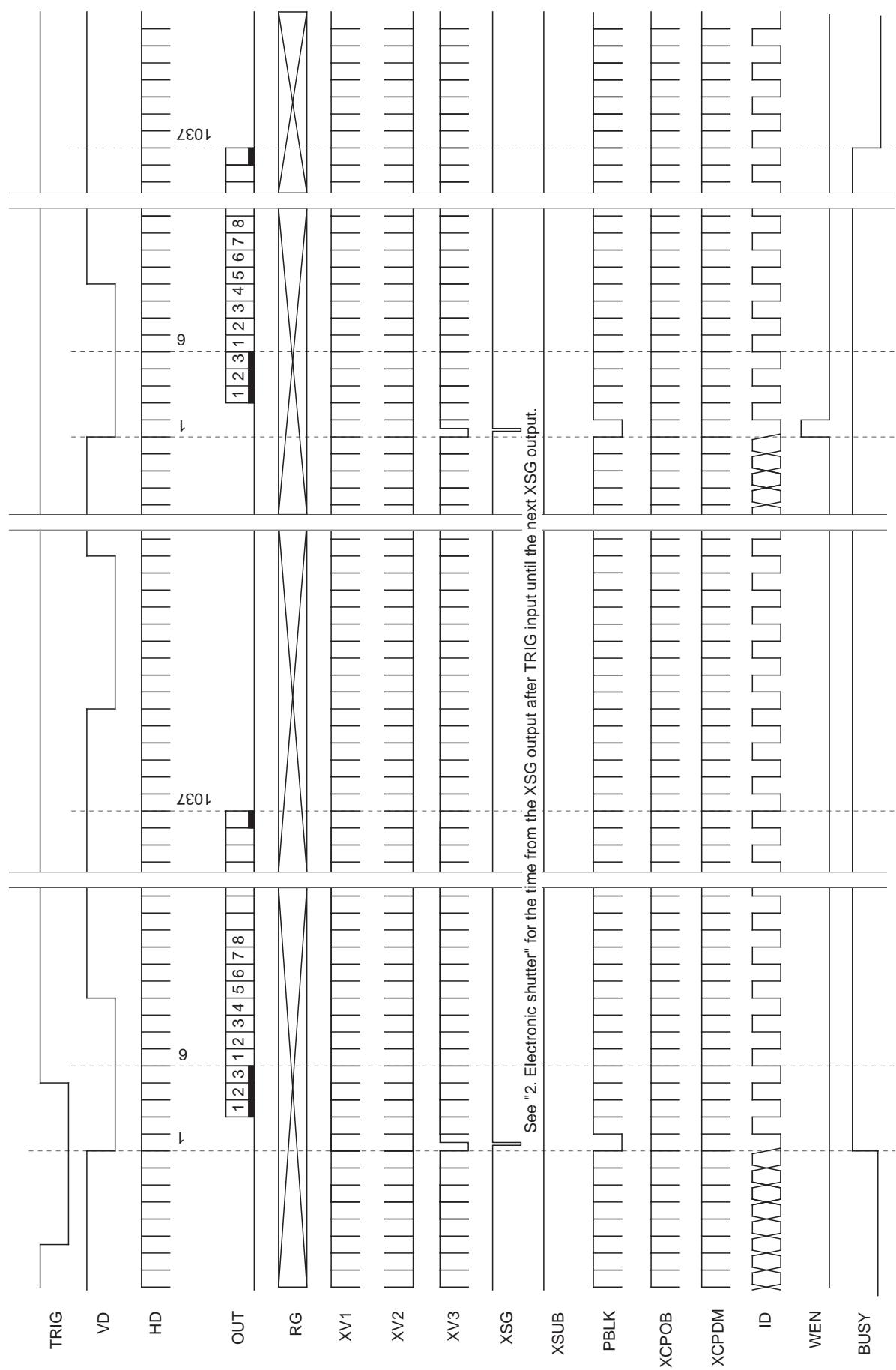
Chart-14   External Trigger Mode: Low-speed electronic shutter, double-speed mode (SMDE = high, RM = low)

See "2. Electronic shutter" for the time from the XSG output after TRIG input until the next XSG output.

TRIG
VD
HD
OUT
RG
XV1
XV2
XV3
XSG
XSUB
PBLK
XCPOB
XCPDM
ID
WEN
BUSY
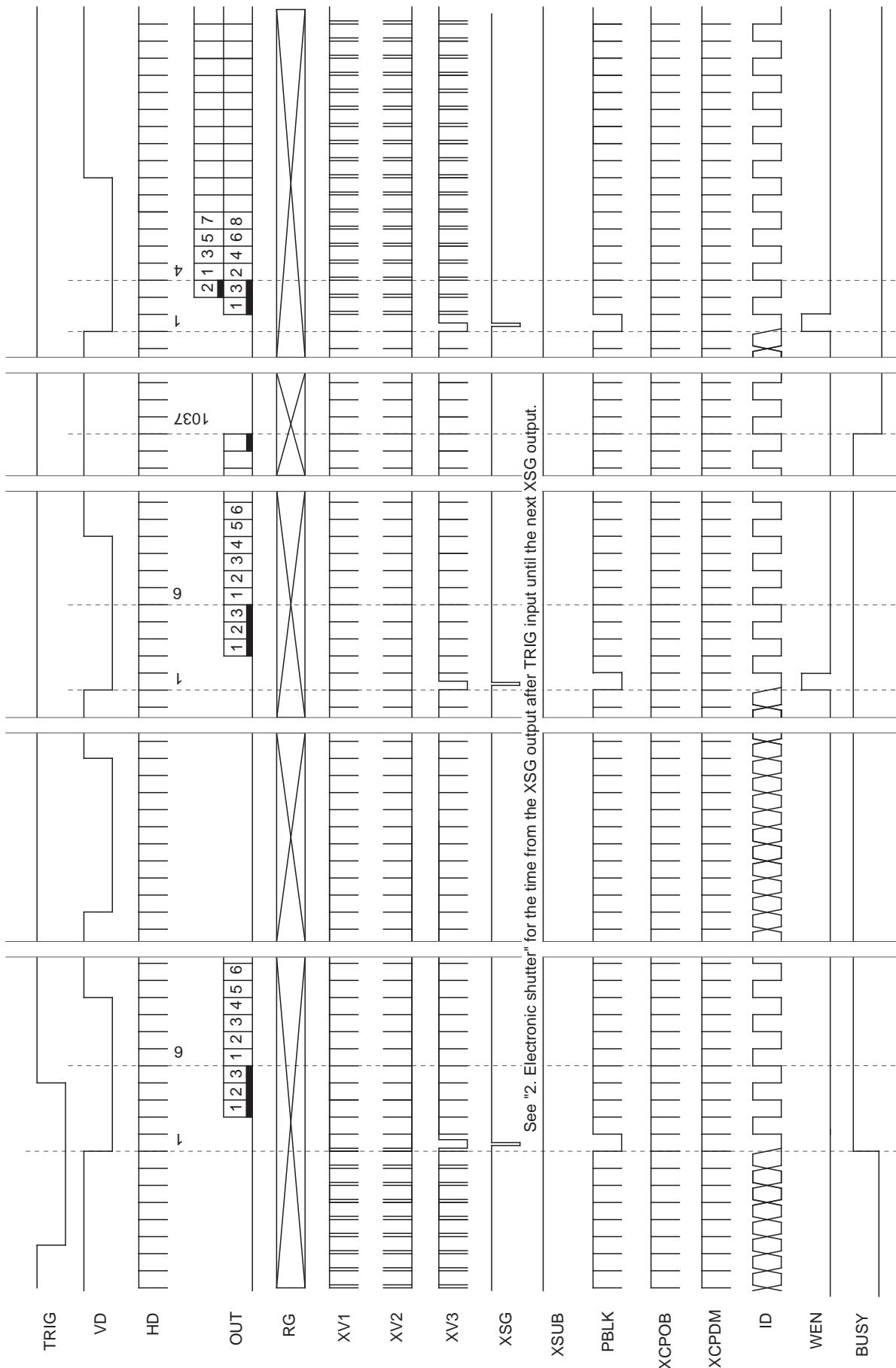
Chart-15   Example during ESG Input: Discharge, normal readout (FSE = high, RMDE = low, RM = high)
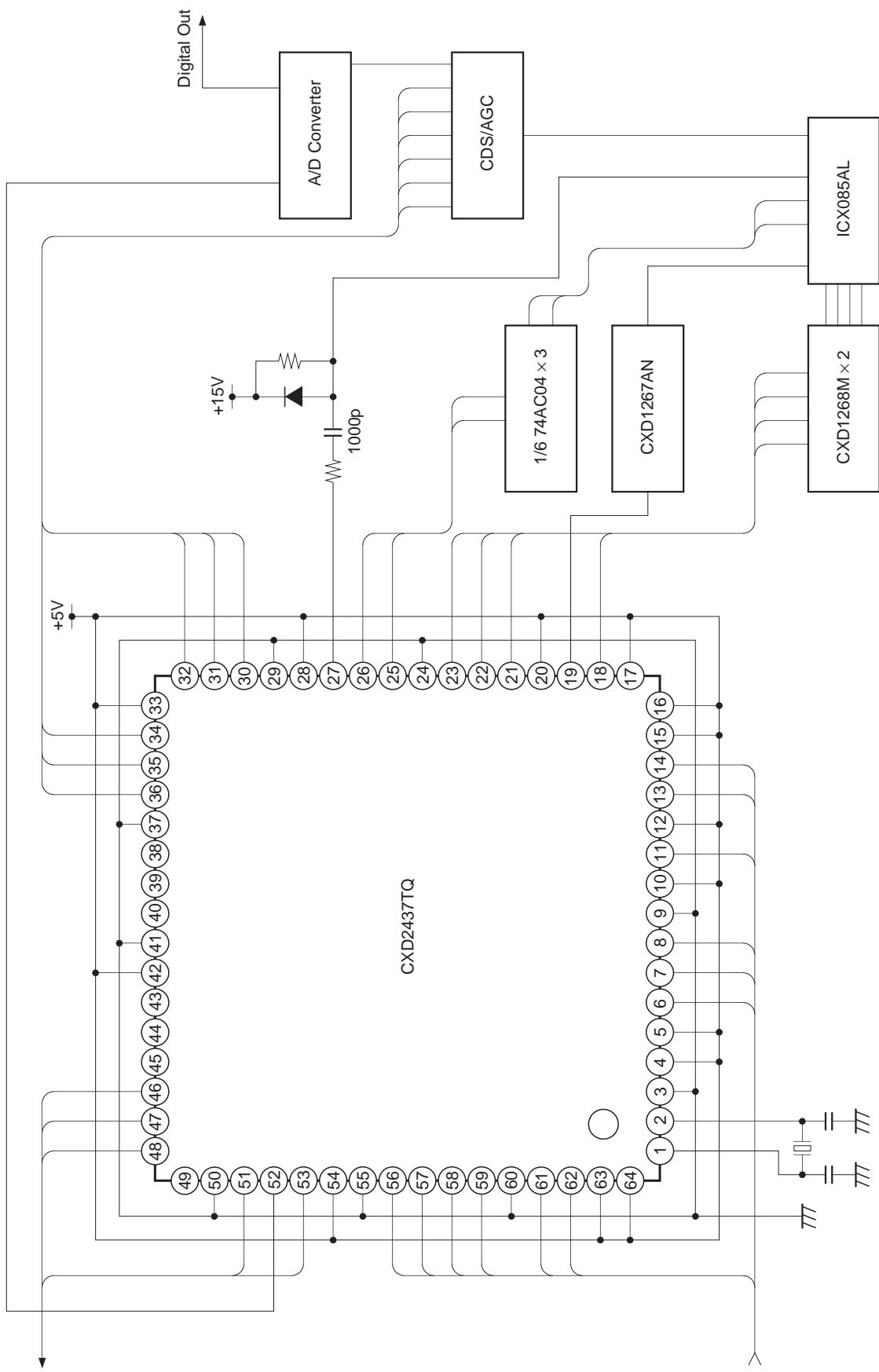
This VD is ignored.

The number of XSUB pulses here conforms to normal operation.

TRIG

ESG

VD

HD

OUT

RG

XV1

XV2

XV3

XSG

XSUB

PBLK

XCPOB

XCPDM

ID

WEN

BUSY

Application Circuit 1

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2
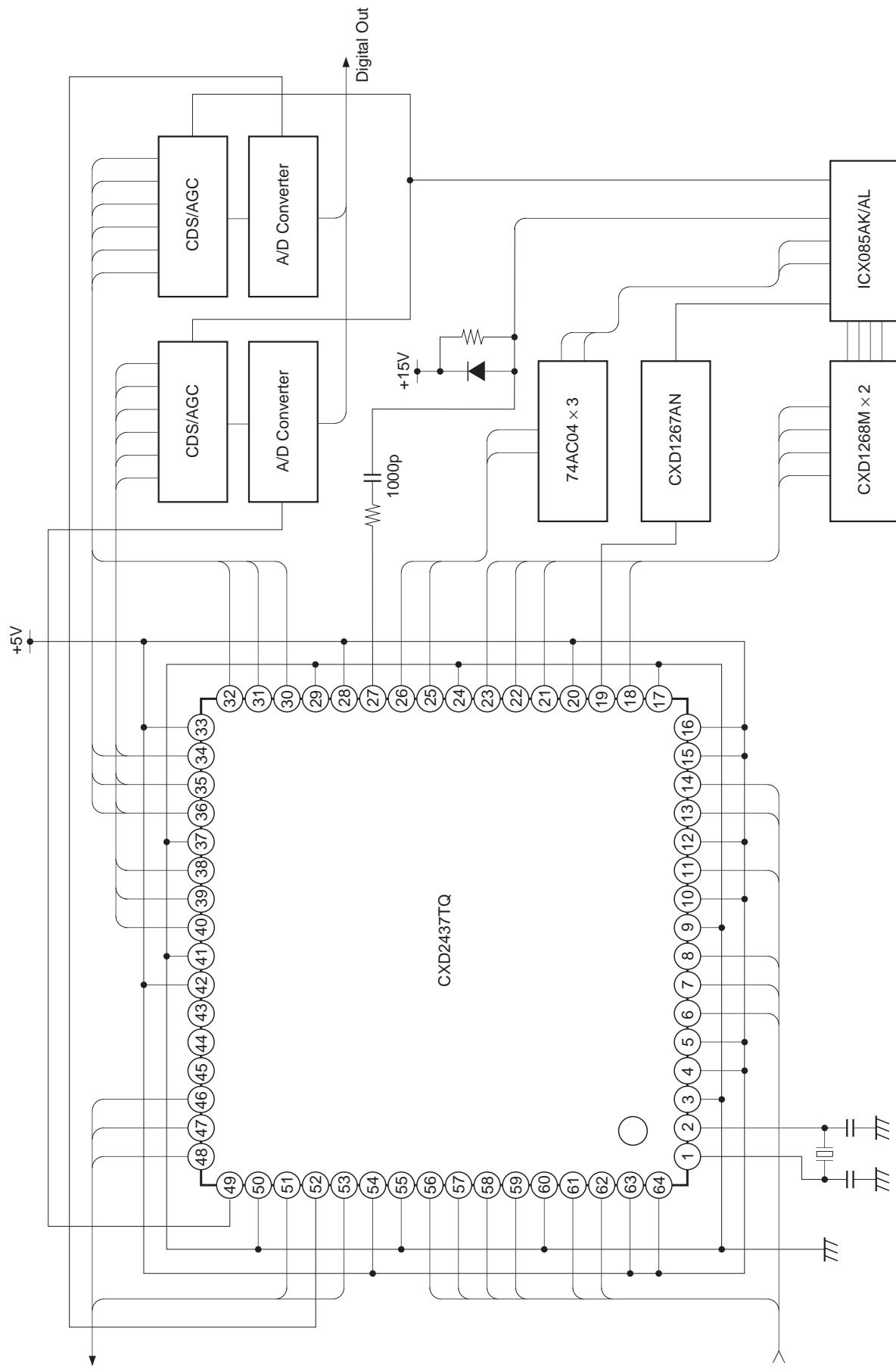
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

64PIN TQFP (PLASTIC)

☐ 12.0 ± 0.4
☐ 10.0 ± 0.2

48 33

49 32

64 17

1 16

0.5 0.2 ± 0.1 ⊕ 0.08 Ⓜ

1.27 MAX
1.0 ± 0.1

◠ 0.1

A

0.125 ± 0.05

0.1 ± 0.1

0.5 ± 0.2 1.0 ± 0.2

+ 7°
3° − 3°

DETAIL **A**
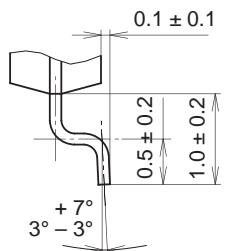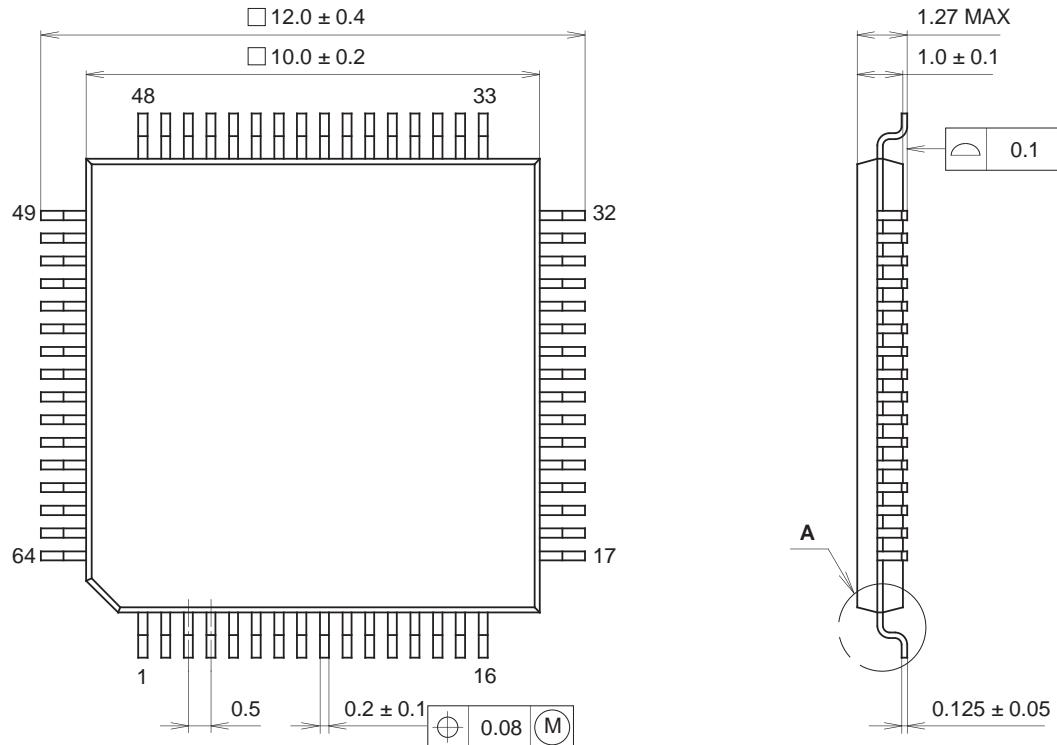
SONY CODE	TQFP-64P-L071
EIAJ CODE	TQFP064-P-1010-AN
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g