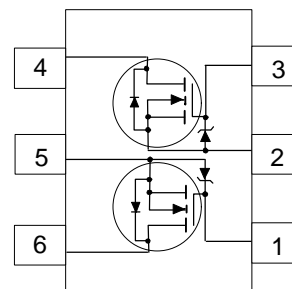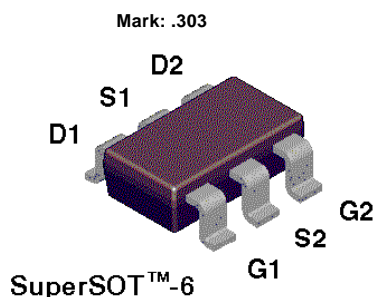**FAIRCHILD**
SEMICONDUCTOR ™

FDC6303N
Digital FET, Dual N-Channel

General Description

These dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors in load switching applications. Since bias resistors are not required this one N-Channel FET can replace several digital transistors with different bias resistors like the IMHxA series.

Features

- 25 V, 0.68 A continuous, 2 A Peak.
  $R_{DS(ON)} = 0.6\ \Omega$ @ $V_{GS} = 2.7$ V
  $R_{DS(ON)} = 0.45\ \Omega$ @ $V_{GS} = 4.5$ V.

- Very low level gate drive requirements allowing direct operation in 3V circuits. $V_{GS(th)} < 1.5$ V.

- Gate-Source Zener for ESD ruggedness.
  >6kV Human Body Model

- Replace multiple NPN digital transistors (IMHxA series) with one DMOS FET.

SOT-23	SuperSOT™-6	SuperSOT™-8	SO-8	SOT-223	SOIC-16

Mark: .303

D2
S1
D1
G2
S2
G1

SuperSOT™-6

4		3
5		2
6		1

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

| Symbol	Parameter		FDC6303N	Units
V_{DSS}	Drain-Source Voltage		25	V
V_{GSS}	Gate-Source Voltage		8	V
I_D	Drain Current - Continuous		0.68	A
	- Pulsed		2	
P_D	Maximum Power Dissipation	(Note 1a)	0.9	W
		(Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)		6.0	kV
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	140	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60	°C/W

## DMOS Electrical Characteristics (T_A = 25 $^{\circ}$C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA		25			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 $^{\circ}$C			26		mV /$^{\circ}$C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V				1	µA
			T_J = 55°C			10	µA
I_{GSS}	Gate - Body Leakage Current	V_{GS} = 8 V, V_{DS} = 0 V				100	nA
ON CHARACTERISTICS (Note 2)							
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp.Coefficient	I_D = 250 µA, Referenced to 25 $^{\circ}$C			-2.6		mV /$^{\circ}$C
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA		0.65	0.8	1.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 0.5 A			0.33	0.45	Ω
			T_J =125°C		0.52	0.8	
		V_{GS} = 2.7 V, I_D = 0.2 A			0.44	0.6	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 2.7 V, V_{DS} = 5 V		0.5			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 0.5 A			1.45		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz			50		pF
C_{oss}	Output Capacitance				28		pF
C_{rss}	Reverse Transfer Capacitance				9		pF
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 6 V, I_D = 0.5 A, V_{GS} = 4.5 V, R_{GEN} = 50 Ω			3	6	ns
t_r	Turn - On Rise Time				8.5	18	ns
$t_{D(off)}$	Turn - Off Delay Time				17	30	ns
t_f	Turn - Off Fall Time				13	25	ns
Q_g	Total Gate Charge	V_{DS} = 5 V, I_D = 0.5 A, V_{GS} = 4.5 V			1.64	2.3	nC
Q_{gs}	Gate-Source Charge				0.38		nC
Q_{gd}	Gate-Drain Charge				0.45		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Source Current					0.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.5 A (Note 2)			0.83	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.
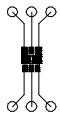
a. 140°C/W on a 0.125 in^2 pad of 2oz copper.
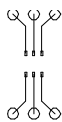
b. 180°C/W on a 0.005 in^2 of pad of 2oz copper.

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

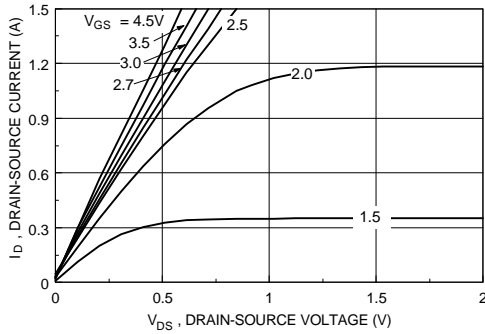## Typical Electrical Characteristics

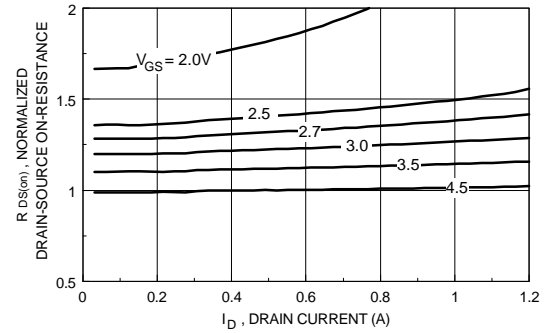Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with
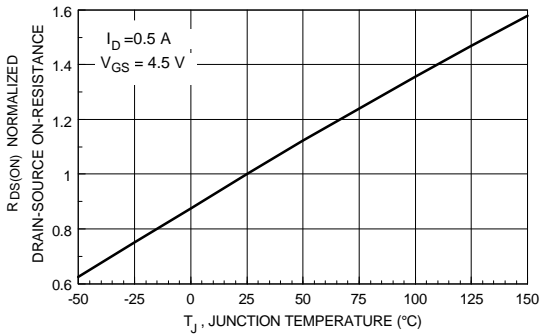Drain Current and Gate Voltage.

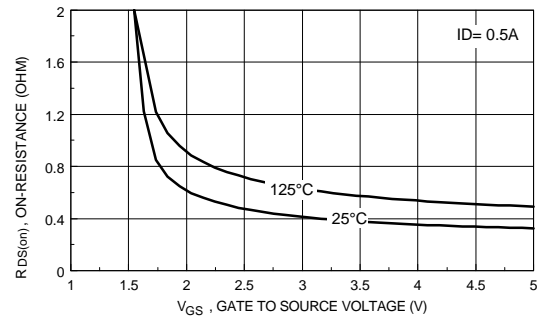Figure 3. On-Resistance Variation
with Temperature.

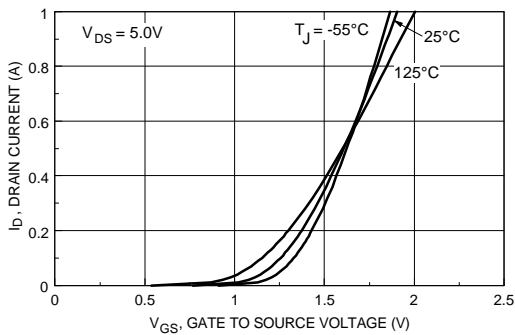Figure 4. On Resistance Variation with
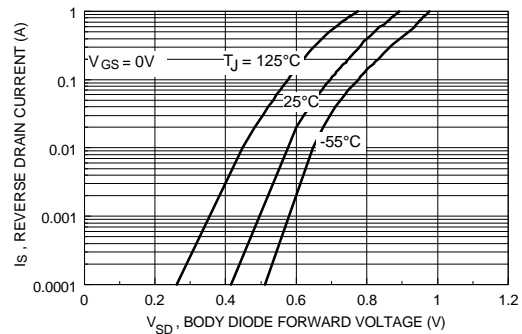Gate-To- Source Voltage.

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage
Variation with Source Current and
Temperature.

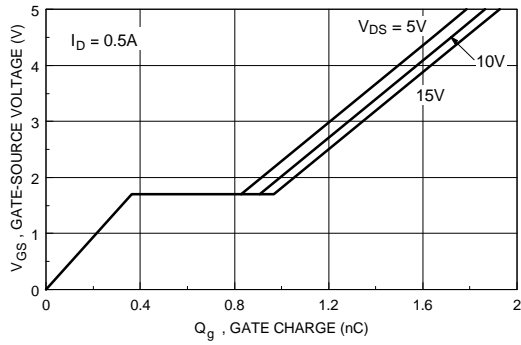# Typical Electrical And Thermal Characteristics
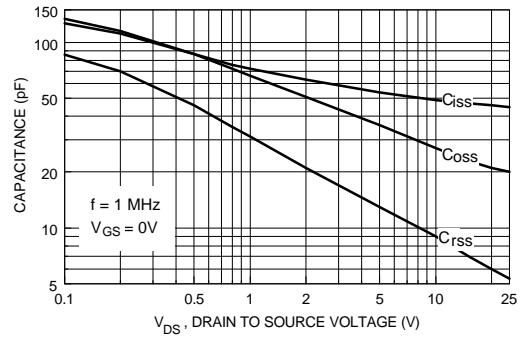
Figure 7. Gate Charge Characteristics.
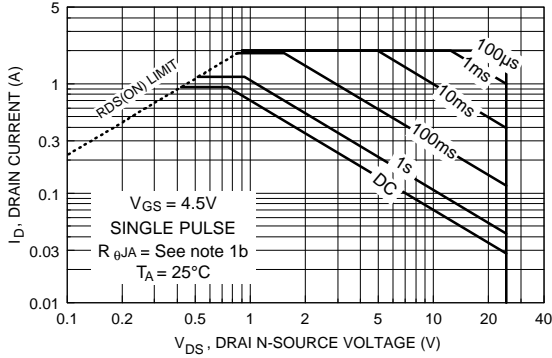
Figure 8. Capacitance Characteristics.

Figure 9. Maximum Safe Operating Area.
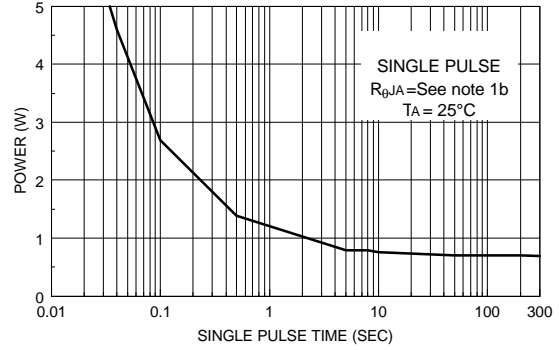
Figure 10. Single Pulse Maximum Power Dissipation.

$R_{\theta JA}(t) = r(t) * R_{\theta JA}$
$R_{\theta JA}$ = See Note 1b

$T_J \cdot T_A = P * R_{\theta JA}(t)$
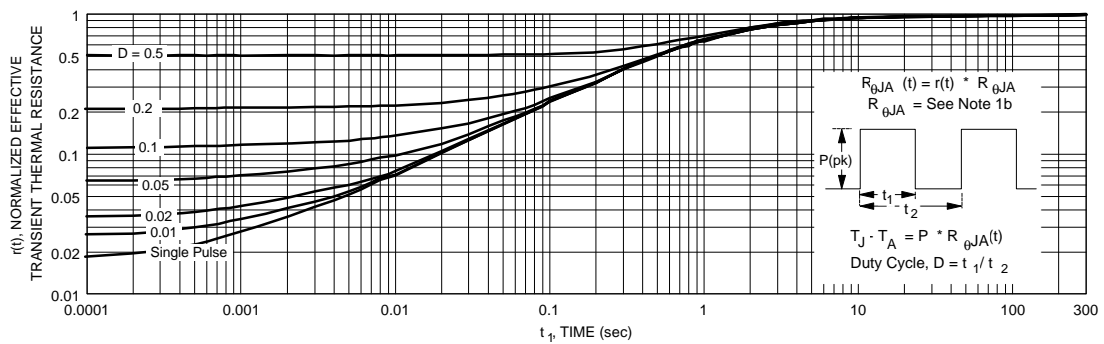Duty Cycle, $D = t_1 / t_2$

Figure 11. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.