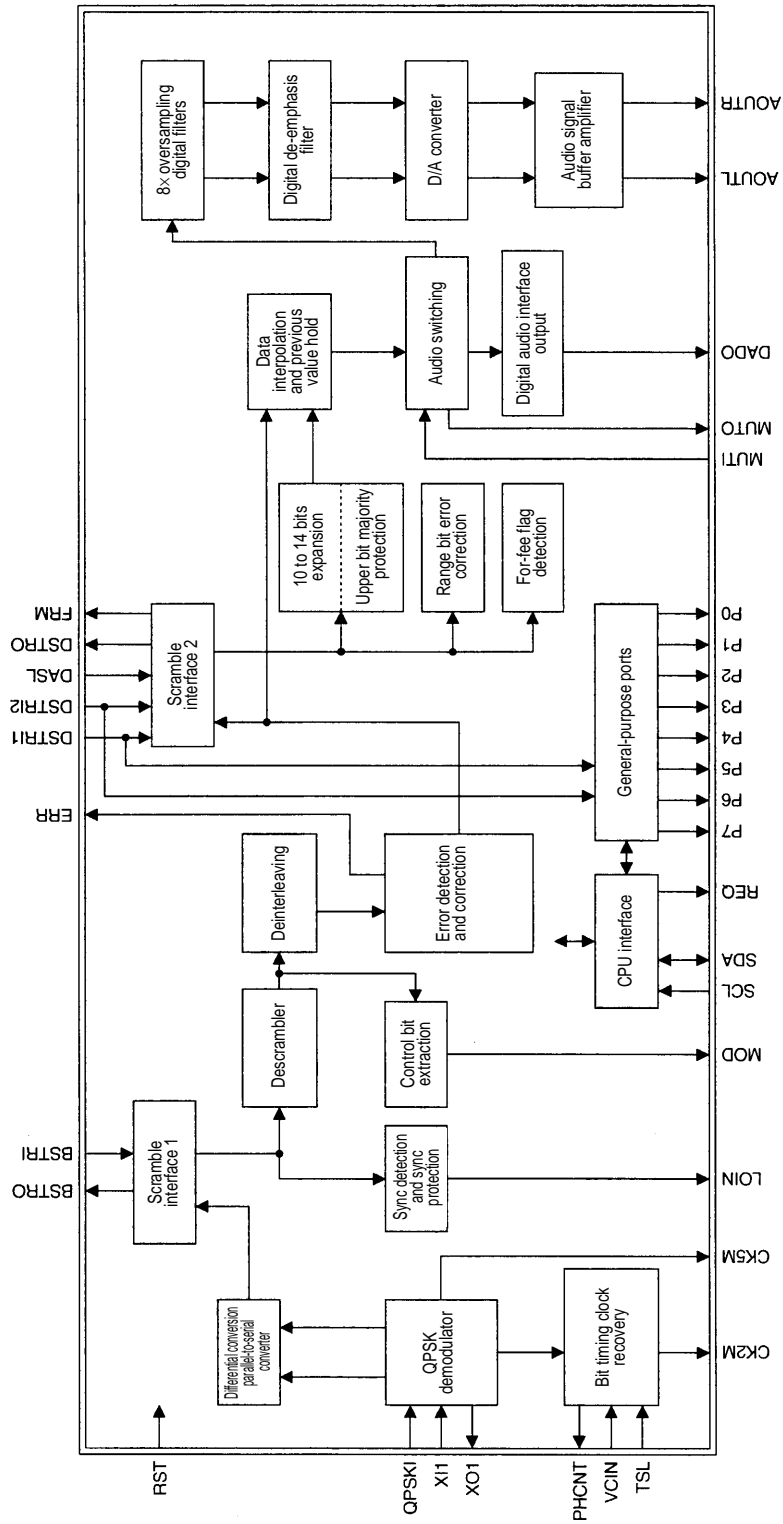


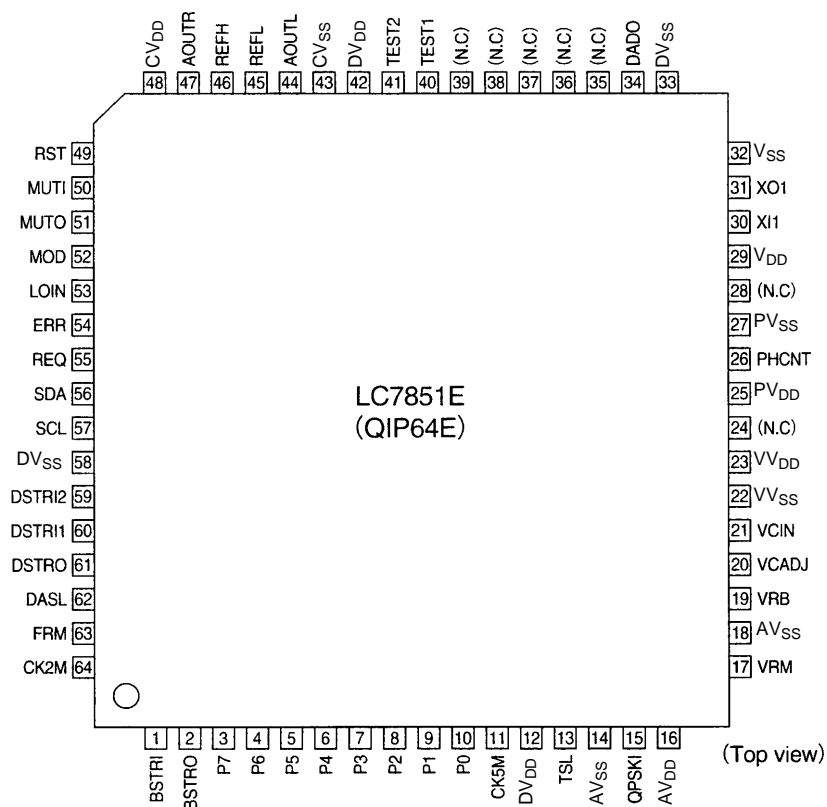
Block Diagram



A07436

LC7851E

Pin Assignment



A07437

Pin Functions

Pin No.	Pin	I/O	Function
1	BSTRI	I	Bit stream input
2	BSTRO	O	Bit stream output
3	P7	O	General-purpose output port
4	P6	O	General-purpose output port
5	P5	O	General-purpose output port
6	P4	O	General-purpose output port
7	P3	O	General-purpose output port
8	P2	O	General-purpose output port
9	P1	O	General-purpose output port
10	P0	O	General-purpose output port
11	CK5M	O	Filter adjustment clock output (5.7272 MHz)
12	DV _{DD}	I	Digital system power supply
13	TSL	I	Output control for the state when reset by the PHCNT pin (Low: high-impedance, high: 50% duty pulse output)
14	AV _{SS}	I	Internal A/D converter ground
15	QPSKI	I	QPSK modulated signal input
16	AV _{DD}	I	Internal A/D converter power supply
17	VRM	O	Internal A/D converter reference (center) output
18	AV _{SS}	I	Internal A/D converter ground
19	VRB	O	Internal A/D converter reference (low) output
20	VCADJ		Connection for internal VCO adjustment external resistor
21	VCIN	I	Internal VCO control input

Continued on next page.

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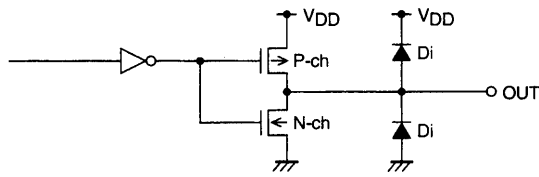
Pin No.	Pin	I/O	Function
22	VV _{SS}	I	Internal VCO ground
23	VV _{DD}	I	Internal VCO power supply
24	(N.C)		
25	PV _{DD}	I	Phase comparator power supply
26	PHCNT	O	Phase comparator output
27	PV _{SS}	I	Phase comparator ground
28	(N.C)		
29	V _{DD}	I	Oscillator circuit power supply
30	XI1	I	Crystal oscillator (22.909088 MHz) input
31	XO1	O	Crystal oscillator (22.909088 MHz) output
32	V _{SS}	I	Oscillator circuit ground
33	DV _{SS}	I	Digital system ground
34	DADO	O	Digital audio interface output
35	(N.C)		
36	(N.C)		
37	(N.C)		
38	(N.C)		
39	(N.C)		
40	TEST1	I	Test pin
41	TEST2	I	Test pin
42	DV _{DD}	I	Digital system power supply
43	CV _{SS}	I	Internal D/A converter ground
44	AOUTL	O	Left channel audio data output
45	REFL	O	Internal D/A converter reference voltage: low
46	REFH	O	Internal D/A converter reference voltage: high
47	AOUTR	O	Right channel audio data output
48	CV _{DD}	I	Internal D/A converter power supply
49	RST	I	Reset input
50	MUTI	I	Forced muting input
51	MUTO	O	Mute detection output (When muting detected: high)
52	MOD	O	Audio mode detection output (A mode: low, B mode: high)
53	LOIN	O	Frame synchronization detection output (When synchronized: low)
54	ERR	O	Error detection output (Error detected: high)
55	REQ	O	Host CPU readout request signal
56	SDA	I/O	I ² C bus data I/O
57	SCL	I	I ² C bus clock input
58	DV _{SS}	I	Digital system ground
59	DSTRI2	I	Data stream input 2/general-purpose I/O port
60	DSTRI1	I	Data stream input 1/general-purpose I/O port
61	DSTRO	O	Data stream output (post-error correction data)
62	DASL	I	Descrambler interface switching
63	FRM	O	Frame synchronization signal
64	CK2M	O	Bit stream clock (2.048 MHz)

Caution: All NC pins must be left open.

LC7851E

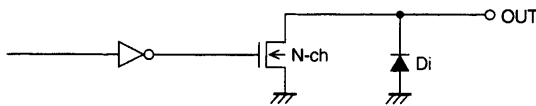
Pin Input and Output Circuit Diagrams

- Output pins (Output pins other than P0 to P7, SDA, PHCNT, CK5M, VRM, VRB, REFH, REFL, AOUTR, and AOUTL)



A07438

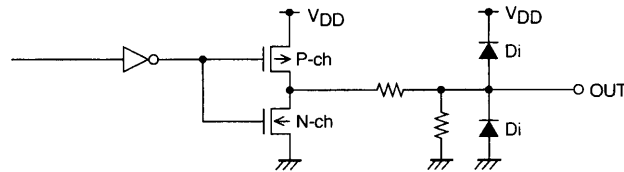
- Output pins: P0 to P7



These are n-channel open drain outputs.

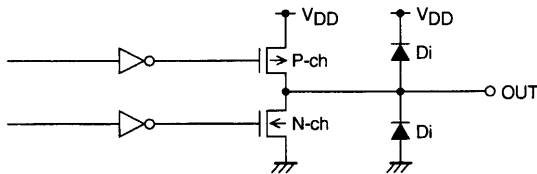
A07439

- Output pin: CK5M



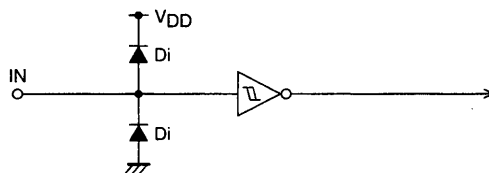
A07440

- Output pin: PHCNT



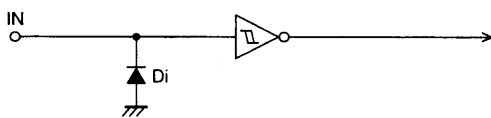
A07441

- Input pins (Input pins other than QPSKI, SCL, SDA, DSTR11, DSTR12, and VCIN)



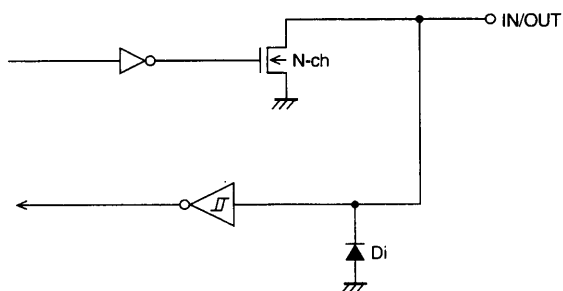
A07442

- Input pins: SCL, DSTR11, and DSTR12



A07443

- I/O pin: SDA



A07444

LC7851E

Specifications

Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.3 to +7.0	V
Input voltage	V _{I1}	Pins other than SCL and SDA	-0.3 to V _{DD} +0.3	V
	V _{I2}	SCL and SDA	-0.3 to +5.3	V
Output voltage	V _O		-0.3 to V _{DD} +0.3	V
Allowable power dissipation	Pd max	Ta = -20 to +75°C	360	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V _{DD}		4.5	5.0	5.5	V
Input high-level voltage	V _{IH}		0.75 V _{DD}		V _{DD}	V
Input low-level voltage	V _{IL}		0		0.25 V _{DD}	V
QPSKI input voltage	V _{QPSKI}		0.7	0.9	1.1	V

DC Characteristics at Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5 V, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I _{DD}			68	98	mA
Output high-level current	I _{OH1}	V _{OH} = V _{DD} - 0.4 V ; V _{OH} = V _{DD} - 0.4 V, CMOS output pins:PHCNT, LOIN, MOD, DSTRO, FRM, ERR, CK2M, BSTRO, MUTO, DADO, REQ, SYCKO	1.0			mA
	I _{OH2}	V _{OH} = V _{CK5MH} - 25 mV, CK5M	-350		-100	μA
Output low-level current 1	I _{OL1}	V _{OL} = 0.4 V ; CMOS output pins: PHCNT, LOIN, MOD, DSTRO, FRM, ERR, CK2M, BSTRO, MUTO, DADO, REQ, SYCKO	1.0			mA
	I _{OL2}	V _{OL} = 0.4 V, open drain output Pin 1: P0 to P7	1.0			mA
	I _{OL3}	V _{OL} = 0.4 V, open drain output Pin 2: SDA	4.0			mA
	I _{OL4}	V _{OL} = V _{CK5ML} + 25 mV, CK5M	100		350	μA
Output amplitude level	V _{CK5M}	I _{OH} = 30 μA, CK5M	236	295	354	mV
Input high-level current	I _{IH}	V _I = V _{DD} , Schmitt inputs: TSL, RST, TEST1, TEST2, BSTRI, DSTRI1, DSTRI2, DASL, MUTI, SCL, SDA, P0 to P7			10	μA
Input low-level current	I _{IL}	V _I = V _{SS} , Schmitt inputs: TSL, RST, TEST1, TEST2, BSTRI, DSTRI1, DSTRI2, DASL, MUTI, SCL, SDA, P0 to P7	-10			μA
Output load resistance	R _L	AOUTL and AOUTR	5.0			kΩ

D/A Converter Characteristics at Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5 V, GND = 0 V

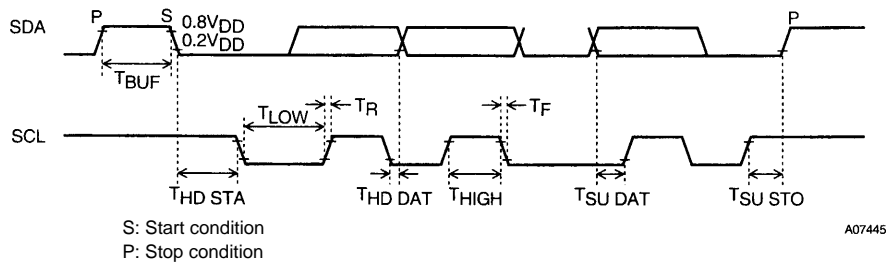
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Resolution	RES	1 kHz 0 dB		16		Bits
Total harmonic distortion	THD1	1 kHz A mode, FS - 18 dB *		0.08		%
	THD2	1 kHz B mode, FS - 18 dB *		0.05		%
Signal-to-noise ratio	S/N	1 kHz 0 dB *		105		dB
Crosstalk	C. T	1 kHz 0 dB *		95		dB
Full scale output voltage	VFS		2.8	3.0	3.2	Vp-p

Note: *Values when measured in the Sanyo evaluation board and with a QPSK modulated signal (1 kHz sine wave) input.

LC7851E

I²C Bus Interface at Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5 V, GND = 0 V

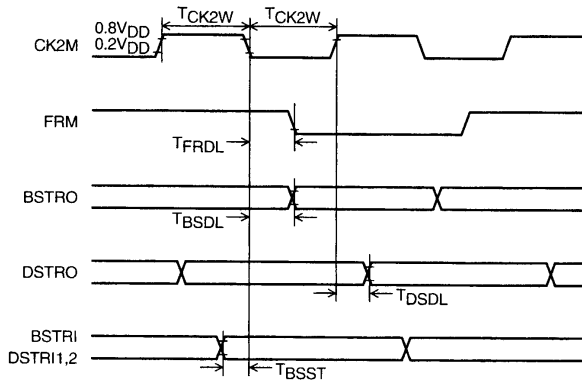
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SCL frequency	f _{SCL}				100	kHz
Bus release time	T _{BUF}		4.7			μs
Start hold time	T _{HD STA}		4.0			μs
SCL low time	T _{LOW}		4.7			μs
SCL high time	T _{HIGH}		4.0			μs
Data hold time	T _{HD DAT}		0			ns
Data setup time	T _{SU DAT}		250			ns
Rise time	T _R				1000	ns
Fall time	T _F				300	ns
Stop setup time	T _{SU STO}		4.0			μs



A07445

Descrambler Interface at Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5 V, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock pulse width	T _{CK2M}		244			ns
BSTRO pin output delay time	T _{BSDL}				15	ns
DSTRO pin output delay time	T _{DSDL}				15	ns
BSTRI and DSTRI1 two-pin input setup time	T _{BSST}		10			ns

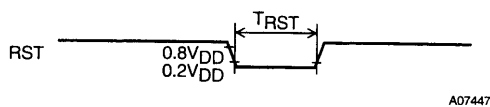


A07446

Reset Timing at Power on at Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5 V, GND = 0 V

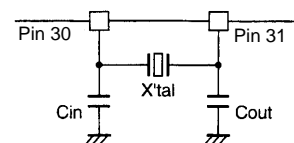
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reset time	T _{RST}	TSL pin high; The LC7851E must be used with the TSL pin (pin 13) high.	200			ms

The LC7851E must be reset with the following timing when power is first applied.



A07447

Pin I/O Circuit



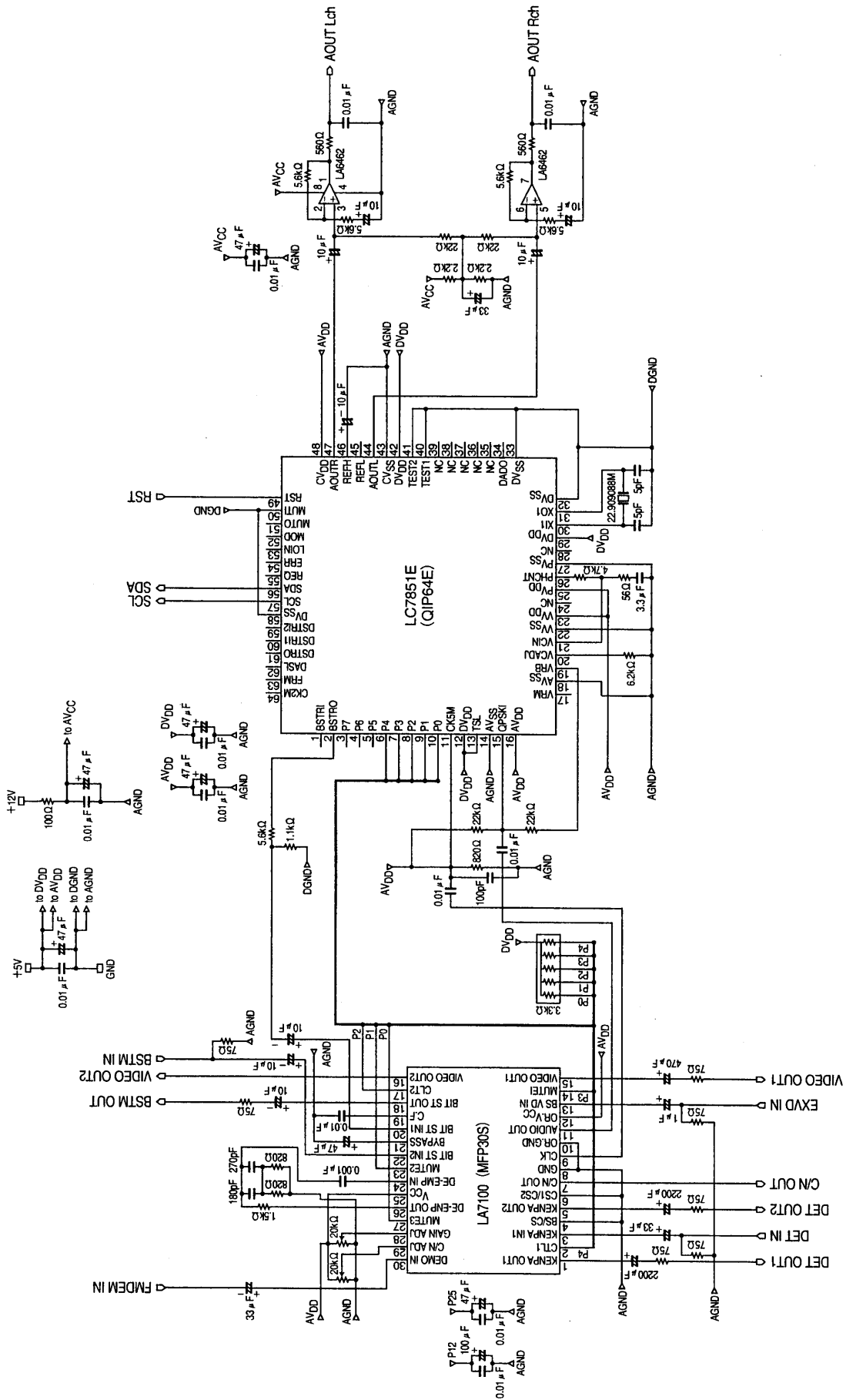
A07448

Recommended Crystal Oscillator Constants

Supplier	Oscillator element	Cin/Cout
Citizen Watch Co., Ltd.	CSA-309 (22.909088 MHz)	5pF (Cin = Cout)

LC7851E

Application Circuit Diagram



A07449

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