

# LH521028A

CMOS 64K × 18 Static RAM

## FEATURES

- Fast Access Times: 15/17/20/25/35 ns
- Wide Word (18-Bits) for:
  - Improved Performance
  - Reduced Component Count
  - Nine-bit Byte for Parity
- Transparent Address Latch
- Reduced Loading on Address Bus
- Low-Power Stand-by Mode when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- 2 V Data Retention
- JEDEC Standard Pinout
- Package: 52-Pin PLCC

## FUNCTIONAL DESCRIPTION

The LH521028 is a high-speed 1,179,648-bit CMOS SRAM organized as 64K × 18. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells. The LH521028 is available in a compact 52-Pin PLCC, which along with the six pairs of supply terminals, provide for reliable operation.

The control signals include Write Enable ( $\overline{W}$ ), Chip Enable ( $\overline{E}$ ), High and Low Byte Select ( $\overline{S}_L$  and  $\overline{S}_H$ ), Output Enable ( $\overline{G}$ ) and Address Latch Enable (ALE). The wide word provides for reduced component count, improved density, reduced Address bus loading and improved performance. The wide word also allows for byte-parity with no additional RAM required.

This RAM is fully static in operation. The Chip Enable ( $\overline{E}$ ) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). The Byte-select controls,  $\overline{S}_H$

and  $\overline{S}_L$ , are also used to enable or disable Read and Write operations on the high and the low bytes. The Address Latches are transparent when ALE is HIGH (for applications not requiring a latch), and are latched when ALE is LOW. The Address Latches and the wide word help to eliminate the need for external Address bus buffers and/or latches.

Write cycles occur when Chip Enable ( $\overline{E}$ ),  $\overline{S}_H$  and/or  $\overline{S}_L$ , and Write Enable ( $\overline{W}$ ) are LOW. The Byte-select signals can be used for Byte-write operations by disabling the other byte during the Write operation. Data is transferred from the DQ pins to the memory location specified by the 16 address lines. The proper use of the Output Enable control ( $\overline{G}$ ) can prevent bus contention.

When  $\overline{E}$  and either  $\overline{S}_H$  or  $\overline{S}_L$  are LOW and  $\overline{W}$  is HIGH, a static Read will occur at the memory location specified by the address lines.  $\overline{G}$  must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address with ALE HIGH.

## PIN CONNECTIONS

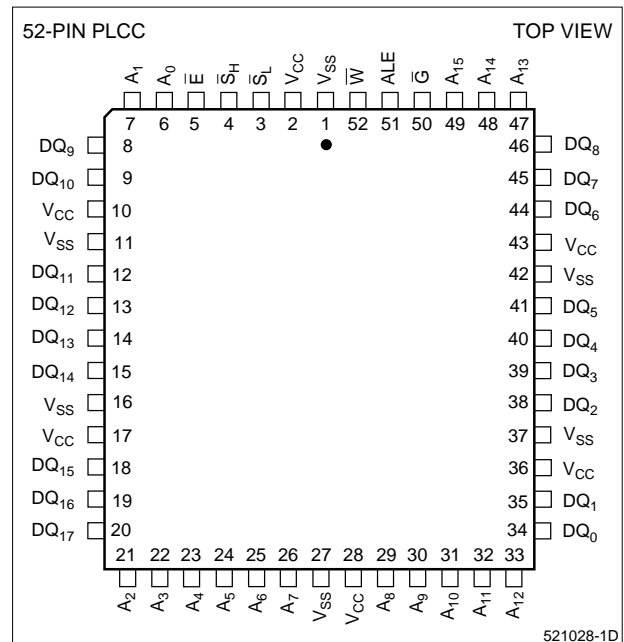
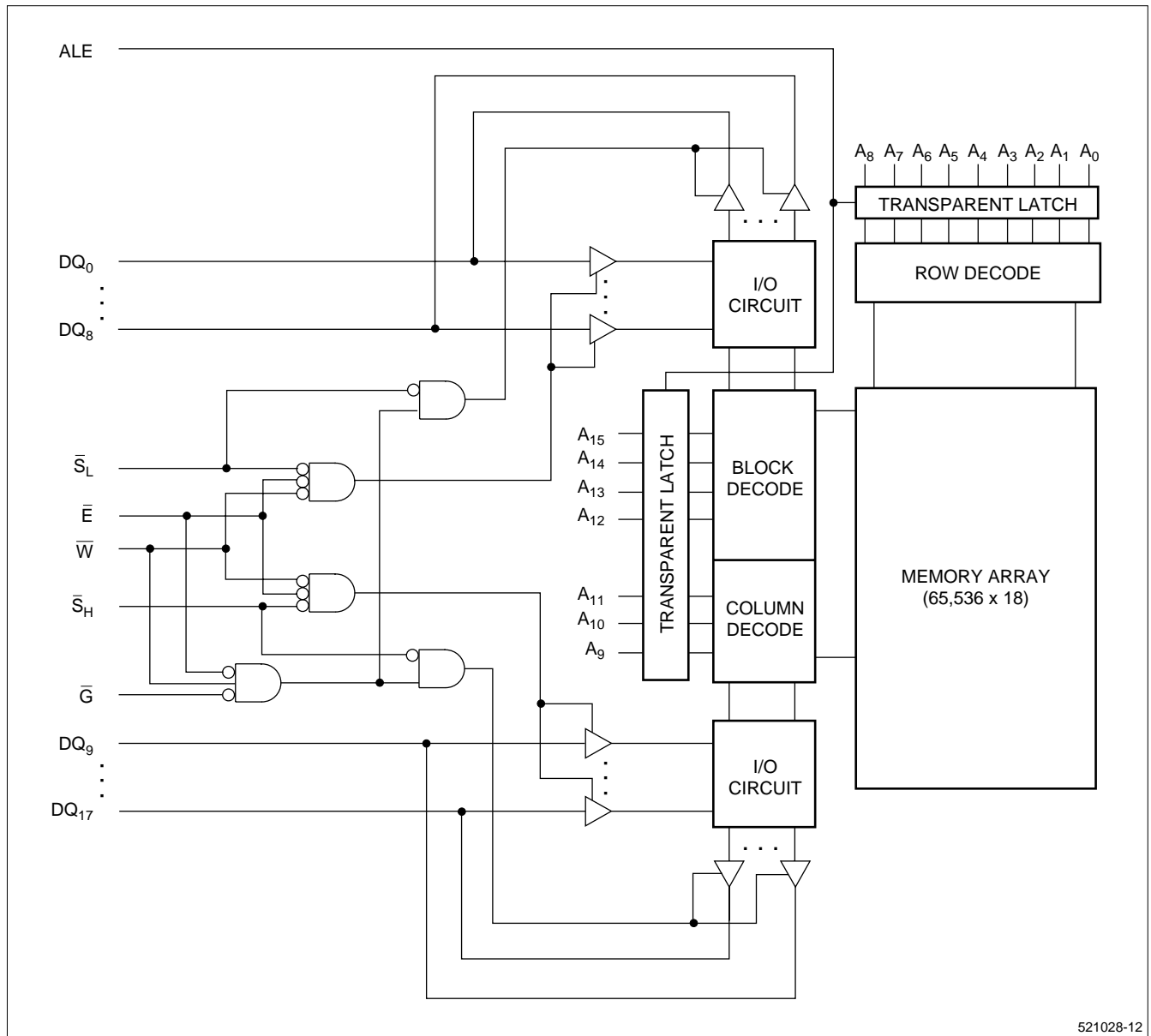


Figure 1. Pin Connections for PLCC Package



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Figure 2. LH521028A Block Diagram

## TRUTH TABLE

ADDRESS	$\bar{E}$	$\bar{S}_H$	$\bar{S}_L$	ALE	$\bar{G}$	$\bar{W}$	DQ <sub>0</sub> -DQ <sub>8</sub>	DQ <sub>9</sub> -DQ <sub>17</sub>	MODE	I <sub>CC</sub>
Don't Care	H	X	X	H	X	X	High-Z	High-Z	Standby	I <sub>SB</sub>
Valid	L	L	H	H	L	H	Active	High-Z	Read	I <sub>CC1</sub>
Valid	L	H	L	H	L	H	High-Z	Active	Read	I <sub>CC1</sub>
Valid	L	L	L	H	L	H	Active	Active	Read	I <sub>CC1</sub>
Valid	L	L	L	H	H	H	High-Z	High-Z	Read	I <sub>CC1</sub>
Don't Care	L	L	L	L	L	H	Data Out	Data Out	Read	I <sub>CC1</sub>
Valid	L	L	H	H	X	L	Data In	Don't Care	Write, low byte	I <sub>CC1</sub>
Valid	L	H	L	H	X	L	Don't Care	Data In	Write, high byte	I <sub>CC1</sub>
Valid	L	L	L	H	X	L	Data In	Data In	Write, both bytes	I <sub>CC1</sub>
Valid	L	H	H	H	X	L	Don't Care	Don't Care	Write, inhibited	I <sub>CC1</sub>
Don't Care	L	L	L	L	X	L	Data In	Data In	Write, both bytes	I <sub>CC1</sub>

## NOTE:

X = Don't Care, L = LOW, H = HIGH

## PIN DESCRIPTIONS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	V <sub>SS</sub>	14	DQ <sub>13</sub>	27	V <sub>SS</sub>	40	DQ <sub>4</sub>
2	V <sub>CC</sub>	15	DQ <sub>14</sub>	28	V <sub>CC</sub>	41	DQ <sub>5</sub>
3	$\bar{S}_L$	16	V <sub>SS</sub>	29	A <sub>8</sub>	42	V <sub>SS</sub>
4	$\bar{S}_H$	17	V <sub>CC</sub>	30	A <sub>9</sub>	43	V <sub>CC</sub>
5	$\bar{E}$	18	DQ <sub>15</sub>	31	A <sub>10</sub>	44	DQ <sub>6</sub>
6	A <sub>0</sub>	19	DQ <sub>16</sub>	32	A <sub>11</sub>	45	DQ <sub>7</sub>
7	A <sub>1</sub>	20	DQ <sub>17</sub>	33	A <sub>12</sub>	46	DQ <sub>8</sub>
8	DQ <sub>9</sub>	21	A <sub>2</sub>	34	DQ <sub>0</sub>	47	A <sub>13</sub>
9	DQ <sub>10</sub>	22	A <sub>3</sub>	35	DQ <sub>1</sub>	48	A <sub>14</sub>
10	V <sub>CC</sub>	23	A <sub>4</sub>	36	V <sub>CC</sub>	49	A <sub>15</sub>
11	V <sub>SS</sub>	24	A <sub>5</sub>	37	V <sub>SS</sub>	50	$\bar{G}$
12	DQ <sub>11</sub>	25	A <sub>6</sub>	38	DQ <sub>2</sub>	51	ALE
13	DQ <sub>12</sub>	26	A <sub>7</sub>	39	DQ <sub>3</sub>	52	$\bar{W}$

## PIN DEFINITIONS

**V<sub>CC</sub>** Positive Supply Voltage Terminals

**V<sub>SS</sub>** Reference Terminals

**A<sub>0</sub> – A<sub>15</sub>** Address Bus **Input**

The Address bus is decoded to select one 18-bit word out of the total 64K words for Read and Write operations.

**$\overline{E}$**  Chip Enable **Active LOW Input**

Chip Enable is used to enable the device for Read and Write operations. When HIGH, both Read and Write operations are disabled and the device is in a reduced power state. When LOW, a Read or Write operation is enabled.

**$\overline{W}$**  Write Enable **Active LOW Input**

Write Enable is used to select either Read or Write operations when the device is enabled. When Write Enable is HIGH and the device is Enabled, a Read operation is selected. When Write Enable is LOW and the device is enabled, a Write operation is selected. A Byte-write operation is available by using the Byte-select controls.

**$\overline{S}_H, \overline{S}_L$**  Select High Select Low **Active LOW Inputs**

The Select High and Select Low signals, in conjunction with the Chip Enable and Write Enable signals, allow the selection of the individual bytes for Read and Write operations. When High, the Select signal will deselect its

byte and prevent Read or Write operations. When the Select signal is LOW and Chip Enable is LOW, a Read or Write operation is performed at the location determined by the contents of the Address bus. When Chip Enable is HIGH, the Select signals are Don't Care. Select Low ( $\overline{S}_L$ ) is assigned to DQ<sub>0</sub> – DQ<sub>8</sub> and Select High ( $\overline{S}_H$ ) is assigned to DQ<sub>9</sub> – DQ<sub>17</sub>.

**ALE** Address Latch Enable **Active High Input**

The Address Latch Enable signal is used to control the Transparent latches on the Address bus. The Latches are transparent when HIGH and are latched when LOW. If not required, Address Latch Enable may be tied HIGH, leaving the Address bus in a transparent condition.

**DQ<sub>0</sub> – DQ<sub>17</sub>** Data Bus **Input/Output**

DQ<sub>0</sub> – DQ<sub>8</sub> comprise the Low byte, selected by  $\overline{S}_L$ , and DQ<sub>9</sub> – DQ<sub>17</sub> comprise the High Data byte, selected by  $\overline{S}_H$ . The Data Bus is in a high impedance input mode during Write operations and standby. The Data bus is in a low-impedance output mode during Read operations.

**$\overline{G}$**  Output Enable **Active LOW Input**

The Output Enable signal is used to control the output buffers on the Data Input/Output bus. When  $\overline{G}$  is HIGH, all output buffers are forced to a high impedance condition. When  $\overline{G}$  is LOW, the output buffers will become active only during a Read operation ( $\overline{E}$  and  $\overline{S}_H / \overline{S}_L$  are LOW,  $\overline{W}$  is HIGH).

**ABSOLUTE MAXIMUM RATINGS**<sup>1</sup>

PARAMETER	RATING
V <sub>CC</sub> to V <sub>SS</sub> Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V <sub>CC</sub> + 0.5 V
DC Output Current <sup>2</sup>	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 W

**NOTES:**

- Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

**OPERATING RANGES**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T <sub>A</sub>	Temperature, Ambient	0		70	°C
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
V <sub>IL</sub>	Logic '0' Input Voltage <sup>1</sup>	−0.5		0.8	V
V <sub>IH</sub>	Logic '1' Input Voltage	2.2		V <sub>CC</sub> + 0.5	V

**NOTE:**

- Negative undershoot of up to 3.0 V is permitted once per cycle.

**DC ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>CC1</sub>	Operating Current <sup>1</sup>	t <sub>CYCLE</sub> = minimum			300	mA
I <sub>SB1</sub>	Standby Current	$\bar{E} \geq V_{CC} - 0.2 V$ $V_{IN} \geq V_{CC} - 0.2 V$ or $V_{IN} \leq 0.2 V$ $f = 0$			4	mA
I <sub>SB2</sub>	Standby Current	$\bar{E} \geq V_{IH}$ $V_{IN} = V_{IH}$ or $V_{IL}$			50	mA
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	−2		2	μA
I <sub>LO</sub>	I/O Leakage Current	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	−2		2	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = −4.0 mA	2.4			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8.0 mA			0.4	V

**NOTE:**

- I<sub>CC</sub> is dependent upon output loading and cycle rates. Specified values are with outputs open.

## AC TEST CONDITIONS

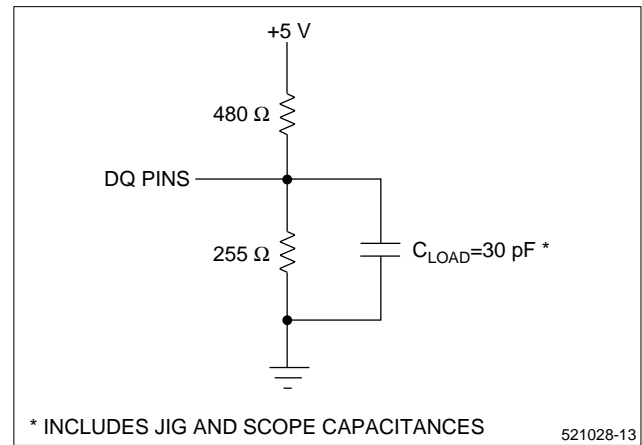
PARAMETER	RATING
Input Pulse Levels	V <sub>SS</sub> to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

## CAPACITANCE <sup>1,2</sup>

PARAMETER	RATING
C <sub>IN</sub> (Input Capacitance)	5 pF
C <sub>DQ</sub> (I/O Capacitance)	7 pF

### NOTES:

- Capacitances are maximum values at 25°C measured at 1.0 MHz with V<sub>Bias</sub> = 0 V and V<sub>CC</sub> = 5.0 V.
- Guaranteed but not tested.



**Figure 3. Output Load Circuit**

AC ELECTRICAL CHARACTERISTICS <sup>1</sup> (Over Operating Range)

SYMBOL	DESCRIPTION	-15		-17		-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<b>READ CYCLE</b>												
t <sub>RC</sub>	Read Cycle Timing	15		17		20		25		35		ns
t <sub>AA</sub>	Address Access Time		15		17		20		25		35	ns
t <sub>ASL</sub>	Address Setup to Latch Enable	2		2		2		2		2		ns
t <sub>AHL</sub>	Address Hold from Latch Enable	3		3		4		4		4		ns
t <sub>LEA</sub>	Latch Enable to Data Valid		16		18		21		26		36	ns
t <sub>LHM</sub>	Latch Enable High Pulse Width	5		5		5		5		5		ns
t <sub>OH</sub>	Output Hold from Address Change	4		4		4		4		4		ns
t <sub>LH</sub>	Output Hold from Latch High	4.5		4.5		4.5		4.5		4.5		ns
t <sub>EA</sub>	$\bar{E}$ Low to Valid Data		15		17		20		25		35	ns
t <sub>ELZ</sub>	$\bar{E}$ Low to Output Active <sup>2,3</sup>	3		3		3		3		3		ns
t <sub>EHZ</sub>	$\bar{E}$ High to Output High-Z <sup>2,3</sup>		9		10		10		12		20	ns
t <sub>SA</sub>	$\bar{S}$ Low to Valid Data		7		8		10		12		20	ns
t <sub>SLZ</sub>	$\bar{S}$ Low to Output Active <sup>2,3</sup>	2		2		2		3		3		ns
t <sub>SHZ</sub>	$\bar{S}$ High to Output High-Z <sup>2,3</sup>		10		10		10		12		20	ns
t <sub>GA</sub>	$\bar{G}$ Low to Valid Data		7		8		9		12		20	ns
t <sub>GLZ</sub>	$\bar{G}$ Low to Output Active <sup>2,3</sup>	0		0		0		0		0		ns
t <sub>GHZ</sub>	$\bar{G}$ High to Output High-Z <sup>2,3</sup>		7		8		8		10		20	ns
t <sub>RCS</sub>	Read Setup from $\bar{W}$ High	0		0		0		0		0		ns
t <sub>RCH</sub>	Read Hold from $\bar{W}$ Low	0		0		0		0		0		ns
t <sub>PU</sub>	$\bar{E}$ LOW to Power Up Time <sup>3</sup>	0		0		0		0		0		ns
t <sub>PD</sub>	$\bar{E}$ HIGH to Power Down Time <sup>3</sup>		15		17		20		25		35	ns
t <sub>WA</sub>	Access Time From Write Enable HIGH		18		20		20		25		35	ns
<b>WRITE CYCLE</b>												
t <sub>WC</sub>	Write Cycle Time	15		17		20		25		35		ns
t <sub>EW</sub>	$\bar{E}$ Low to End of Write	11		12		13		20		30		ns
t <sub>SW</sub>	$\bar{S}$ LOW to End of Write	7		8		10		20		30		ns
t <sub>AW</sub>	Address Valid to End of Write	11		12		13		20		30		ns
t <sub>AS</sub>	Address Setup to Start of Write	0		0		0		0		0		ns
t <sub>AH</sub>	Address Hold from End of Write	0		0		0		0		0		ns
t <sub>ASL</sub>	Address Setup to Latch Enable	2		2		2		2		2		ns
t <sub>AHL</sub>	Address Hold from Latch Enable	3		3		4		4		4		ns
t <sub>LHW</sub>	Latch Hold from $\bar{W}$ High	0		0		0		0		0		ns
t <sub>LHM</sub>	Latch Enable HIGH Pulse Width	5		5		5		5		5		ns
t <sub>WP</sub>	$\bar{W}$ Pulse Width	11		12		13		20		30		ns
t <sub>DW</sub>	Input Data Setup Time	7		8		9		10		15		ns
t <sub>DH</sub>	Input Data Hold Time	0		0		0		0		0		ns
t <sub>WHZ</sub>	$\bar{W}$ Low to Output High-Z <sup>2,3</sup>		7		8		8		10		14	ns
t <sub>WLZ</sub>	$\bar{W}$ High to Output Active <sup>2,3</sup>	3		3		3		3		3		ns

**NOTES:**

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C<sub>Load</sub> = 5 pF.
3. Guaranteed but not tested.

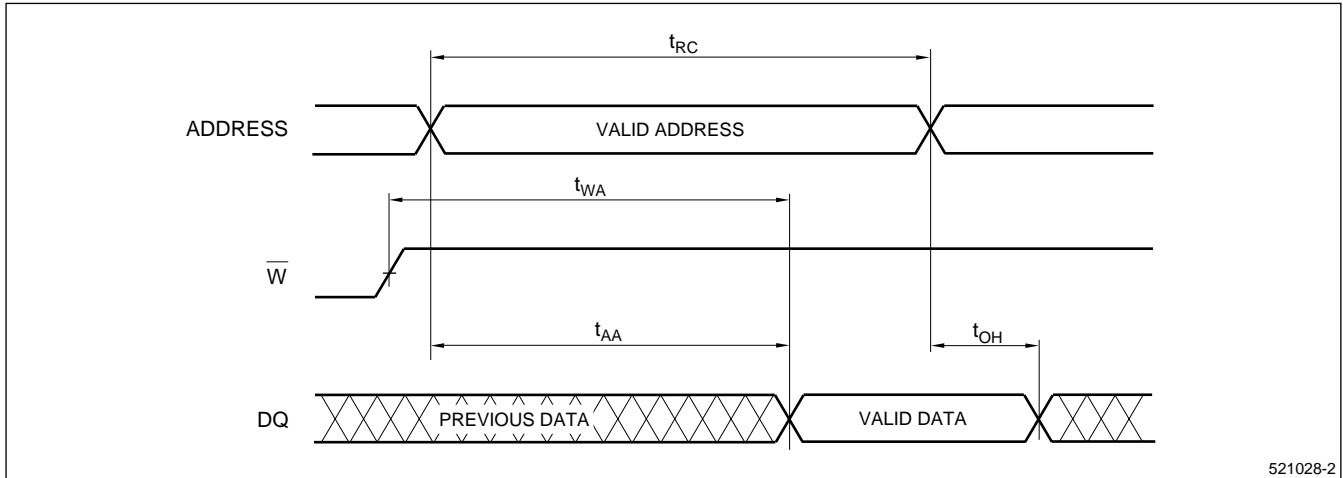
**TIMING DIAGRAMS – READ CYCLE**

**Read Cycle No. 1  
(Unlatched Address Controlled Read)**

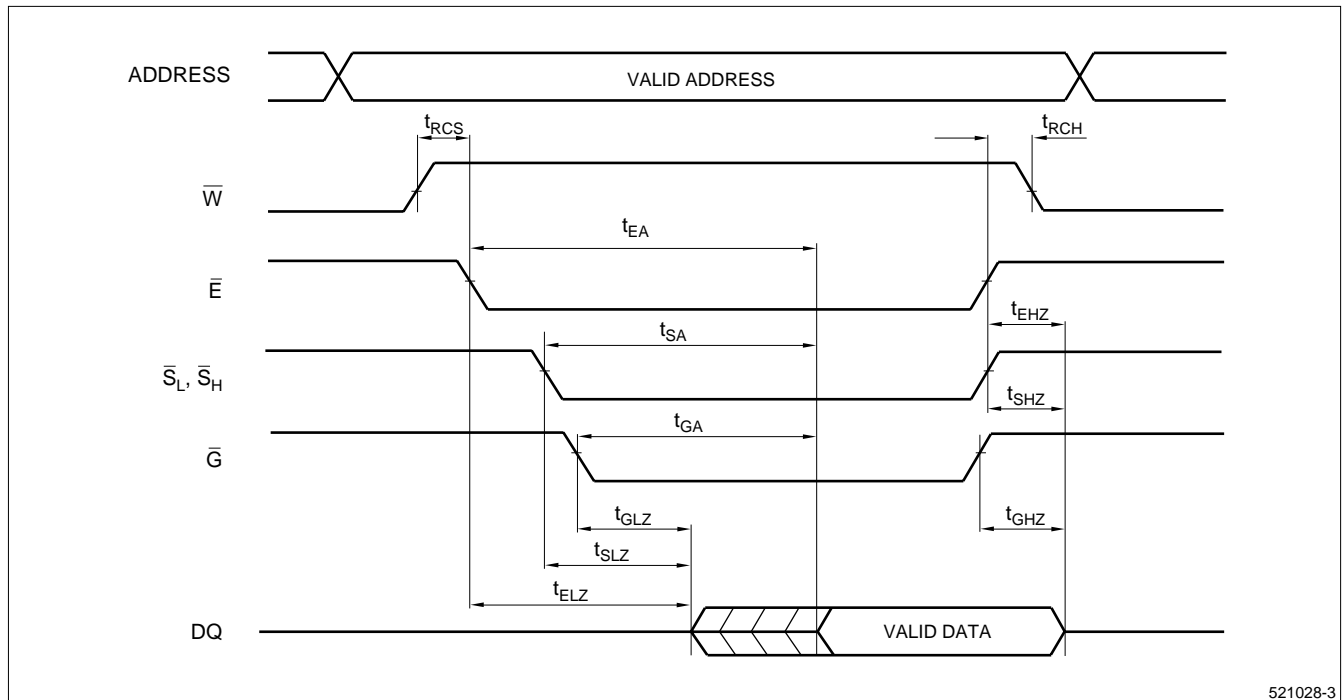
Chip is in Read Mode: ALE is HIGH (transparent mode),  $\bar{E}$  and  $\bar{G}$  are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Following a  $\bar{W}$ -controlled Write cycle,  $t_{WA}$  and  $t_{AA}$  must both be satisfied to ensure valid data. Cross-hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until  $t_{AA}$ .

**Read Cycle No. 2  
(Unlatched Chip Enable Controlled Read)**

Chip is in Read Mode: ALE is HIGH (transparent mode). Read cycle timing is referenced from when  $\bar{E}$ ,  $\bar{S}$ , and  $\bar{G}$  are stable until the first address transition. Cross-hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid.



**Figure 4. Read Cycle No. 1**



**Figure 5. Read Cycle No. 2**

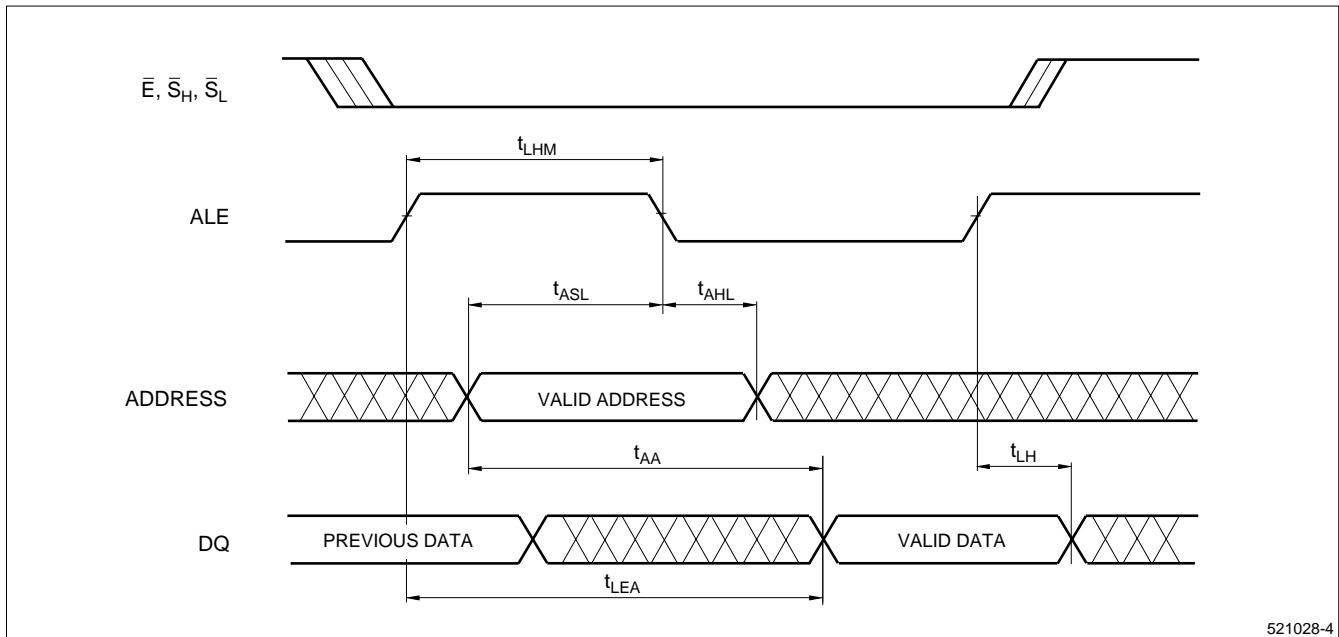


**TIMING DIAGRAMS – READ CYCLE (cont'd)**

**Read Cycle No. 3  
(Latched Address Controlled Read)**

Chip is in Read Mode:  $\bar{W}$  is HIGH,  $\bar{E}$ ,  $\bar{S}_H$ ,  $\bar{S}_L$  and  $\bar{G}$  are LOW. Both  $t_{AA}$  and  $t_{LEA}$  must be met before valid data is available. If the address is valid prior to the rising edge of

ALE, then the access time is  $t_{LEA}$ . If the address is valid after ALE is HIGH (or if ALE is tied HIGH) then the access time is  $t_{AA}$ . Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until  $t_{AA}$ .

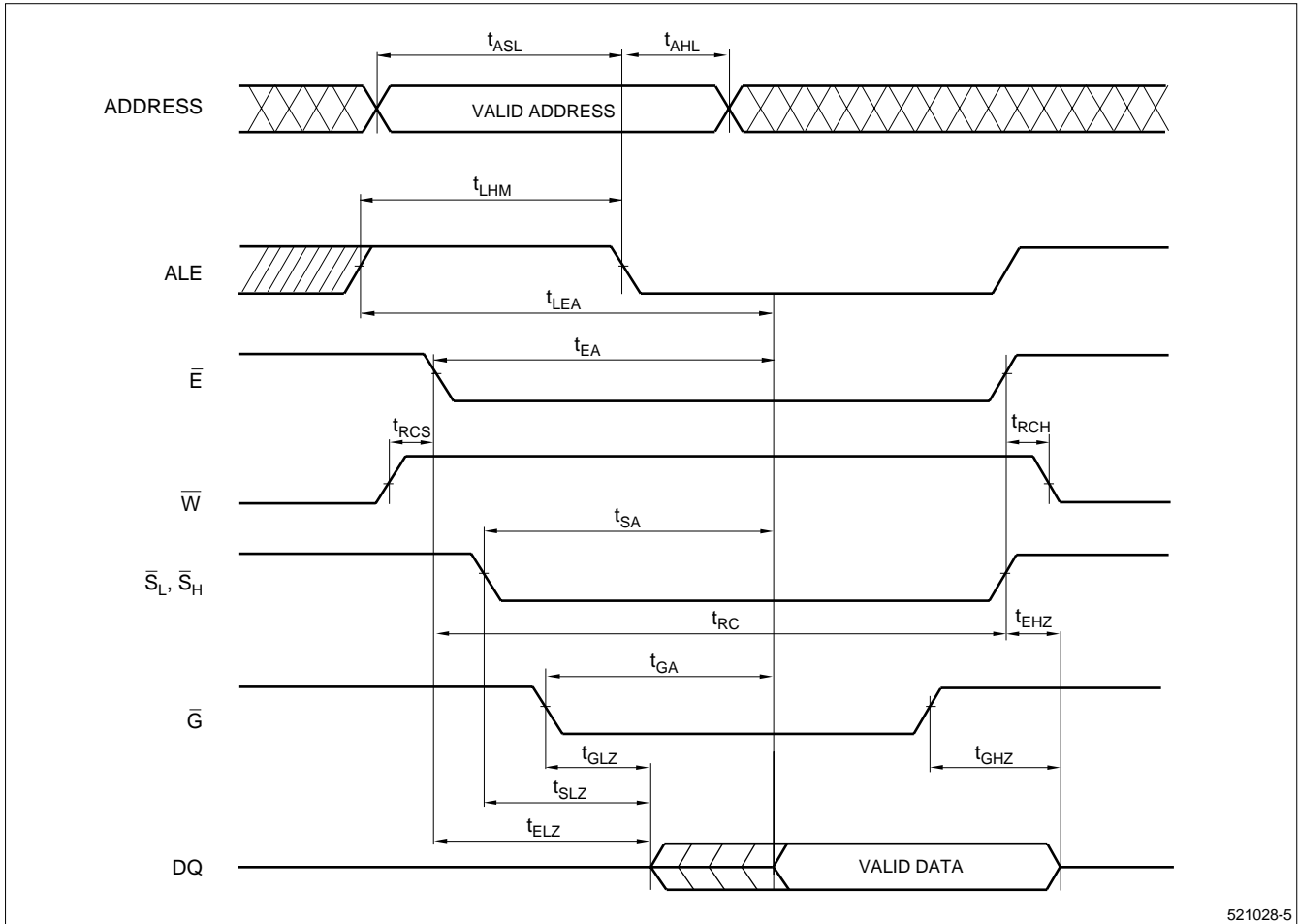


**Figure 6. Read Cycle No. 3**

**TIMING DIAGRAMS – READ CYCLE (cont'd)**

**Read Cycle No. 4**

Chip is in Read Mode: Timing illustrated for the case when addresses are valid before  $\bar{E}$  goes LOW. Data Out is not specified to be valid until  $t_{EA}$ ,  $t_{SA}$  and  $t_{GA}$ , but may become active as early as  $t_{ELZ}$ ,  $t_{SLZ}$  or  $t_{GLZ}$ .



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**Figure 7. Read Cycle No. 4**

**TIMING DIAGRAMS – WRITE CYCLE**

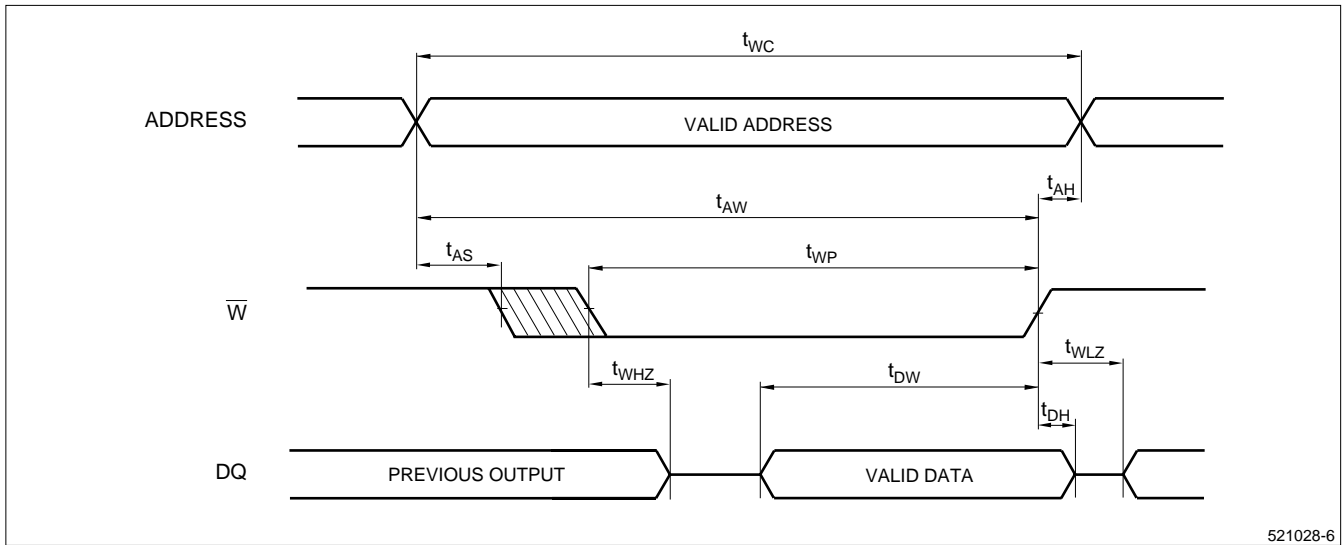
Addresses must be stable during unlatched Write cycles. The outputs will remain in the High-Z state if  $\overline{W}$  is LOW when  $\overline{E}$  and  $\overline{S}_H / \overline{S}_L$  go LOW. If  $\overline{G}$  is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with  $\overline{G}$  active, it is recommended that  $\overline{G}$  be held HIGH for all Write cycles. This will prevent the LH521028's outputs from becoming active, preventing bus contention, thereby reducing system noise.

**Write Cycle No. 1 (Unlatched  $\overline{W}$  Controlled Write)**

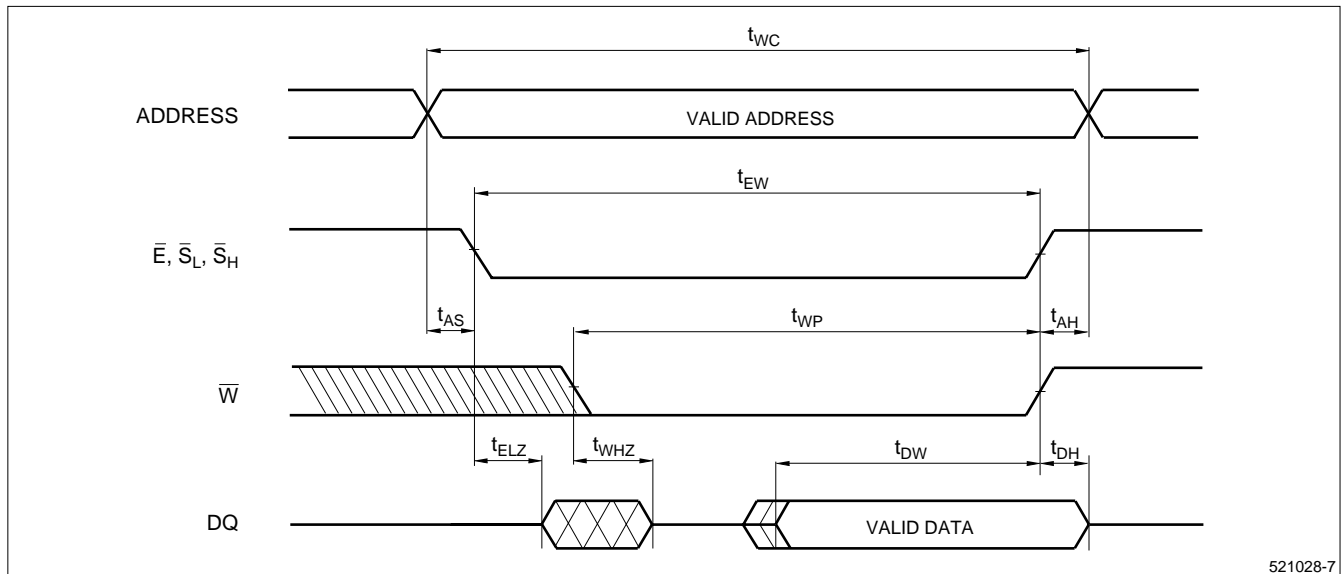
Chip is selected:  $\overline{E}$ ,  $\overline{G}$ , and  $\overline{S}_H / \overline{S}_L$  are LOW, ALE is High. Using only  $\overline{W}$  to control Write cycles may not offer the best performance since both  $t_{WHZ}$  and  $t_{DW}$  timing specifications must be met.

**Write Cycle No. 2 ( $\overline{E}$ ,  $\overline{S}_L$ ,  $\overline{S}_H$  Controlled Write)**

$\overline{G}$  is LOW. DQ lines may transition to Low-Z if the falling edge of  $\overline{W}$  occurs after the falling edge of  $\overline{E}$ ,  $\overline{S}_H / \overline{S}_L$  if  $\overline{G}$  is LOW.



**Figure 8. Write Cycle No. 1**



**Figure 9. Write Cycle No. 2**

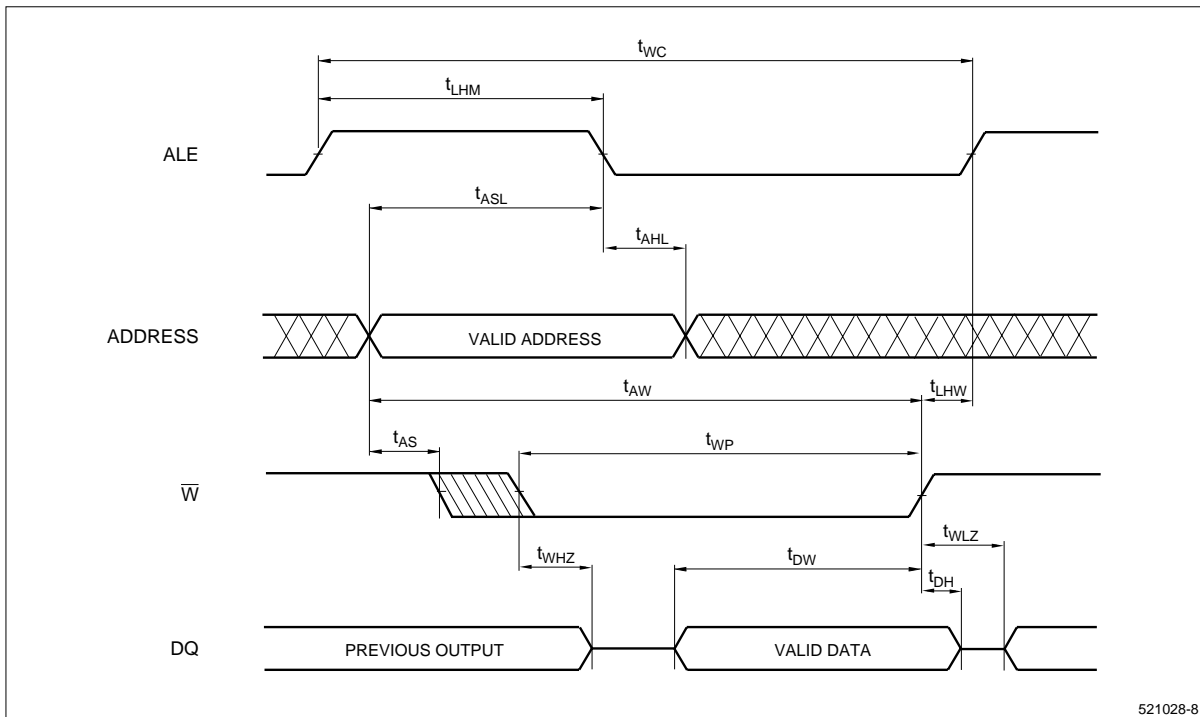
**TIMING DIAGRAMS – WRITE CYCLE (cont'd)**

**Write Cycle No. 3 (Latched  $\overline{W}$  Controlled Write)**

Chip is selected:  $\overline{E}$ ,  $\overline{G}$ , and  $\overline{S}_H / \overline{S}_L$  are LOW.

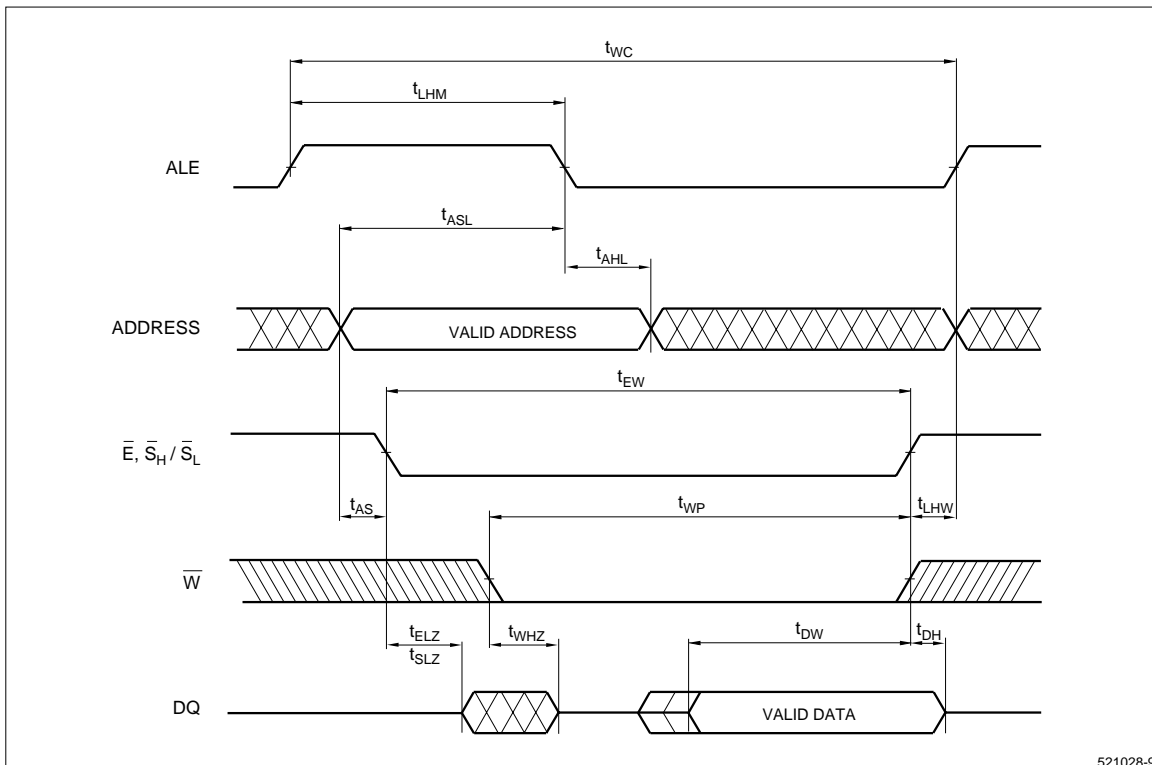
**Write Cycle No. 4 ( $\overline{E}$  Controlled)**

$\overline{G}$  is LOW. DQ lines may transition to Low-Z if the falling edge of  $\overline{W}$  occurs after the falling edges of  $\overline{E}$  and  $\overline{S}_H / \overline{S}_L$ .



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**Figure 10. Write Cycle No. 3**



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**Figure 11. Write Cycle No. 4**

## BYTE OPERATIONS

### Byte Read Description (Figure 12)

To read individual bytes, the device must be enabled ( $\bar{E}$  is LOW),  $\bar{W}$  must be HIGH, the outputs must be enabled ( $\bar{G}$  is LOW) and the addresses must be either stable or latched with ALE. Figure 12 is one example of the byte read capabilities of this device. The example shows two read operations. The first is a read of the high byte of the current memory location and the second is a read of the low byte of the memory location.

(1) At the beginning of the cycle both  $\bar{S}_L$  and  $\bar{S}_H$  are HIGH.

- (2)  $\bar{S}_H$  goes LOW initiating a Read on the upper byte  $DQ_{H(9-17)}$ .  $\bar{S}_L$  remains HIGH keeping the lower byte  $DQ_{L(0-8)}$  disabled and in a high-impedance mode.
- (3)  $\bar{S}_L$  goes LOW activating  $DQ_{L(0-8)}$ . Valid data is available in  $t_{SA}$  following  $\bar{S}_L$  going LOW.
- (4) When  $\bar{S}_H$  goes HIGH,  $DQ_{H(9-17)}$  remains valid for  $t_{SHZ}$  before returning to a high-impedance condition.
- (5) Finally, the Read for the lower byte is terminated by deasserting  $\bar{S}_L$  (HIGH).  $DQ_{L(0-8)}$  remains active for  $t_{SHZ}$  following  $\bar{S}_L$  going HIGH.

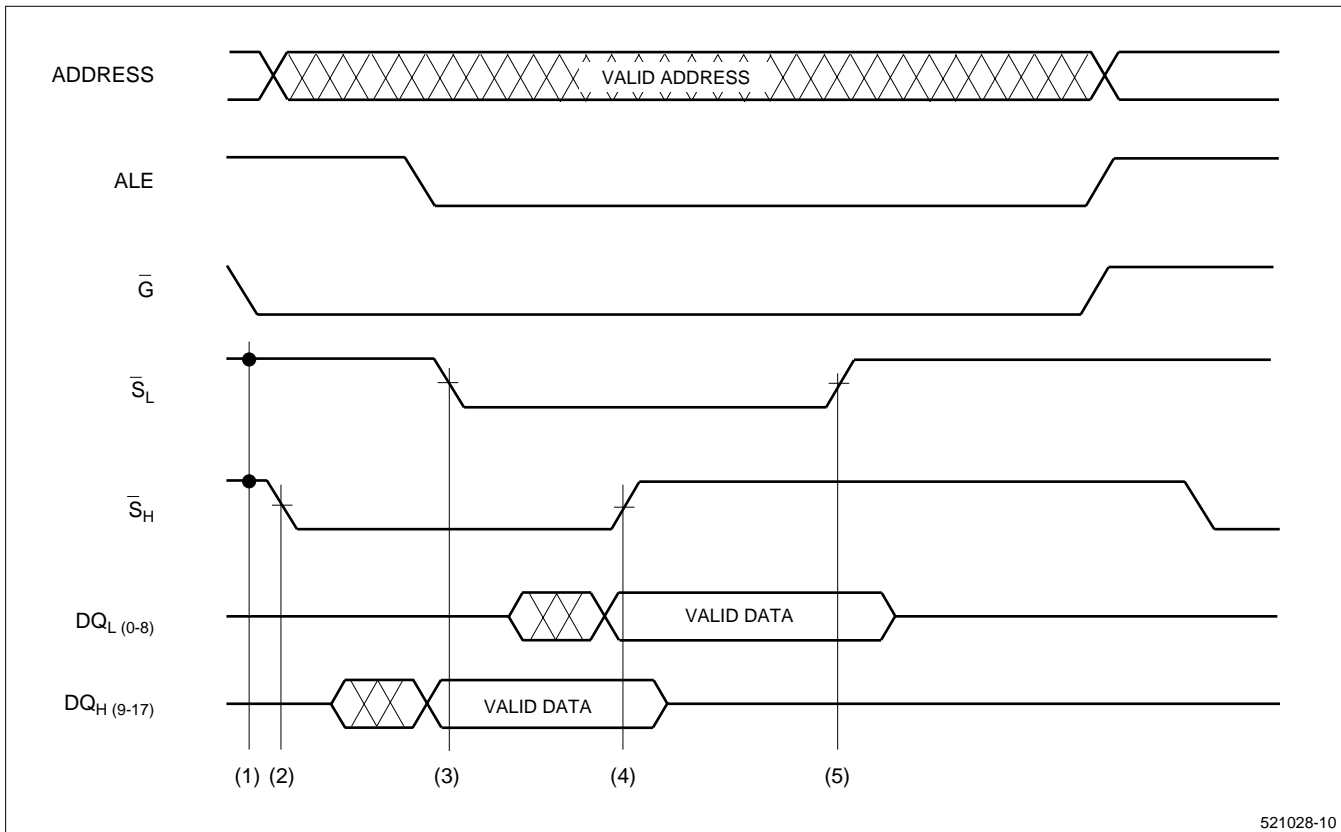


Figure 12. Byte Read ( $\bar{E}$  is LOW and  $\bar{W}$  is HIGH)

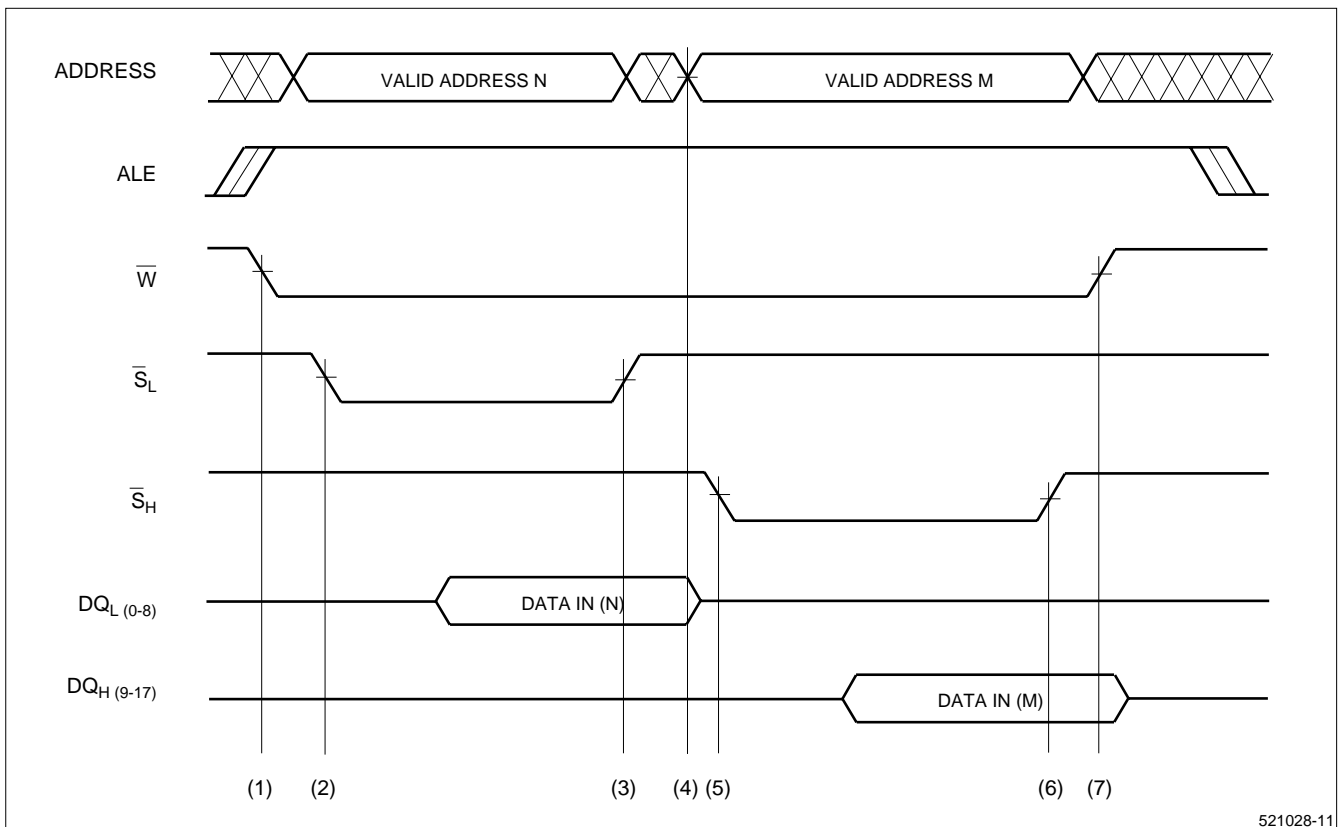
**BYTE OPERATIONS (cont'd)**

**Byte Write Description (Figure 13)**

To do individual byte-write operations, the device must be enabled ( $\bar{E}$  is LOW,  $\bar{G}$  is don't care) and addresses must be either stable or latched. Figure 13 is one example of the byte-write capabilities of this device. The diagram shows two write operations with unlatched addresses. The first is a write to the low byte of memory location N and the second is a write to the high byte of memory location M.

- (1)  $\bar{W}$  goes LOW while  $\bar{S}_L$  and  $\bar{S}_H$  remain HIGH.
- (2)  $\bar{S}_L$  goes LOW initiating a Write into the lower byte  $DQ_{L(0-8)}$  of memory location N.  $\bar{S}_H$  remains HIGH preventing a Write into the upper byte  $DQ_{L(9-17)}$  of memory location N.

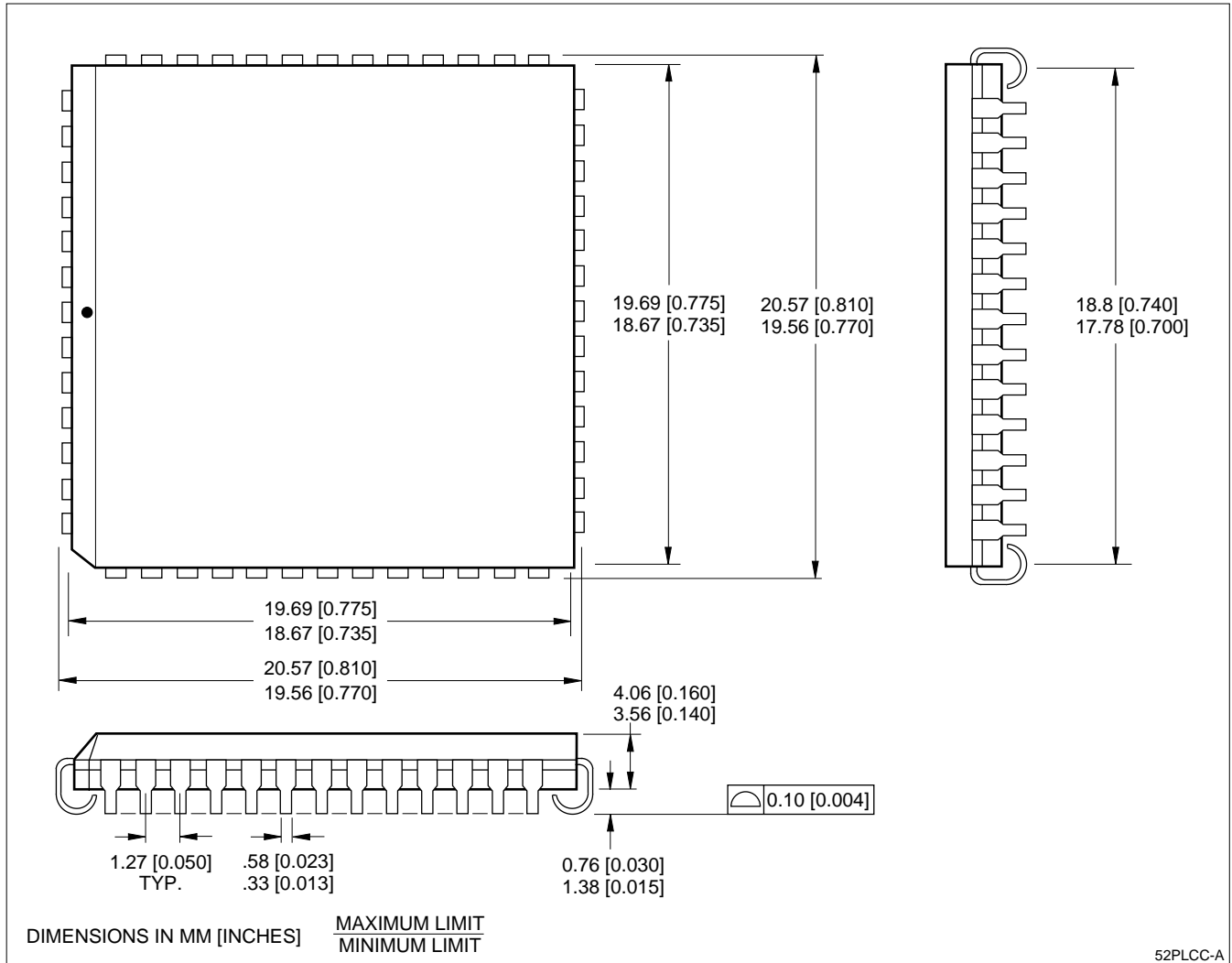
- (3)  $\bar{S}_L$  now goes HIGH terminating the Write operation on the lower byte of memory location N.
- (4) Address N is changed to M.
- (5) The Write operation is now initiated on the upper byte  $DQ_{H(9-17)}$  by bringing  $\bar{S}_H$  LOW.  $\bar{S}_L$  remains HIGH preventing a Write operation from occurring in the lower byte  $DQ_{L(0-8)}$  of memory location N+ 1.
- (6)  $\bar{S}_H$  now goes HIGH terminating the Write operation on the upper byte of address M.
- (7)  $\bar{W}$  goes HIGH, ending the Write operation.



**Figure 13. Byte Write ( $\bar{E}$  is LOW)**

521028-11

**PACKAGE DIAGRAM**



**52-Pin PLCC**

**ORDERING INFORMATION**

