PRELIMINARY
Notice ; This is not a final specification.
some parametric limits are subject to change.

M65830BP/FP

DIGITAL DELAY

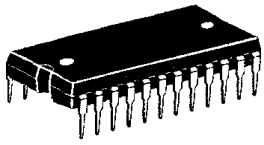
DESCRIPTION

The M65830B is a CMOS IC developed to produce surround effects on TV sets and video disc players.Among the series,it has the highest degree of freedom in the selection of delay time,so it permits fine adjustments when mounted on a set.

FEATURES

- Selection of delay time in a range between 0.5msec and 32.0msec in 64 increments of 0.5msec
- Selection of delay time is controlled by serial data
- Built-in A-D, D-A converters,input/output low-pass filter, and 16K bit memory
- High sound quality is assured by simple system construction,due to A-D, D-A converters with ADM (Adaptive Delta Modulation) system
  Output noise voltage : -95dBV (typ)
  Total harmonic distortion : 0.2% (typ)

Outline



Outline 24P4 (BP)
2.54mm pitch 600mil DIP
(13.0mm X 31.1mm X 3.8mm)

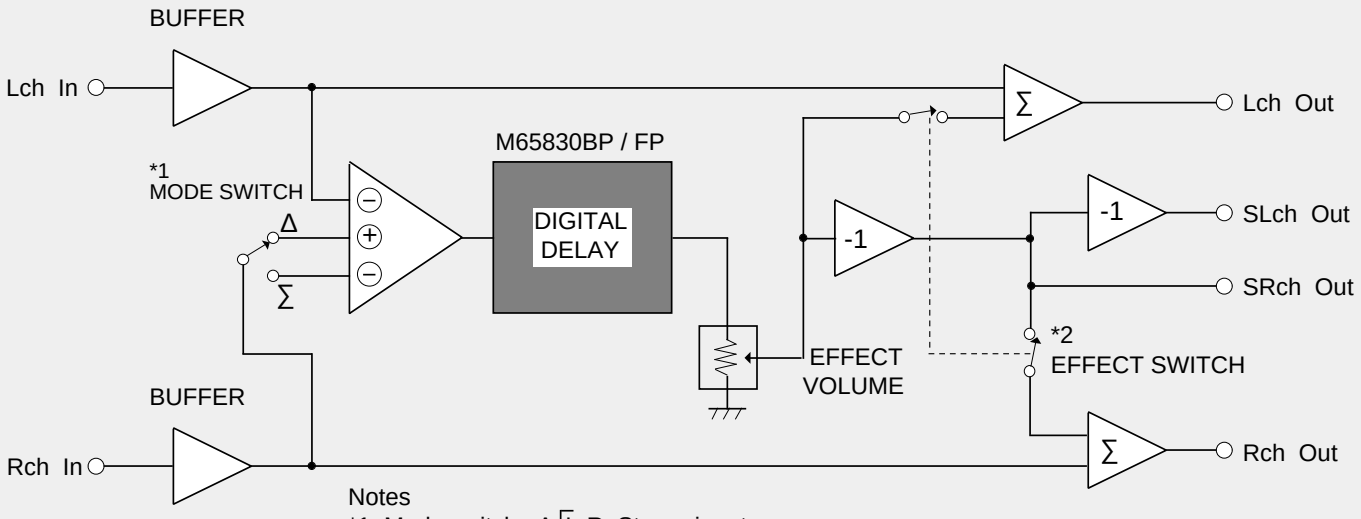
Outline 24P2W-A(BFP)
1.27mm pitch 450mil SOP
(8.4mm X15.0mm X2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ---------- VCC,VDD=4.5 to 5.5V

Rated supply voltage ---------- VCC,VDD=5V

SYSTEM CONFIGURATION

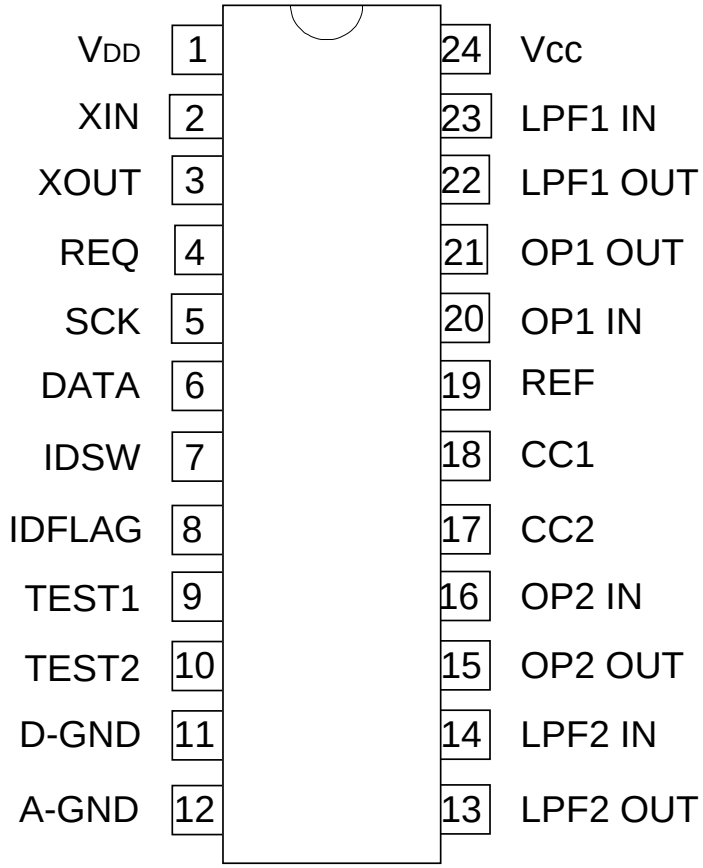


Notes
*1 Mode switch : Δ 「L-R」 Stereo input
Mode switch : Σ 「L+R」 Monaural input
*2 Effect switch ON: Surround output disabled (2 loudspeakers)
OFF:Surround output enabled(4 loudspeakers)

M65830BP/FP

DIGITAL DELAY

Pin Configuration

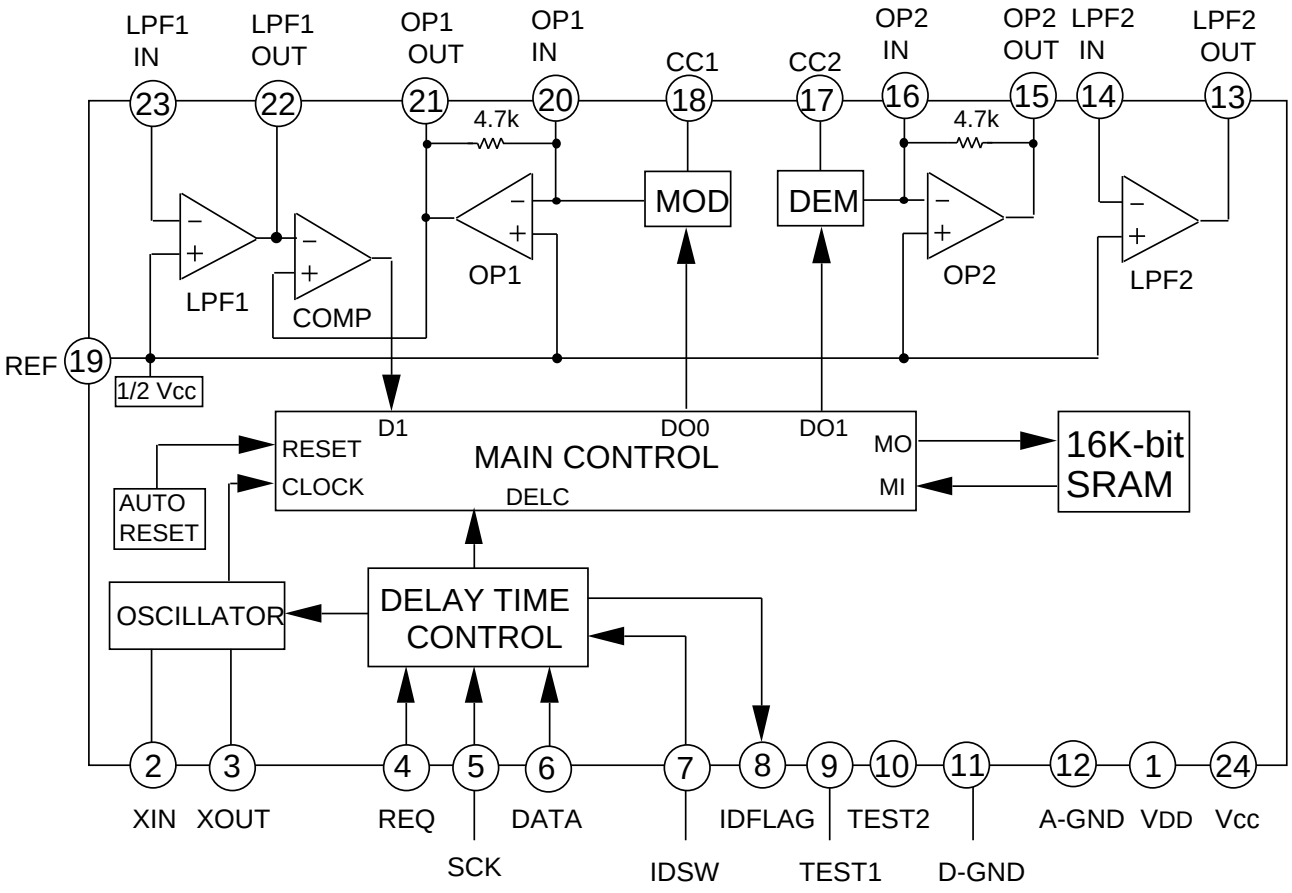


Outline 24P4 (BP)
24P2W-A (BFP)

M65830BP/FP

DIGITAL DELAY

BLOCK DIAGRAM



Unit Resistance: Ω

NC : NO CONNECTION

PIN DESCRIPTION

NO.	Symbol	Name	I/O	Function
①	VDD	Digital VDD	—	Supply voltage
②	XIN	Oscillator input	I	Connects ceramic filter or inputs an external clock
③	XOUT	Oscillator output	O	Connects ceramic filter/ Set to open when external is used
④	REQ	Request	I	Input request data from µ -COM
⑤	SCK	Shift clock	I	Input shift clock from µ -COM
⑥	DATA	Serial data	I	Input serial data from µ -COM
⑦	IDSW	ID switch	I	Controls ID code
⑧	IDFLAG	ID flag	O	Outputs pulse at setting function mode and function mode data
⑨	TEST1	Test 1	—	L=normal mode
⑩	TEST2	Test 2	—	L=normal mode
⑪	D-GND	Digital GND	—	Connects to analog GND at one point
⑫	A-GND	Analog GND	—	
⑬	LPF2 OUT	Lowpass filter2 output	O	Forms low pass filter with external C,R
⑭	LPF2 IN	Lowpass filter2 input	I	
⑮	OP2 OUT	OP-AMP2 output	O	Forms integrator with external C
⑯	OP2 IN	OP-AMP2 input	I	
⑰	CC2	Current control 2	—	Demodulator ADM control
⑱	CC1	Current control 1	—	Modulator ADM control
⑲	REF	Reference	—	1/2VCC
⑳	OP1 IN	OP-AMP1 input	I	Forms integrator with external C,R
㉑	OP1 OUT	OP-AMP1 output	O	
㉒	LPF1 OUT	Lowpass filter1 output	O	Forms low pass filter with external C,R
㉓	LPF1 IN	Lowpass filter1 input	I	
㉔	VCC	Analog VCC	—	Supply voltage

M65830BP/FP

DIGITAL DELAY

ABSOLUTE MAXIMUM RATINGS

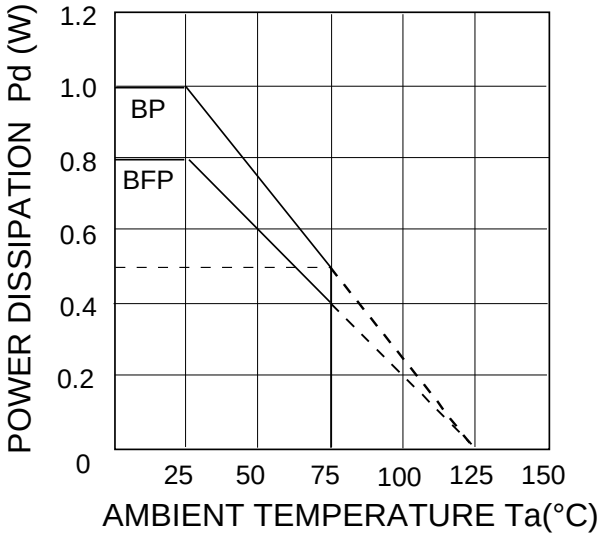
(Ta=25°C,unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Units
Vcc	Supply voltage			6.5	V
Icc	Circuit current			100	mA
Pd	Power dissipation	M65830BP		1	W
		M65830BFP		0.8	
Topr	Operating temperature			-20~+75	°C
Tstg	Storage temperature			-40~+125	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
Vcc	Supply voltage		4.5	5	5.5	V
V_{DD}	Supply voltage		4.5	5	5.5	V
Vcc-V_{DD}	Difference voltage		-0.3	0	0.3	V
fck	Clock frequency		1	2	3	MHz
V_{IH}	High input voltage		0.7VDD	—	V_{DD}	V
V_{IL}	Low input voltage		0	—	0.3VDD	V
f sck	Serial clock		—	—	4.0	MHz

THERMAL DERATING
(MAXIMUM RATING)



ELECTRICAL CHARACTERISTICS

(Vcc=5V,f=1kHz,Vi=100mV(rms),Ta=25°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
Icc	Circuit current	No signal	—	16	35	mA
Gv	Voltage gain	RL=47kΩ	-3.5	-0.5	2.5	dB
Vomax	Maximum output voltage	THD=10%	0.7	1	—	V(rms)
THD	Total harmonic distortion	30kHz LPF	—	0.2	1.0	%
No	Output noise voltage	DIN-AUDIO	—	-95	-75	dBV
SVRR	Supply voltage rejection ratio	ΔVcc=-20dBV,f=100Hz	—	-40	-25	dB
Iccs	Circuit current (Sleep Mode)	Sleep Mode	—	12	30	mA

OPERATION

1)DELAY TIME

D6	D5	D4	D3	D2	D1	Delay time(ms)
L	L	L	L	L	L	0.5
					H	1.0
				H	L	1.5
					H	2.0
			H	L	L	2.6
					H	3.1
				H	L	3.6
					H	4.1
		H	L	L	L	4.6
					H	5.1
				H	L	5.6
					H	6.1
			H	L	L	6.7
					H	7.2
				H	L	7.7
					H	8.2
	H	L	L	L	L	8.7
					H	9.2
				H	L	9.7
					H	10.2
			H	L	L	10.8
					H	11.3
				H	L	11.8
					H	12.3
		H	L	L	L	12.8
					H	13.3
				H	L	13.8
					H	14.3
			H	L	L	14.8
					H	15.4
				H	L	15.9
					H	16.4

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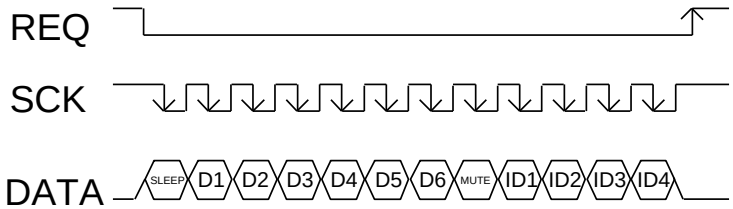
DIGITAL DELAY

D6	D5	D4	D3	D2	D1	Delay time(ms)
H	L	L	L	L	L	16.9
					H	17.4
				H	L	17.9
					H	18.4
			H	L	L	18.9
					H	19.5
				H	L	20.0
					H	20.5
		H	L	L	L	21.0
					H	21.5
				H	L	22.0
					H	22.5
			H	L	L	23.0
					H	23.6
				H	L	24.1
					H	24.6
	H	L	L	L	L	25.1
					H	25.6
				H	L	26.1
					H	26.6
			H	L	L	27.1
					H	27.6
				H	L	28.2
					H	28.7
		H	L	L	L	29.2
					H	29.7
				H	L	30.2
					H	30.7
			H	L	L	31.2
					H	31.7
				H	L	32.3
					H	32.8

2) SAMPLING FREQUENCY

fs=500kHz (at fck=2MHz)

3) SETTING DELAY TIME



Timing Diagram

D1~D6 : DELAY TIME ...12-1)
ID1~D4 : ID codes

This time chart shows that delay time is set by serial data from μ-COM.

DATA signal is latches at the falling edge of SCK signal, and the last twelve data are set at the rising edge of REQ signal when ID codes are satisfied*.

* { ID1 , ID2 : L
ID3 : H
ID4 : equal to IDSW

Sleep data is

{ H : clock and RAM stop to reduce circuit current (sleep mode)
L : normal operation

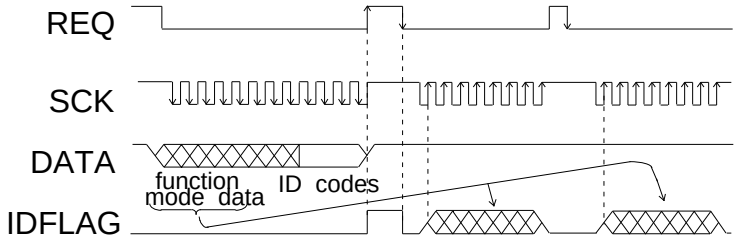
Mute data is

{ H : mute
L : not mute

4) ID CODE FLAG

When ID codes are satisfied, IDFLAG signal is set on high-level at rising of REQ signal, and it is set on low-level at falling of REQ signal.

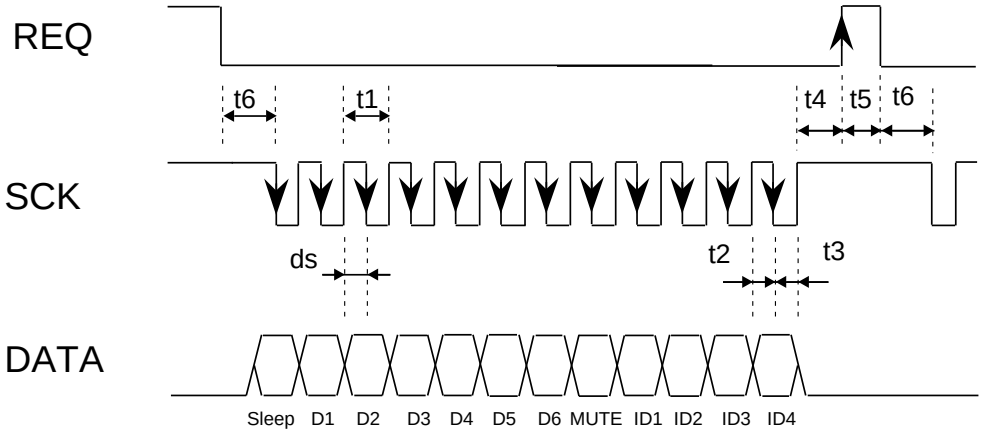
Each time the REQ signal fall the IDFLAG signal outputs function mode data (input from DATA signal) at the rising edge of the SCK signal.



5) SYSTEM RESET

It is automatic power-on reset, and the reset time is about 120ms. Then delay time is set on 20.0ms.

REQ,SCK,DATA INPUT TIMING



Symbol	Parameter	min	typ	max	Units
t1	SCK pulse width	250	—	—	ns
ds	SCK pulse duty	—	50	—	%
t2	DATA setup time	100	t1/2	—	ns
t3	DATA hold time	100	t1/2	—	ns
t4	REQ hold time	100	—	—	ns
t5	REQ pulse width	100	—	—	ns
t6	SCK setup time	100	—	—	ns

TEST METHODS

Switch condition

No	Parameter	Symbol	Conditions	PIN			SWITCH		
				4	5	6	S7	S24	S30
1	Circuit current	Icc	No signal	*	*	*	#	2	2
2	Voltage gain	Gv	Gv=20log(Vo/Vi)	*	*	*	#	1	1
3	Delay time	Td		*	*	*	#	1	1
4	Maximum Output voltage	Vomax	30kHz L.P.F. THD=10%	*	*	*	#	1	1
5	Total harmonic distortion	THD	30kHz L.P.F.	*	*	*	#	1	1
6	Output noise voltage	No	DIN AUDIO Vi=0mV(rms)	*	*	*	#	1	2
7	Supply voltage rejection ratio	SVRR	ΔVcc=-20dBv,f =100Hz	*	*	*	#	1	2
8	Circuit current (Sleep mode)	Iccs	Sleep mode	*	*	*	#	1	2

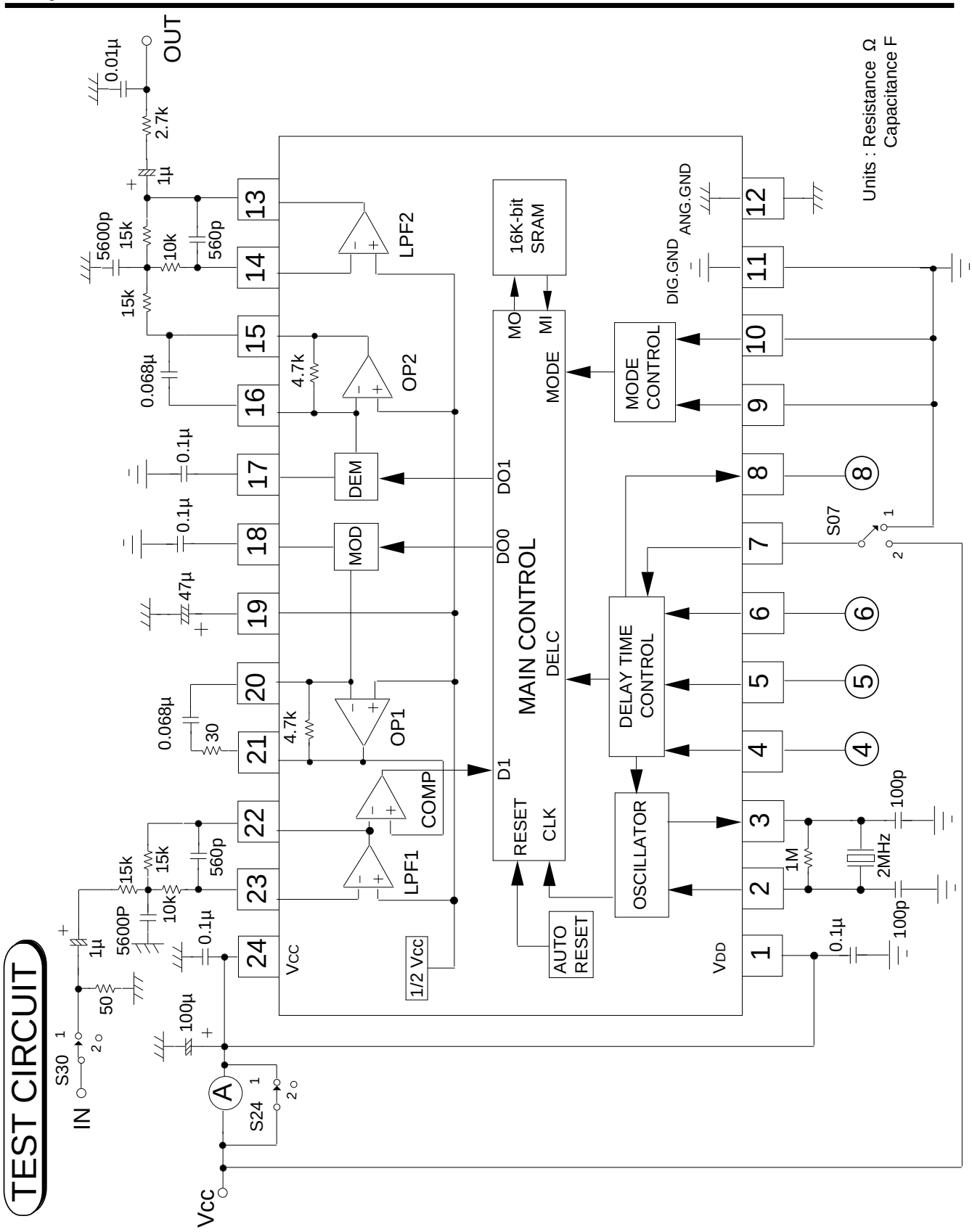
*....Serial Data "L " or "H"

#.... 1 or 2

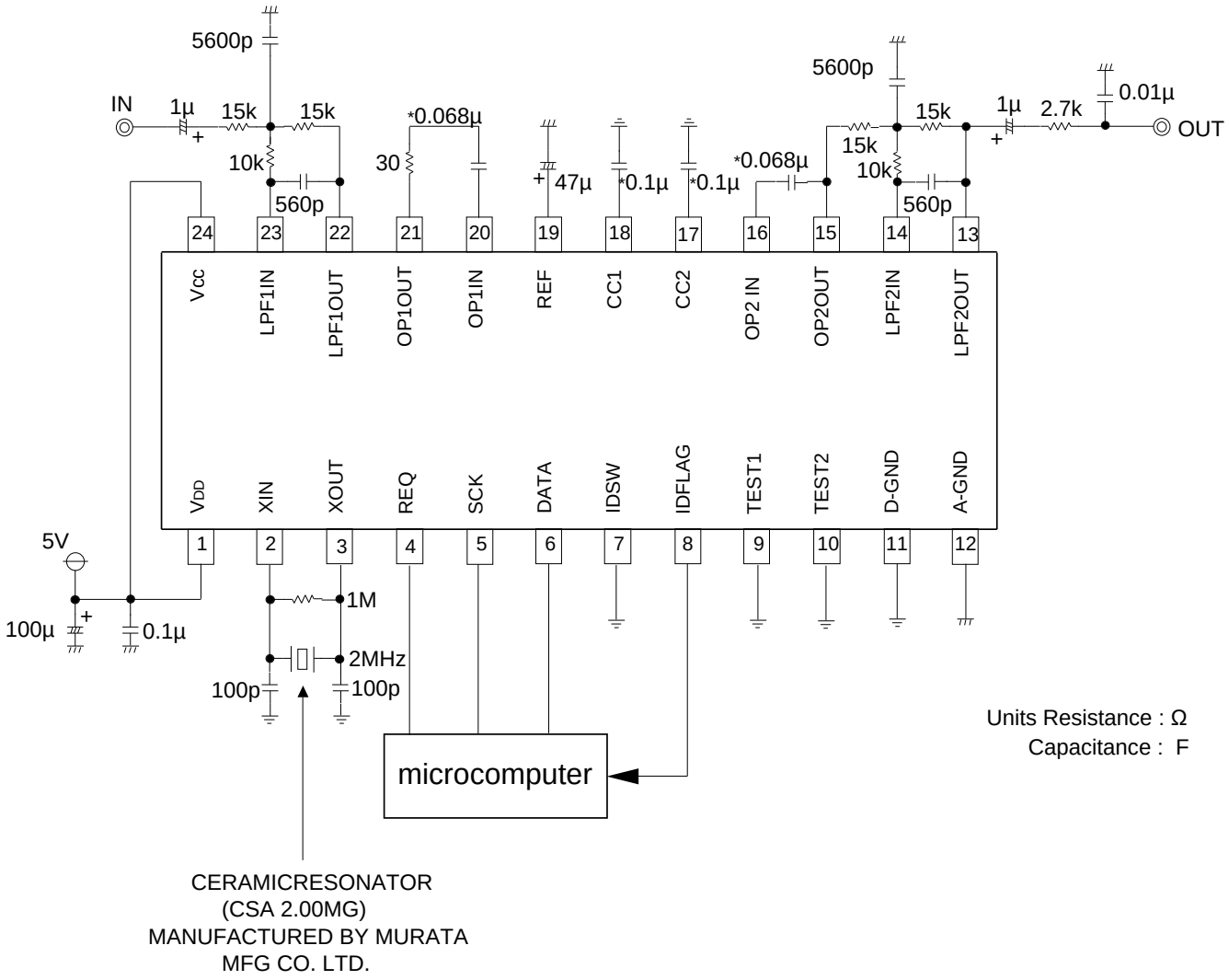
M65830BP/FP

DIGITAL DELAY

TEST CIRCUIT



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

CERAMICRESONATOR
(CSA 2.00MG)
MANUFACTURED BY MURATA
MFG CO. LTD.

The relative precision of capacitors marked with a * should be within ±5%