



**General Description**

The MIC10937 Alphanumeric Display Controllers is a MOS/LSI general purpose display controllers designed to interface to segmented displays (vacuum fluorescent or LED).

The MIC10937 will drive displays with up to 16 characters with 14 or 16 segments. Segment decoding within each device provides for the ASCII character set (upper case only). No external driver circuitry is required for displays that operate on 20mA of drive current up to 50V. A 16 × 64-bit segment decoder provides internal ASCII character set decoding for the display.

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**Features**

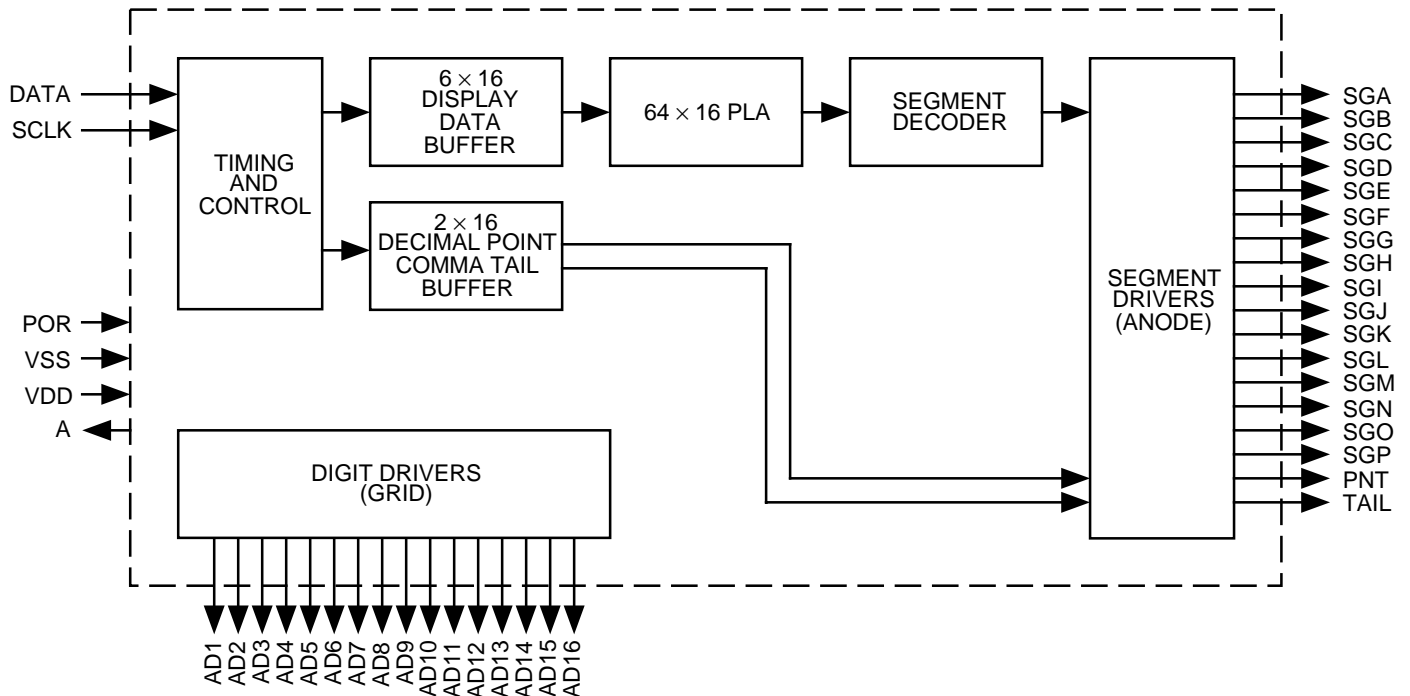
- 16-character display with decimal point and comma tail
- 14 or 16-segment drivers
- Up to 66kHz data rate
- Direct digit drive and 20mA at 50V
- Supports vacuum fluorescent or LED displays
- 64 × 16-bit PLA provides segment decoding for ASCII character set (all caps only)
- Serial data input for 8-bit display and control data words
- 40-pin DIP or 44-pin PLCC

**Ordering Information**

| Part Number                      | Drive | Temp. Range    | Package      |
|----------------------------------|-------|----------------|--------------|
| MIC10937J-40                     | 40V   | 0°C to +70°C   | 44-pin PLCC  |
| MIC10937P-40/<br>MIC10937P-50†   | 50V   | 0°C to +70°C   | 40-pin P-DIP |
| MIC10937PE-40/<br>MIC10937PE-50† | 50V   | -40°C to +85°C | 40-pin P-DIP |

† Dual-marked devices replace both 40V and 50V versions

**Block Diagram**



INTERFACE DESCRIPTION

Pin Functions

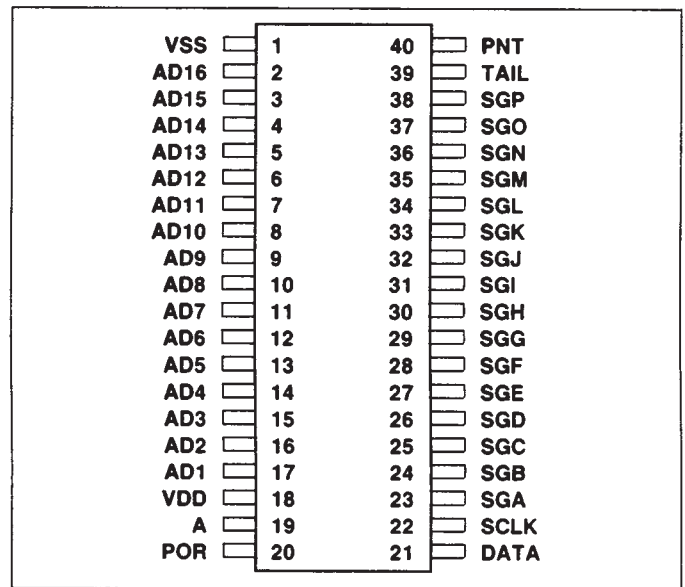
| Signal Name | Pin No. | Function                            |
|-------------|---------|-------------------------------------|
| VSS         | 1       | Power and signal reference          |
| AD16-AD1    | 2-17    | Digits 16 through 1 driver outputs  |
| VDD         | 18      | DC power connection                 |
| A           | 19      | A clock output used for testing     |
| POR         | 20      | Power-on reset input                |
| DATA        | 21      | Serial data input                   |
| SCLK        | 22      | Serial data clock input             |
| SGA-SGP     | 23-38   | Segments A through P driver outputs |
| TAIL        | 39      | Comma tail driver output            |
| PNT         | 40      | Decimal point driver output         |

SPECIFICATIONS

MAXIMUM RATINGS\*

All voltages are specified relative to V<sub>SS</sub>.

| Parameter               | Symbol           | Min  | Max  | Unit |
|-------------------------|------------------|------|------|------|
| Supply Voltage          | V <sub>DD</sub>  | +0.3 | -20  | V    |
| Input Voltage           | V <sub>IN</sub>  | +0.3 | -20  | V    |
| Output Voltage          | V <sub>OUT</sub> | +0.3 | -50  | V    |
| Operating Current       | I <sub>DD</sub>  |      | 7    | mA   |
| Output Current Digits   | I <sub>SD</sub>  |      | 20   | mA   |
| Output Current Segments | I <sub>SS</sub>  |      | 10   | mA   |
| Operating Temperature   |                  |      |      |      |
| Commercial              | T <sub>C</sub>   | 0    | +70  | °C   |
| Industrial              | T <sub>I</sub>   | -40  | +85  | °C   |
| Storage Temperature     | T <sub>STG</sub> | -55  | +125 | °C   |
| Input Capacitance       | C <sub>IN</sub>  |      | 5    | pF   |
| Output Capacitance      | C <sub>OUT</sub> |      | 10   | pF   |



Pin Configuration

\*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

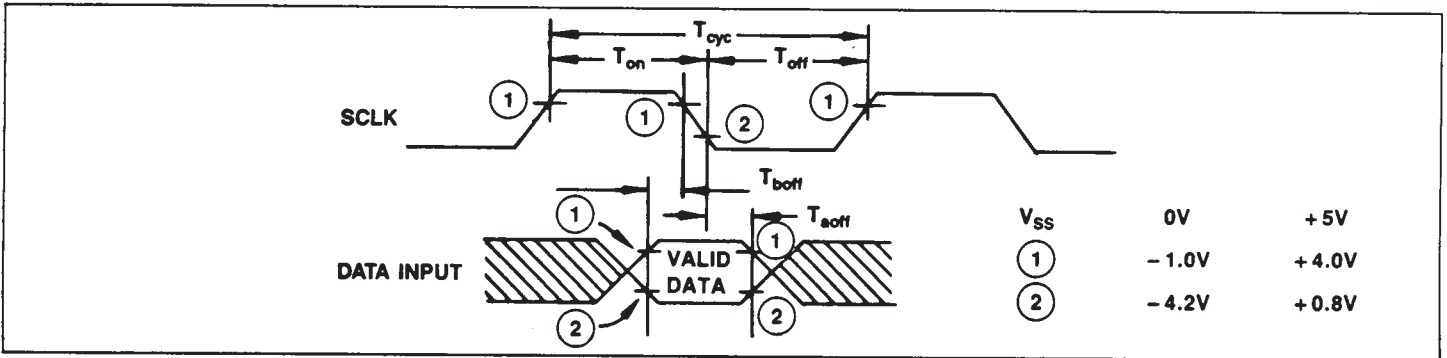
DC CHARACTERISTICS

| Parameter                         | Limits (V <sub>SS</sub> = 0) |       |       | Limits (V <sub>SS</sub> = +5V) |       |      | Conditions                                  | Unit |
|-----------------------------------|------------------------------|-------|-------|--------------------------------|-------|------|---|------|
|                                   | Min.                         | Typ.  | Max.  | Min.                           | Typ.  | Max. |   |      |
| Supply Voltage (V <sub>DD</sub> ) | -16.5                        | -15.0 | -13.5 | -11.5                          | -10.0 | -8.5 |   | V    |
| Power dissipation                 |                              | 40    | 100   |                                | 40    | 100  |   | mW   |
| Input DATA, SCLK, Logic "1"       | -1.0                         |       | +0.3  | +4.0                           |       | +5.3 |   | V    |
| Input DATA, SCLK, Logic "0"       | V <sub>DD</sub>              |       | -4.2  | V <sub>DD</sub>                |       | +0.8 |   | V    |
| Input POR, Logic "1"              | -3.0                         |       | +0.3  | +2.0                           |       | +5.3 |   | V    |
| Input POR, Logic "0"              | V <sub>DD</sub>              |       | -10.0 | V <sub>DD</sub>                |       | -5.0 |   | V    |
| Output Digit and Segment Strobes  |                              |       |       |                                |       |      |   |      |
| Driver On                         |                              |       |       |                                |       |      |   |      |
| Commercial                        |                              |       | -1.5  |                                |       | +3.5 | At 10 mA                                    | V    |
| Industrial                        |                              |       | -1.7  |                                |       | +3.3 |   | V    |
| Driver Off 109X7-40               |                              |       | -40   |                                |       | -35  | Actual value determined by external circuit | V    |
| Driver Off 109X7-50               |                              |       | -50   |                                |       | -45  |   | V    |
| Output Leakage                    |                              |       | 10    |                                |       | 10   | Per driver when driver is off               | μA   |
| Input Leakage                     |                              |       | 10    |                                |       | 10   |   | μA   |

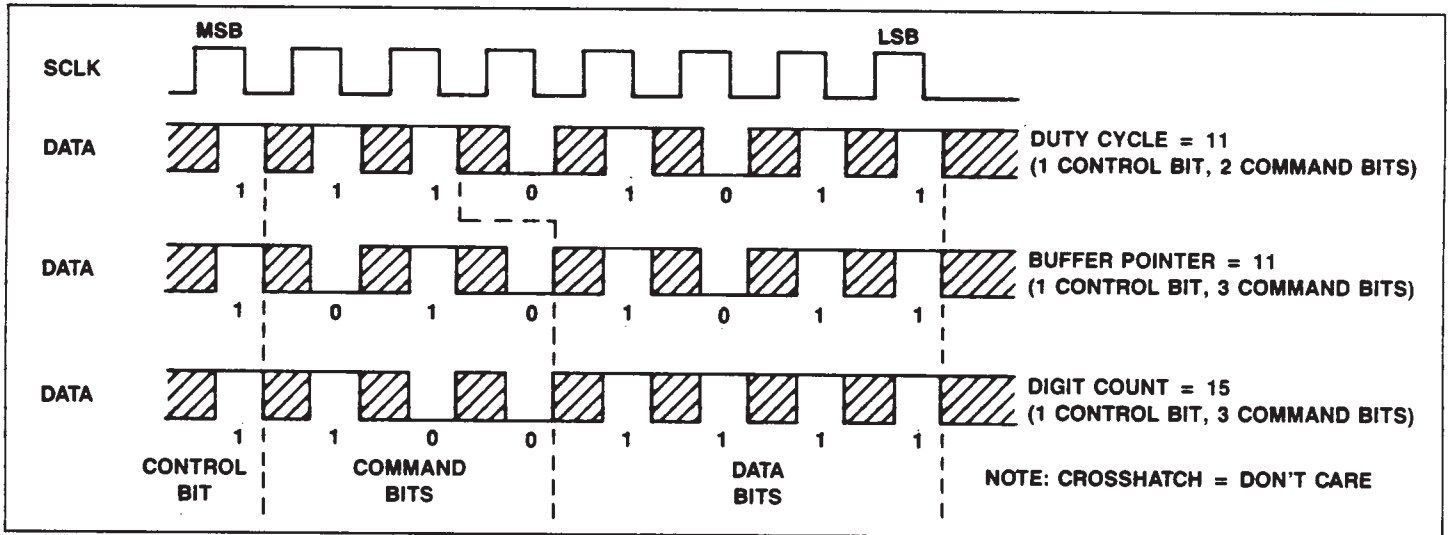
Notes: All outputs require pulldown resistors. X = 3 or 5 depending on device.

AC CHARACTERISTICS

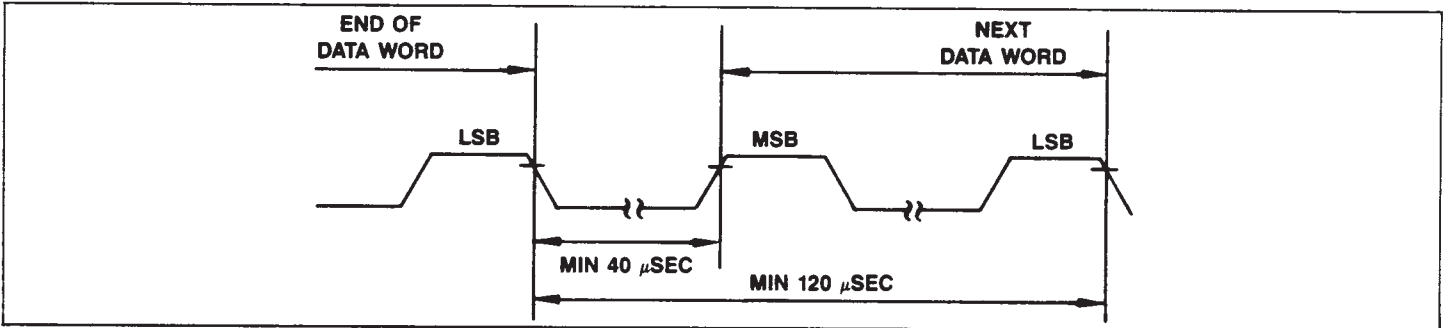
| Parameter              | Symbol            | Min | Typ | Max  | Unit |
|------------------------|-------------------|-----|-----|------|------|
| SCLK Clock             |                   |     |     |      |      |
| On Time                | T <sub>on</sub>   | 1.0 |     | 20.0 | μs   |
| Off Time               | T <sub>off</sub>  | 1.0 |     |      | μs   |
| Data Input Sample Time |                   |     |     |      |      |
| Before SCLK Clock Off  | T <sub>boff</sub> | 200 |     |      | ns   |
| After SCLK Clock Off   | T <sub>aoff</sub> | 100 |     |      | ns   |



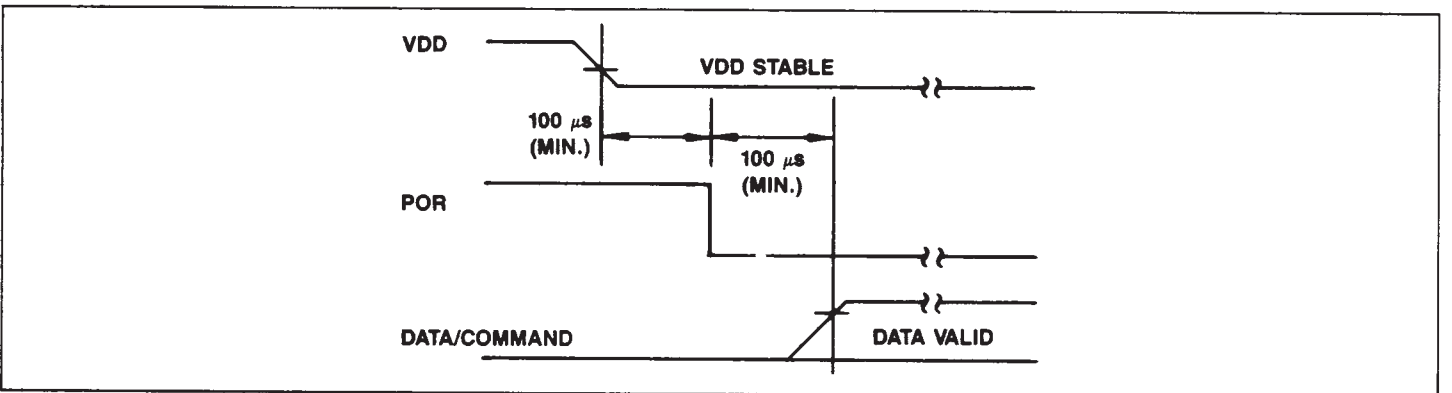
SCLK and Serial Data Timing



SCLK and Serial Data (Control Word) Examples



Data Word LSB/MSB Timing



Power-On Reset Timing

## FUNCTIONAL DESCRIPTION

The 10937 or 10957 is a general purpose display controller for multiplexed, segmented displays with up to 16 character positions and 14 or 16 segments, plus decimal point and comma tail. No external drive circuitry is needed for displays requiring up to 20 ma of drive current up to 50 volts. All timing signals required to control the display are generated in the 10937 or 10957 device without any refresh input from the host processor.

Input data is loaded into the Display Data Buffer via the Serial Data Input (Data) channel. Internal timing and control blocks synchronize the segment and digit output signals to provide the proper timing for the multiplexing operation. A 16 × 64-bit PLA is provided for segment decoding for the full ASCII character set (upper case only).

Input data is loaded into the 10937 or 10957 ADC as a series of 8-bit words with the most significant bit (MSB), bit 7, first. If bit 7 of any word loaded is a logic 1 (this bit is referred to as the control bit C), the loaded word is a control data word. If the C bit of any word is a logic 0, the loaded word is a display data word. The following paragraphs describe the format and functions of these control and display data words.

### INPUT CONTROL DATA WORDS

When the C-Bit (bit 7) of the 8-bit input word is a logic 1, bits 5 and 6 are decoded into one of four control commands while data associated with the command are extracted from bits 0 – 4 (see Table 1). The four control codes perform the following display functions:

- Load the Display Data Buffer pointer,
- Load the Digit Counter,
- Load the Duty Cycle register,
- Enable the Test Mode.

Table 1 lists the control codes and their functions.

### Buffer Pointer Control

The Buffer Pointer Control code allows the Display Data Buffer pointer to be set to any digit position so that individual characters may be modified. The Buffer Pointer is loaded with a decimal equivalent value 2 less than the desired value (i.e., to point to the digit controlled by AD6 of the display, a value of 4 is entered). See Table 2 for a complete list of the Buffer Pointer values.

Table 2. Buffer Pointer Control Codes

| Hex Code | Pointer Value | Character Controlled By |
|----------|---------------|-------------------------|
| A0       | 0             | AD2                     |
| A1       | 1             | AD3                     |
| A2       | 2             | AD4                     |
| A3       | 3             | AD5                     |
| A4       | 4             | AD6                     |
| A5       | 5             | AD7                     |
| A6       | 6             | AD8                     |
| A7       | 7             | AD9                     |
| A8       | 8             | AD10                    |
| A9       | 9             | AD11                    |
| AA       | 10            | AD12                    |
| AB       | 11            | AD13                    |
| AC       | 12            | AD14                    |
| AD       | 13            | AD15                    |
| AE       | 14            | AD16                    |
| AF       | 15            | AD1                     |

### Digit Counter Control

The Digit Counter Control code is normally used only during initialization routines to define the number of character positions to be controlled. This code maximizes the duty cycle for any display. If 16 characters are to be controlled, enter a value of 0 (zero). Otherwise, enter the value desired.

### Duty Cycle Control

The Duty Cycle Control code is used to turn the display on and off, and to adjust display brightness. As shown in the block diagram, the time slot for each character is 32 clock cycles. The segment and digit drivers for each character are on for a maximum of 31 cycles with a 1 cycle inter-digit off-time. The Duty Cycle Control code contains a 5-bit numeric field which modifies the on-time for the driver outputs from 0 to 31 cycles. A duty cycle of 0 puts both the segment and digit drivers into the off state.

### Test Mode Enable

The Test Mode Enable code is a device test function only. If executed, it will lock the device in the Test Mode. Once locked in, the device can only be removed from Test Mode by performing a power-on reset.

If this mode is activated, the digit time is reduced from 32 to 4 clock cycles to speed up the output driver sequencing time for ease in testing.

### INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit ASCII format codes. The 64 codes available (with the C-bit set to 0 to indicate a display data word) are shown in Table 3 with their corresponding ASCII characters.

Table 1. Control Data Words

| 8-Bit Control Word  |                         | Function  |
|---|-------------------------|---|
| C-Bit (Bit 7)   | 7-Bit Code (Bits 6 – 0) |   |
| 1   | 010NNNN <sup>(1)</sup>  | BUFFER POINTER CONTROL (Position of character to be changed)<br>DIGIT COUNTER CONTROL (Number of characters to be output)<br>DUTY CYCLE CONTROL (On/off and brightness control)<br>TEST MODE ENABLE (Not a user function) |
| 1   | 100NNNN <sup>(1)</sup>  |   |
| 1   | 11NNNNN <sup>(2)</sup>  |   |
| 1   | 00NNNNN <sup>(3)</sup>  |   |
| <b>Notes:</b> 1. NNNN is a 4-bit binary value representing the digit number to be loaded.<br>2. NNNNN is a 5-bit binary value representing the number of clock cycles each digit is on. |                         | 3. This code is a device test function only. If executed it will lock the device in the test mode. Once locked in, the device can only be removed from Test Mode by performing a power-on reset.                          |

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented before each data word is stored in the Display Buffer except for decimal point and comma words. These do not cause the Buffer Pointer to increment and thus are always associated with the previous character entered. To select the next character

position to be loaded out of the normal sequence, use the Buffer Pointer Control command before entering the display data word. It is not necessary to use the Buffer Pointer Control command to cycle back to position 1 when less than 16 character positions are being used.

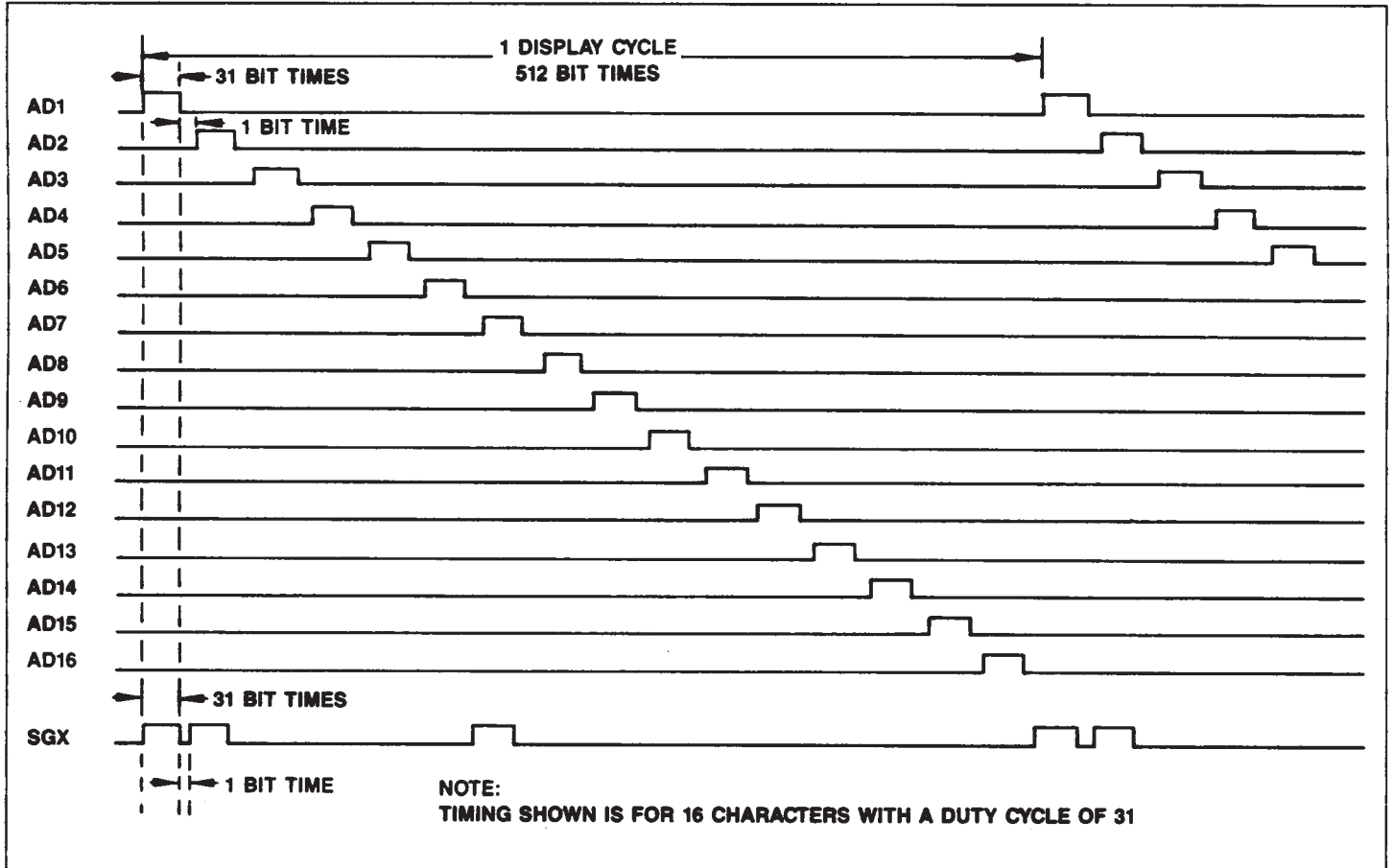


Figure 1. Display Scan Timing Diagram (Duty Cycle)

Table 3. Character Assignments for Display Data Words

| DATA WORD |     | CHARACTER | DATA WORD |     | CHARACTER | DATA WORD |     | CHARACTER | DATA WORD |     | CHARACTER |
|-----------|-----|-----------|-----------|-----|-----------|-----------|-----|-----------|-----------|-----|-----------|
| BINARY    | HEX |           | BINARY    | HEX |           | BINARY    | HEX |           | BINARY    | HEX |           |
| 0X000000  | 00  | @         | 0X010000  | 10  | P         | 0X100000  | 20  |           | 0X110000  | 30  | 0         |
| 0X000001  | 01  | A         | 0X010001  | 11  | Q         | 0X100001  | 21  | !         | 0X110001  | 31  | 1         |
| 0X000010  | 02  | B         | 0X010010  | 12  | R         | 0X100010  | 22  | "         | 0X110010  | 32  | 2         |
| 0X000011  | 03  | C         | 0X010011  | 13  | S         | 0X100011  | 23  | #         | 0X110011  | 33  | 3         |
| 0X000100  | 04  | D         | 0X010100  | 14  | T         | 0X100100  | 24  | \$        | 0X110100  | 34  | 4         |
| 0X000101  | 05  | E         | 0X010101  | 15  | U         | 0X100101  | 25  | %         | 0X110101  | 35  | 5         |
| 0X000110  | 06  | F         | 0X010110  | 16  | V         | 0X100110  | 26  | &         | 0X110110  | 36  | 6         |
| 0X000111  | 07  | G         | 0X010111  | 17  | W         | 0X100111  | 27  | '         | 0X110111  | 37  | 7         |
| 0X001000  | 08  | H         | 0X011000  | 18  | X         | 0X101000  | 28  | (         | 0X111000  | 38  | 8         |
| 0X001001  | 09  | I         | 0X011001  | 19  | Y         | 0X101001  | 29  | )         | 0X111001  | 39  | 9         |
| 0X001010  | 0A  | J         | 0X011010  | 1A  | Z         | 0X101010  | 2A  | *         | 0X111010  | 3A  | ::        |
| 0X001011  | 0B  | K         | 0X011011  | 1B  | [         | 0X101011  | 2B  | +         | 0X111011  | 3B  | ::        |
| 0X001100  | 0C  | L         | 0X011100  | 1C  | /         | 0X101100  | 2C  | '         | 0X111100  | 3C  | <         |
| 0X001101  | 0D  | M         | 0X011101  | 1D  | ]         | 0X101101  | 2D  | -         | 0X111101  | 3D  | =         |
| 0X001110  | 0E  | N         | 0X011110  | 1E  |           | 0X101110  | 2E  | .         | 0X111110  | 3E  | >         |
| 0X001111  | 0F  | O         | 0X011111  | 1F  | -         | 0X101111  | 2F  | \         | 0X111111  | 3F  | ?         |

Note: X means this bit (bit 7) is a "don't care" bit except for PNT and TAIL on 10957 only. The hex codes shown assume bit 7 is a zero.

**POWER-ON RESET (POR)**

The Power-On Reset (POR) initializes the internal circuits of the 10937 or 10957 ADC when power ( $V_{DD}$ ) is applied. The following conditions are established after a Power-On Reset:

- a. The Digit Drivers (AD1-AD16) are in the off state (floating).
- b. The Segment Drivers (SGA-SGP) are in the off state (floating). This includes PNT and TAIL.
- c. The Duty Cycle is set to 0.
- d. The Digit Counter is set to 16 (a bit code value of 0).
- e. The Buffer Pointer points to the character controlled by AD1.

**DIGIT DRIVERS (AD1-AD16)**

The sixteen Digit Drivers (AD1 – AD16) are used to select each of the display digits sequentially during a refresh scan. Display segments will be illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The timing characteristics of both the digits and segments are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

**Table 4. Comparison of 10957 with 10937**

| Input Data | 10937 Character | 10957 Character |
|------------|-----------------|-----------------|
| 2C         | ;               | ;               |
| 2E         | .               | .               |
| 6C         | ;               | .               |
| 6E         | .               | ,               |

**SEGMENT DRIVERS (SGA-SGP)**

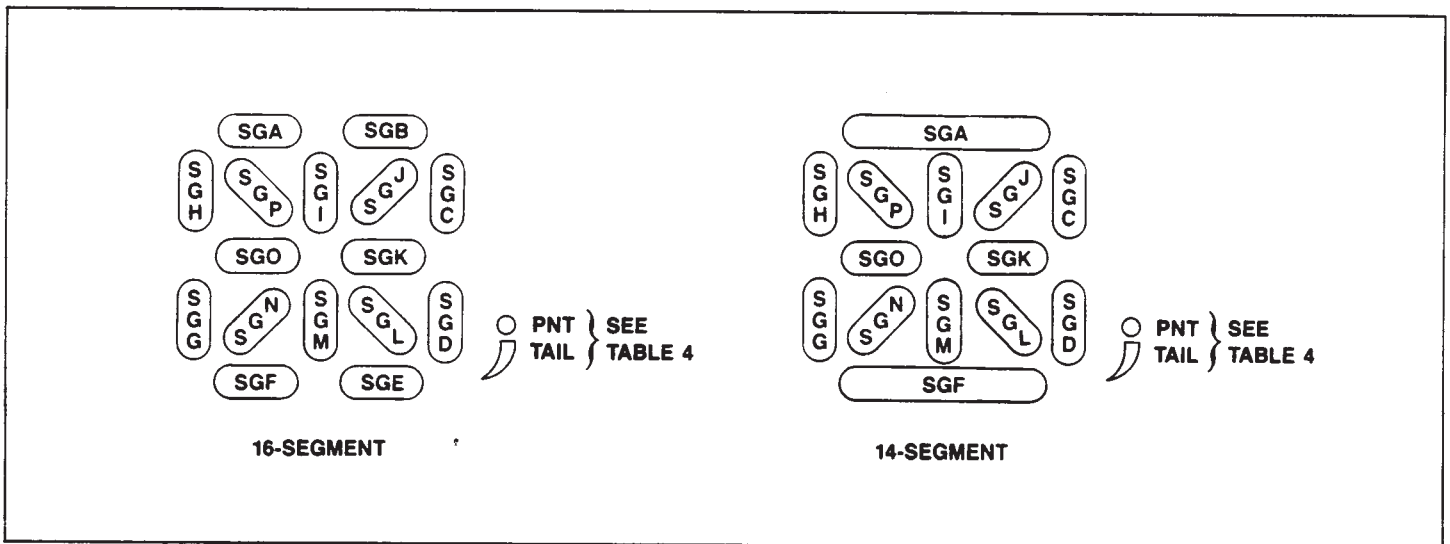
Sixteen (16) Segment Drivers are provided (SGA – SGP), plus the decimal point (PNT) and comma tail (TAIL). The segment outputs are internally decoded from the 8-bit characters in the Display Data Buffer by means of a 64 × 16-bit PLA. The Segment Driver Allocations are shown in Figure 2. Data codes and their corresponding segment patterns are shown in Figure 3. Timing characteristics for the segment outputs are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

**NOTE**

For 14-segment displays, SGA is used for the top segment and SGF is used for the bottom segment. SGB and SGE can be floated.

**TYPICAL SYSTEM HOOK-UP**

Figure 4 shows the 10937 or 10957 as it would be connected to a V-F display when driven by a host system.  $E_k$  is determined by the V-F display specifications and  $R_C$  is selected to provide proper biasing current for zeners. Pull down resistors  $R_A$  and  $R_G$  are determined by the interconnection capacitance between the device and the display.



**Figure 2. Segment Driver Allocations**

|    |  |    |  |    |  |    |  |    |  |    |  |    |  |    |  |
|----|--|----|--|----|--|----|--|----|--|----|--|----|--|----|--|
| 00 |  | 08 |  | 10 |  | 18 |  | 20 |  | 28 |  | 30 |  | 38 |  |
| 01 |  | 09 |  | 11 |  | 19 |  | 21 |  | 29 |  | 31 |  | 39 |  |
| 02 |  | 0A |  | 12 |  | 1A |  | 22 |  | 2A |  | 32 |  | 3A |  |
| 03 |  | 0B |  | 13 |  | 1B |  | 23 |  | 2B |  | 33 |  | 3B |  |
| 04 |  | 0C |  | 14 |  | 1C |  | 24 |  | 2C |  | 34 |  | 3C |  |
| 05 |  | 0D |  | 15 |  | 1D |  | 25 |  | 2D |  | 35 |  | 3D |  |
| 06 |  | 0E |  | 16 |  | 1E |  | 26 |  | 2E |  | 36 |  | 3E |  |
| 07 |  | 0F |  | 17 |  | 1F |  | 27 |  | 2F |  | 37 |  | 3F |  |

16-Segment Display

|    |  |    |  |    |  |    |  |    |  |    |  |    |  |    |  |
|----|--|----|--|----|--|----|--|----|--|----|--|----|--|----|--|
| 00 |  | 08 |  | 10 |  | 18 |  | 20 |  | 28 |  | 30 |  | 38 |  |
| 01 |  | 09 |  | 11 |  | 19 |  | 21 |  | 29 |  | 31 |  | 39 |  |
| 02 |  | 0A |  | 12 |  | 1A |  | 22 |  | 2A |  | 32 |  | 3A |  |
| 03 |  | 0B |  | 13 |  | 1B |  | 23 |  | 2B |  | 33 |  | 3B |  |
| 04 |  | 0C |  | 14 |  | 1C |  | 24 |  | 2C |  | 34 |  | 3C |  |
| 05 |  | 0D |  | 15 |  | 1D |  | 25 |  | 2D |  | 35 |  | 3D |  |
| 06 |  | 0E |  | 16 |  | 1E |  | 26 |  | 2E |  | 36 |  | 3E |  |
| 07 |  | 0F |  | 17 |  | 1F |  | 27 |  | 2F |  | 37 |  | 3F |  |

14-Segment Display

Notes: Bit 7 of the data byte is a "don't care" bit except for PNT and TAIL on 10957. Data byte hex codes shown assume bit 7 is a zero.  
 \* = 10957 only.

Figure 3. Display Segment Driver Character Patterns

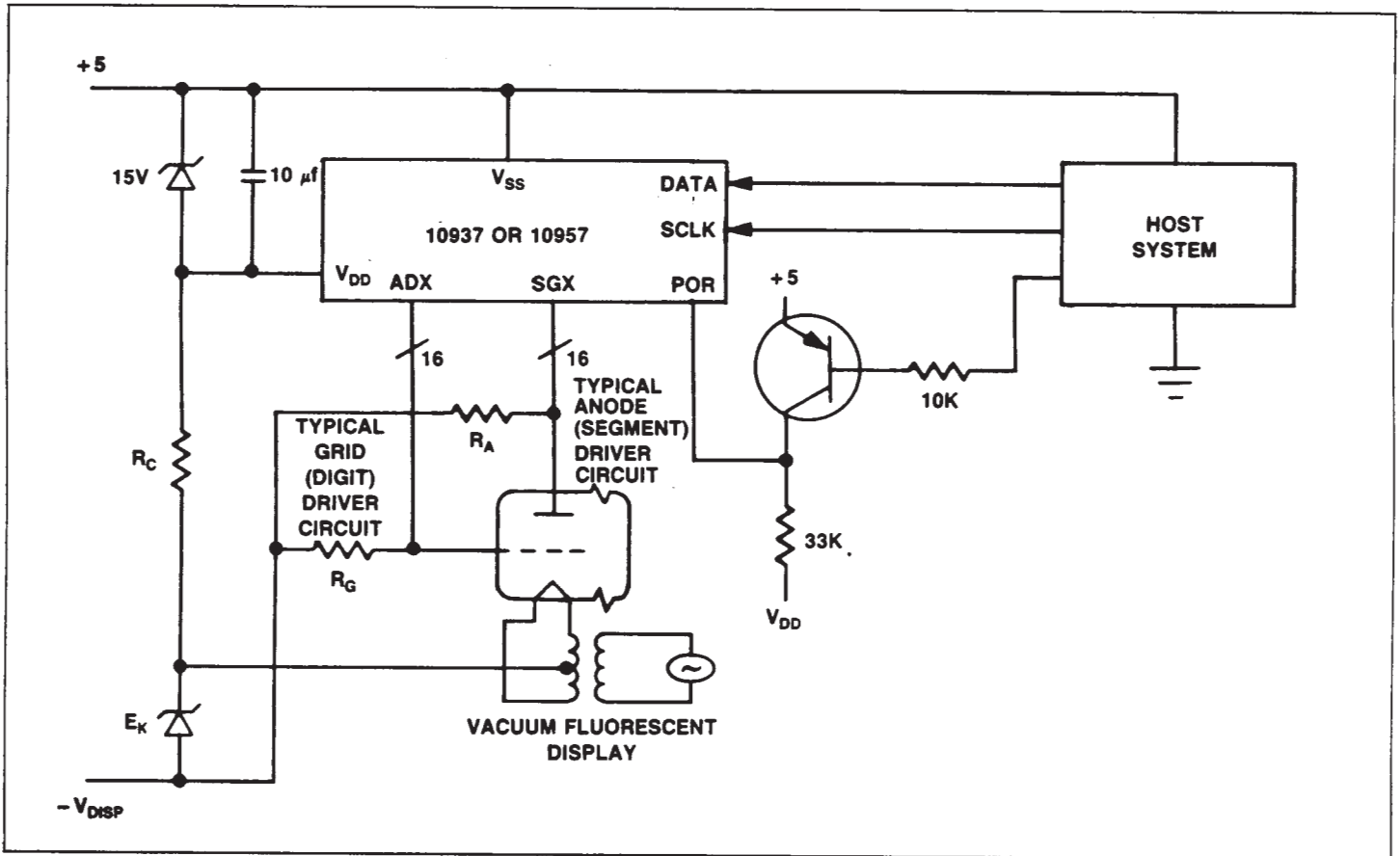


Figure 4. Partial System Schematic

10937 AND 10957 44-PIN PLCC PIN ASSIGNMENTS

| Pin | Function  | Pin | Function     |
|-----|-----------|-----|--------------|
| 1   | VSS (GND) | 23  | PO (VGST)    |
| 2   | AD16      | 24  | DATA         |
| 3   | AD15      | 25  | SCLK (BVDSS) |
| 4   | AD14      | 26  | SGA          |
| 5   | AD13      | 27  | SGB          |
| 6   | NC        | 28  | SGC          |
| 7   | NC        | 29  | NC           |
| 8   | AD12      | 30  | SGD          |
| 9   | AD11      | 31  | SGE          |
| 10  | AD10      | 32  | SGF          |
| 11  | AD09      | 33  | SGG          |
| 12  | AD08      | 34  | SGH          |
| 13  | AD07      | 35  | S GI         |
| 14  | AD06      | 36  | SGJ          |
| 15  | AD05      | 37  | SGK          |
| 16  | AD04      | 38  | SGL          |
| 17  | AD03      | 39  | SGM          |
| 18  | AD02      | 40  | SGN          |
| 19  | NC        | 41  | SGO          |
| 20  | AD01      | 42  | SGP          |
| 21  | VDD       | 43  | TAIL         |
| 22  | A         | 44  | PNT          |

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