MT9042

Global Digital Trunk Synchronizer

Preliminary Information

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Features

- Provides T1 and E1 clocks, and ST-BUS/GCI framing signals locked to an input reference of either 8 kHz (frame pulse), 1.544 MHz (T1), or 2.048 MHz (E1)
- Meets AT & T TR62411 and ETSI ETS 300 011 specifications for a 1.544 MHz (T1), or 2.048 MHz (E1) input reference
- Provides Time Interval Error (TIE) correction to suppress input reference rearrangement transients
- Typical unfiltered intrinsic output jitter is 0.013 UI peak-to-peak
- Jitter attenuation of 15 dB @ 10 Hz, 34 dB @ 100 Hz and 50 dB @ 5 to 40 kHz
- Low power CMOS technology

Applications

- Synchronization and timing control for T1 and E1 digital transmission links
- ST-BUS clock and frame pulse sources
- Primary Trunk Rate Converters

Ordering Information	
MT9042AP	28 Pin PLCC
-40°C to +85°C	

Description

The MT9042 is a digital phase-locked loop (PLL) designed to provide timing and synchronization signals for T1 and E1 primary rate transmission links that are compatible with ST-BUS/GCI frame alignment timing requirements. The PLL outputs can be synchronized to either a 2.048 MHz, 1.544 MHz, or 8 kHz reference. The T1 and E1 outputs are fully compliant with AT & T TR62411 (ACCUNET® T1.5) and ETSI ETS 300 011 intrinsic jitter and jitter transfer specifications, respectively, when synchronized to primary reference input clock rates of either 1.544 MHz or 2.048 MHz.

The PLL also provides additional high speed output clocks at rates of 3.088 MHz, 4.096 MHz, 8.192 MHz, and 16.384 MHz for backplane synchronization.

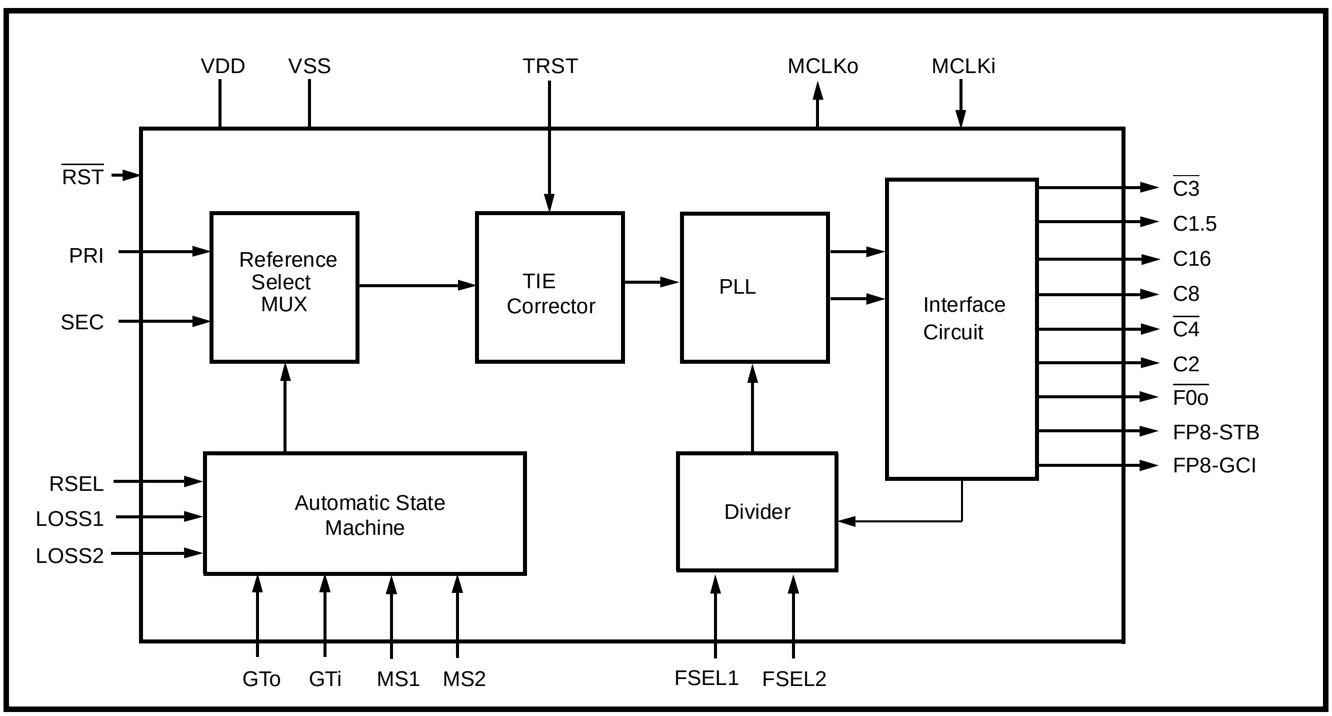

Figure 1 - Functional Block Diagram

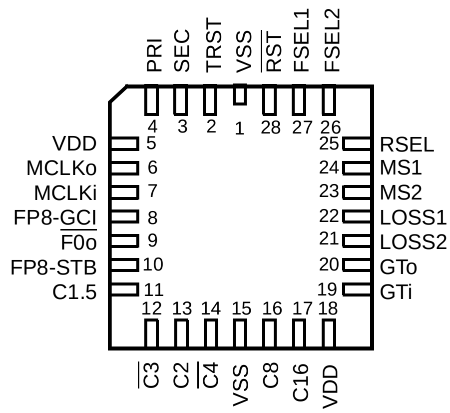

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	V_{SS}	**Negative Power Supply Voltage.** Nominally 0 Volts.
2	TRST	**TIE Circuit Reset (TTL compatible).** When HIGH, the time interval error correction circuit is alternately establishing the phase difference between the PRI and SEC reference inputs, depending upon which input is selected as input for PLL synchronization. This information is used to generate a virtual reference for input to the PLL. When LOW, the time interval error correction circuit is bypassed.
3	SEC	**Secondary Reference Input (TTL compatible).** This input (either 8 kHz, 1.544 MHz, or 2.048 MHz as controlled by the input frequency selection pins) is used as an alternate reference source for PLL synchronization.
4	PRI	**Primary Reference Input (TTL compatible).** This input (either 8 kHz, 1.544 MHz, or 2.048 MHz as controlled by the input frequency selection pins) is used as the primary reference source for PLL synchronization.
5	V_{DD}	**Positive Supply Voltage.** Nominally +5 volts.
6	MCLKo	**Master Clock Oscillator Output.** This is a CMOS buffered output used for driving a 20 MHz crystal.
7	MCLKi	**Master Clock Oscillator Input.** This is a CMOS input for a 20 MHz crystal or crystal oscillator. Signals should be DC coupled to this pin.
8	FP8-GCI	**Frame Pulse Output (CMOS compatible).** This is an 8 kHz output framing pulse that indicates the start of the active GCI-BUS frame. The pulse width is based upon the period of the 8.192 MHz synchronization clock.
9	$\overline{\text{F0o}}$	**Frame Pulse Output (CMOS compatible).** This is an 8 kHz output framing pulse that indicates the start of the active ST-BUS frame. The pulse width is based upon the period of the 4.096 MHz synchronization clock. This is an active low signal.
10	FP8-STB	**Frame Pulse Output (CMOS compatible).** This is an 8 kHz output framing pulse that indicates the start of the active ST-BUS frame. The pulse width is based upon the period of the 8.192 MHz synchronization clock.
11	C1.5	**Clock 1.544 MHz (CMOS compatible).** This ouput is a 1.544 MHz (T1) output clock locked to the selected reference input signal.
12	$\overline{\text{C3}}$	**Clock 3.088 MHz (CMOS compatible).** This output is a 3.088 MHz output clock locked to the selected reference input signal.

Pin Description (continued)

Pin #	Name	Description
13	C2	**Clock 2.048 MHz (CMOS compatible).** This output is a 2.048 MHz (E1) output clock locked to the selected reference input signal.
14	$\overline{C4}$	**Clock 4.096 MHz (CMOS compatible).** This output is a 4.096 MHz output clock locked to the selected reference input signal.
15	V_{SS}	**Negative Power Supply Voltage.** Nominally 0 Volts.
16	C8	**Clock 8.192 MHz (CMOS compatible).** This output is an 8.192 MHz output clock locked to the selected reference input signal.
17	C16	**Clock 16.384 MHz (CMOS compatible).** This output is a 16.384 MHz output clock locked to the selected reference input signal.
18	V_{DD}	**Positive Supply Voltage.** Nominally +5 volts.
19	GTi	**Guard Time Input (TTL Level Schmitt Trigger).** This TTL level Schmitt trigger input is used to determine the threshold level of the RC generated (guard) time constant. This function filters out unwanted rearrangements between the PRI and SEC reference input signals.
20	GTo	**Guard Time Output (CMOS compatible).** This is a CMOS buffered output used to drive the external RC generated (guard) time constant circuit.
21	LOSS2	**Reference Loss Indicator - 2 Input (TTL compatible).** This input, in conjunction with LOSS1, comprises a set of signals which control the event driven state machine when the PLL is operating in AUTOMATIC mode (see Table 4).
22	LOSS1	**Reference Loss Indicator - 1 Input (TTL compatible).** This input, in conjunction with LOSS2, comprises a set of signals which control the event driven state machine when the PLL is operating in AUTOMATIC mode (see Table 4).
23	MS2	**Mode Select - 2 Input (TTL compatible).** This input, in conjunction with MS1, selects the PLL mode of operation (i.e.,NORMAL, HOLDOVER, FREERUN, or AUTOMATIC; see Table 1).
24	MS1	**Mode Select - 1 Input (TTL compatible).** This input, in conjunction with MS2, selects the PLL mode of operation (i.e., NORMAL, HOLDOVER, FREERUN, or AUTOMATIC; see Table 1).
25	RSEL	**Input Reference Select (TTL compatible).** When LOW this input selects PRI as the reference input signal, and when HIGH, selects SEC as the reference input signal (see Table 2).
26	FSEL2	**Frequency Select - 2 Input (TTL compatible).** This input, in conjunction with FSEL1, selects the frequency of the input reference source (i.e., 8 kHz, 1.544 MHz, or 2.048 MHz; see Table 3).
27	FSEL1	**Frequency Select - 1 Input (TTL compatible).** This input, in conjunction with FSEL2, selects the frequency of the input reference source (i.e., 8 kHz, 1.544 MHz, or 2.048 MHz; see Table 3).
28	$\overline{RST}$	**Reset (TTL compatible).** This input (active LOW) puts the MT9042 in its reset state. To guarantee proper operation, the device must be reset after power-up. The time constant for a power-up reset circuit must be a minimum of five times the rise time of the power supply. In normal operation, the $\overline{RST}$ pin must be held low for a minimum of 60 nsec to reset the device.

Functional Description

The MT9042 is a fully digital, phase-locked loop designed to provide timing references to interface circuits for T1 and E1 Primary Rate Digital Transmission links. As shown in Figure 1, the PLL consists of an input reference selection circuit (MUX), a Time Interval Error corrector (TIE), and a PLL that employs a high resolution Digitally Controlled Oscillator (DCO) to generate the T1 and E1 outputs.

The MT9042 accepts two reference clock inputs, primary (PRI) and secondary (SEC) both connected to independent external reference sources, either of which can be selected as reference for synchronization by the reference select (RSEL) input. The selected reference signal is then regenerated by the TIE correction circuit and passed as a virtual reference to the PLL. The TIE correction circuit will limit phase jumps (as specified by AT & T TR62411 and ETSI ETS 300 011) during rearrangement between the external reference clocks. This virtual reference is then used by the PLL for synchronizing the output signals.

The interface circuit on the output of the DCO generates 1.544 MHz (C1.5), 3.088 MHz (C3), 2.048 MHz (C2), 4.096 MHz (C4), 8.192 MHz (C8), 16.384 MHz (C16), and three 8 kHz frame pulses F0o, FP8-STB, and FP8-GCI.

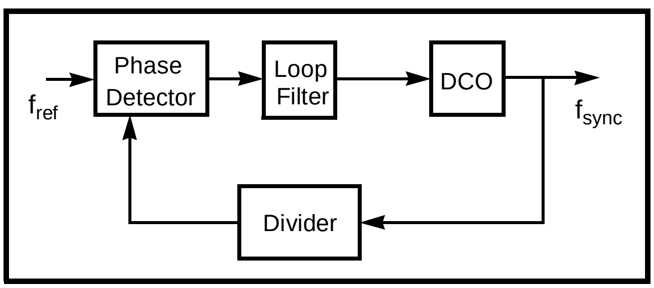

Figure 3 - PLL Block Diagram

As shown in Figure 3, the PLL of the MT9042 consists of a phase detector (PD), a loop filter, a high resolution DCO, and a digital frequency divider. The digitally controlled oscillator (DCO) is locked in frequency (n x f_{ref}) to one of three possible reference frequencies, configured using pins FSEL1 and FSEL2. Combined with the reference select input RSEL, the PLL is capable of providing a full range of E1/T1 clock signals synchronized to either the primary PRI or secondary SEC input. The loop filter is a first order lowpass structure that provides approximately a 2 Hz bandwidth.

Modes of Operation

The MT9042 can operate in one of two modes, MANUAL or AUTOMATIC, as controlled by mode select pins MS1 and MS2 (see Table 1). In MANUAL mode, the user is responsible for switching references during NORMAL operation, as well as forcing the PLL into FREERUN or HOLDOVER states.

When AUTOMATIC mode is selected, operation is controlled by an internal state machine. Under state machine control, input reference selection is automatically based upon the input levels of LOSS1 and LOSS2.

MS2	MS1	Description of Operation
0	0	NORMAL (manual mode)
0	1	HOLDOVER (manual mode)
1	0	FREERUN (manual mode)
1	1	AUTOMATIC MODE

Table 3- Operating Modes of the MT9042

Manual Mode

In MANUAL mode operation, the input reference selection is accomplished through a 2-to-1 multiplexer, which is controlled by the RSEL input pin. As shown in Table 2, for MANUAL mode operation RSEL=0 selects PRI as the primary reference input, while RSEL=1 selects SEC as the primary reference input.

Mode	RSEL	Reference Input Selected
Manual	0	PRI
Manual	1	SEC
Automatic	0	state machine control
Automatic	1	state machine control, but treats SEC as primary and PRI as secondary

Table 4- Reference Input Selection of the MT9042

There are three possible input frequencies for selection as the primary reference clock. These are 8 kHz, 1.544 MHz or 2.048 MHz. Frequency selection is controlled by the logic levels of FSEL1 and FSEL2, as shown in Table 3. This variety of input frequencies was chosen to allow the generation of all the necessary T1 and E1 clocks from either a T1, E1 or frame pulse reference source.

Automatic Mode

In normal AUTOMATIC mode operation, the RSEL input is set to 0. This will allow the state machine to control PLL operation and select the reference input based on the state of the LOSS1 and LOSS2 inputs (see state transitions in Table 4). If the PRI reference signal is lost (LOSS1 = HIGH, LOSS2 = LOW), then the PLL will enter HOLDOVER mode immediately and stay there for a time determined by the RC time constant connected to the Guard Time input (GTi, GTo).

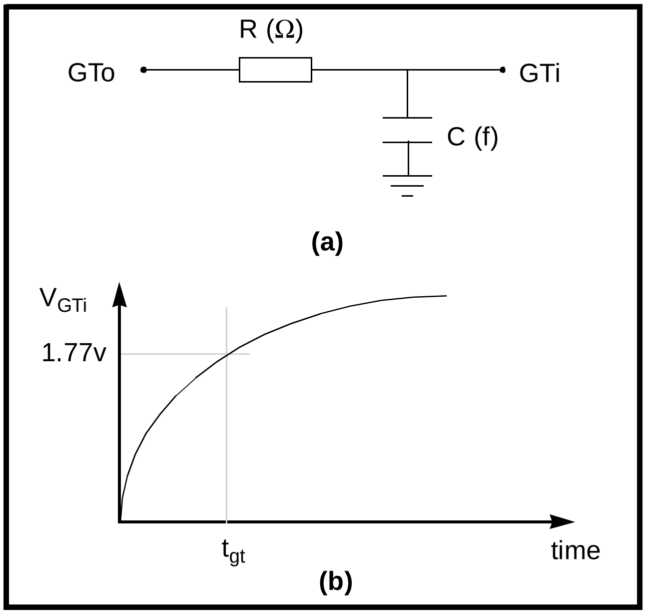

Figure 4 - a) RC circuit for guard time, b) exponential waveform on GTi

When the primary reference signal has not been regained and the guard time has been exceeded, the reference will be switched to SEC. The time constant determined by the RC circuit connected to the GTi input provides the hysteresis on automatic switching between PRI and SEC during very short interruptions of the primary reference signal. The Guard Time, t_{gt}, can be predicted using the step response of an RC network. The capacitor voltage on the RC circuit is described by an exponential curve. When the capacitor voltage reaches the positive going threshold of GTi (typically 1.77 volts for Schmitt trigger TTL inputs, see Figure 4) a logic HIGH level results. This causes the state machine to move from the holdover state of PRI to the state of using SEC as the input reference. The following equation can be used to determine the Guard Time t_{gt}:

$$t_{gt} = -RC\ln\left(\frac{V_{dd} - 1.77}{V_{dd}}\right)$$

The state machine will continue to monitor the LOSS1 input and will switch back to the PRI reference once the primary reference becomes functional as indicated by the LOSS1 input. A logic level HIGH on both the LOSS1 or LOSS2 inputs indicates that none of the external references are available. Under these circumstances, the PLL will be switched into the HOLDOVER state (within a specified rate of frame slip) until a fully functional reference input is available.

FSEL 2	FSEL 1	Input Reference Frequency
0	0	Reserved
0	1	8 kHz
1	0	1.544 MHz
1	1	2.048 MHz

Table 5 - Input Frequency Selection of the MT9042

Time Interval Error Correction Circuit (TIE)

The TIE correction circuit generates a virtual input synchronized to the selected primary input reference. After a reference rearrangement the TIE corrects the phase of this new reference in such a way that the virtual input preserves its phase. In other words, reference switching will not create significant phase changes on the virtual input, and therefore, the outputs of the PLL.

The TIE reset (TRST) aligns the falling edge of the current input with the falling edge of the primary input reference. When TRST is held LOW for at least 100 ns, the next falling edge of the reference input becomes aligned and passes through the TIE circuit without additional delay.

PLL Measures of Performance

To meet the requirements of AT & T TR62411 and ETSI 300 011, the following PLL performance parameters were measured:

- locking range and lock time
- slip rate in holdover mode
- free-run accuracy
- maximum time interval error and slope
- intrinsic jitter
- jitter transfer function
- output jitter spectrum
- wander

Description	Freerun	Normal (PRI)	Normal (SEC)	Holdover (PRI)	Holdover (SEC)
State	**P1**	**P2**	**P3**	**P4a**	**P4b**
Power On (RST=0 LOSS1=X LOSS2=X)	No change	Invalid state	Invalid state	Invalid state	Invalid state
LOSS1=0 LOSS2=0	P2	No change	P2	P2	P2
LOSS1=1 LOSS2=0 time loss < tgt	P3	P4a ST.GD	No change	No change	P3
LOSS1=1 LOSS2=0 time loss > tgt	P3	Invalid state	No change	P3	P3
LOSS1=0 LOSS2=1	P2	No change	P2	P2	P2
LOSS1=1 LOSS2=1	No change	P4a	P4b	No change	No change
Where : ST.GD = Start guard time; X = Don’t care					

Table 4 - State Table For Automatic Input Reference Selection and Operating Mode

Locking Range and Lock Time

The locking range of the PLL is the range that the input reference frequency can be deviated from its nominal frequency while the output signals maintain synchronization. The relevant value is usually specified in parts-per-million (ppm). For both the T1 and E1 outputs, lock was maintained while an 8 kHz input was varied between 7900 Hz to 8100 Hz (corresponding to ±12500 ppm). This is well beyond the required ±100 ppm. The lock range of 12500 ppm also applies to 1.544 MHz and 2.048 MHz reference inputs.

The lock time is a measure of how long it takes the PLL to reach steady state frequency after a frequency step on the reference input signal. The locking time is measured by applying an 8000 Hz signal to the primary reference and an 8000.8 Hz (+100 ppm) to the secondary reference. The output is monitored with a time interval analyzer during slow periodic rearrangements on the reference inputs.

The lock time for both the T1 and E1 outputs is approximately 311 ms, which is well below the required lock time of 1.0 seconds.

Holdover and Freerun Accuracy

The holdover option of the PLL provides the user with the capability of maintaining the integrity of output signals when the input reference signals are lost. Holdover performance is defined as the rate of slip (i.e., amount of slip on 60 seconds) of the 8 kHz reference input. For both the T1 and E1 outputs the rate of slip was measured as a function of the input reference frequency. The results measured over an observation period of 60 seconds, are presented in Table 5.

Reference Input Frequency	% of Frame Pulse Slip
8 kHz	8%
1.544 MHz	58%
2.048 Hz	58%

Table 5 - Holdover Slip Rate (60 seconds)

The freerun accuracy of the PLL is a measure of how accurately the PLL can reproduce the desired output frequency. The freerun accuracy is a function of master clock frequency which must be 20 MHz ±32 ppm in order to meet AT & T TR62411 and ETSI specifications.

Maximum Time Interval Error (MTIE)

MTIE is a measure of the rate of change of phase on the output signal due to a step in phase on the reference input. The specification also clearly indicates a peak constraint on the characteristic of the output signal. The specification is uniquely a function of the loop bandwidth (or loop delay) of the PLL. AT & T TR62411 clearly indicates that a maximum time interval error should not exceed 1µs. As well, during this transient response, the output signal shall not change its phase position in time faster than 81 ns per 1.326 ms observation period.

For the case where the PRI and SEC reference inputs are both at 8 kHz, but phase separated by 180° the maximum time interval recorded for input rearrangement is 320 ns. For a 45 degree separation of the reference inputs, an 85 Hz periodic rearrangement indicated a measured slope of 10ns per 1.326 ms observation period.

Jitter Performance

The output jitter of a digital trunk PLL is composed of intrinsic jitter, measured using a jitter free reference clock, and frequency dependent jitter, measured by applying known levels of jitter on the references clock. The jitter spectrum indicates the frequency content of the output jitter.

Intrinsic Jitter

Intrinsic jitter is the jitter added to an output signal by the processing device, in this case the enhanced PLL. Tables 6 and 7 show the average measured intrinsic jitter of the T1 and E1 outputs. Each measurement is an average based upon a ±100 ppm deviation (in steps of 20 ppm) on the input reference clock. Jitter on the master clock will increase intrinsic jitter of the device, hence attention to minimization of master clock jitter is required.

Jitter Transfer Function

The jitter transfer function is a measure of the transfer characteristics of the PLL to frequency specific jitter on the referenced input of the PLL. It is directly linked to the loop bandwidth and the magnitude of the phase error suppression characteristics of the PLL. It is measured by applying jitter of specific magnitude and frequencies to the input of the PLL, then measuring the magnitude of the output jitter (both filtered and unfiltered) on the T1 or E1 output.

Care must be taken when measuring the transfer characteristics to ensure that critical jitter alias frequencies are included in the measurement (i.e., for digital phase locked loops using an 8 kHz input).

Tables 8 and 9 provide measured results for the jitter transfer characteristics of the PLL for both a 1.544 MHz and 2.048 MHz reference input clock. The transfer characteristics for an 8 kHz reference input will be the same.

Figures 5 and 6 show the jitter attenuation performance of the T1 and E1 outputs plotted against AT & T TR62411 and ETSI requirements, respectively.

Output Jitter in UIp-p				
Reference Input	**FLT0 Unfiltered**	**FLT1 10Hz - 8kHz**	**FLT2 10Hz - 40kHz**	**FLT3 8kHz - 40kHz**
8 kHz	.011	.004	.006	.002
1.544 MHz	.011	.001	.002	.001
2.048 MHz	.011	.001	.002	.001

Table 6 -Typical Intrinsic Jitter for the T1 Output

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Output Jitter in UIp-p			
Reference Input	**FLT0 Unfiltered**	**FLT1 20Hz - 100kHz**	**FLT2 700Hz - 100kHz**
8 kHz	.011	.002	.002
1.544 MHz	.011	.002	.002
2.048 MHz	.011	.002	.002

Table 7 - Typical Intrinsic Jitter for the E1 Output

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Input Jitter Modulation Frequency (Hz)	Input Jitter Magnitude (UIp-p)	Measured Jitter Output (UIp-p)			
		T1 Reference Input		E1 Reference Input	
		Output Jitter Magnitude (UIp-p)	Jitter Attenuation (dB)	Output Jitter Magnitude (UIp-p)	Jitter Attenuation (dB)
10	20	2.42	18.34	2.41	18.38
20	20	1.62	21.83	1.618	21.84
40	20	.900	26.94	.908	26.86
100	20	.375	34.54	.376	34.52
330	10	.060	44.44	.060	44.44
500	8	.032	47.96	.032	47.96
1000	7	.015	53.38	.015	53.38
5000	0.8	.003	48.52	.003	48.52
7900	1.044	.003	50.83	.003	50.83
7950	1.044	.003	50.83	.003	50.83
7980	1.044	.003	50.83	.003	50.83
7999	1.044	.003	50.83	.003	50.83
8001	1.044	.003	50.83	.003	50.83
8020	1.044	.003	50.83	.003	50.83
8050	1.044	.003	50.83	.003	50.83
8100	1.044	.003	50.83	.003	50.83
10000	0.4	.003	42.50	.003	42.50

Table 8 - Typical Jitter Transfer Function for the T1 Output

Notes

1) For input jitter from 10 kHz to 100 kHz, the jitter attenuation is of such magnitude that intrinsic jitter dominates the output signal, rendering the jitter transfer function unmeasurable.

2) Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Input Jitter Modulation Frequency (Hz)	Input Jitter Magnitude (UIp-p)	Measured Jitter Output (UIp-p)			
		T1 Reference Input		E1 Reference Input	
		Output Jitter Magnitude (UIp-p)	Jitter Attenuation (dB)	Output Jitter Magnitude (UIp-p)	Jitter Attenuation (dB)
10	1.5	.355	12.52	.351	12.62
20	1.5	.186	18.13	.185	18.18
40	1.5	.095	23.97	.096	23.88
100	1.5	.039	31.70	.039	31.70
200	1.5	.021	37.08	.020	37.50
400	1.5	.012	41.94	.012	41.94
1000	1.5	.006	47.96	.007	46.62
7900*	1.044	.002	54.35	.002	54.35
7950*	1.044	.002	54.35	.002	54.35
7980*	1.044	.002	54.35	.002	54.35
7999*	1.044	.002	54.35	.002	54.35
8001*	1.044	.002	54.35	.002	54.35
8020*	1.044	.002	54.35	.002	54.35
8050*	1.044	.002	54.35	.002	54.35
8100*	1.044	.002	54.35	.002	54.35
10000	0.35	.004	38.84	.003	41.34
100000	0.20	.004	33.98	.003	36.48

Table 9 - Typical Jitter Transfer Function for the E1 Output

Notes

1) For input jitter from 10 kHz to 100 kHz, the jitter attenuation is of such magnitude that intrinsic jitter dominates the output signal, rendering the jitter transfer function unmeasurable.

2) Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* Output jitter dominated by intrinsic jitter.

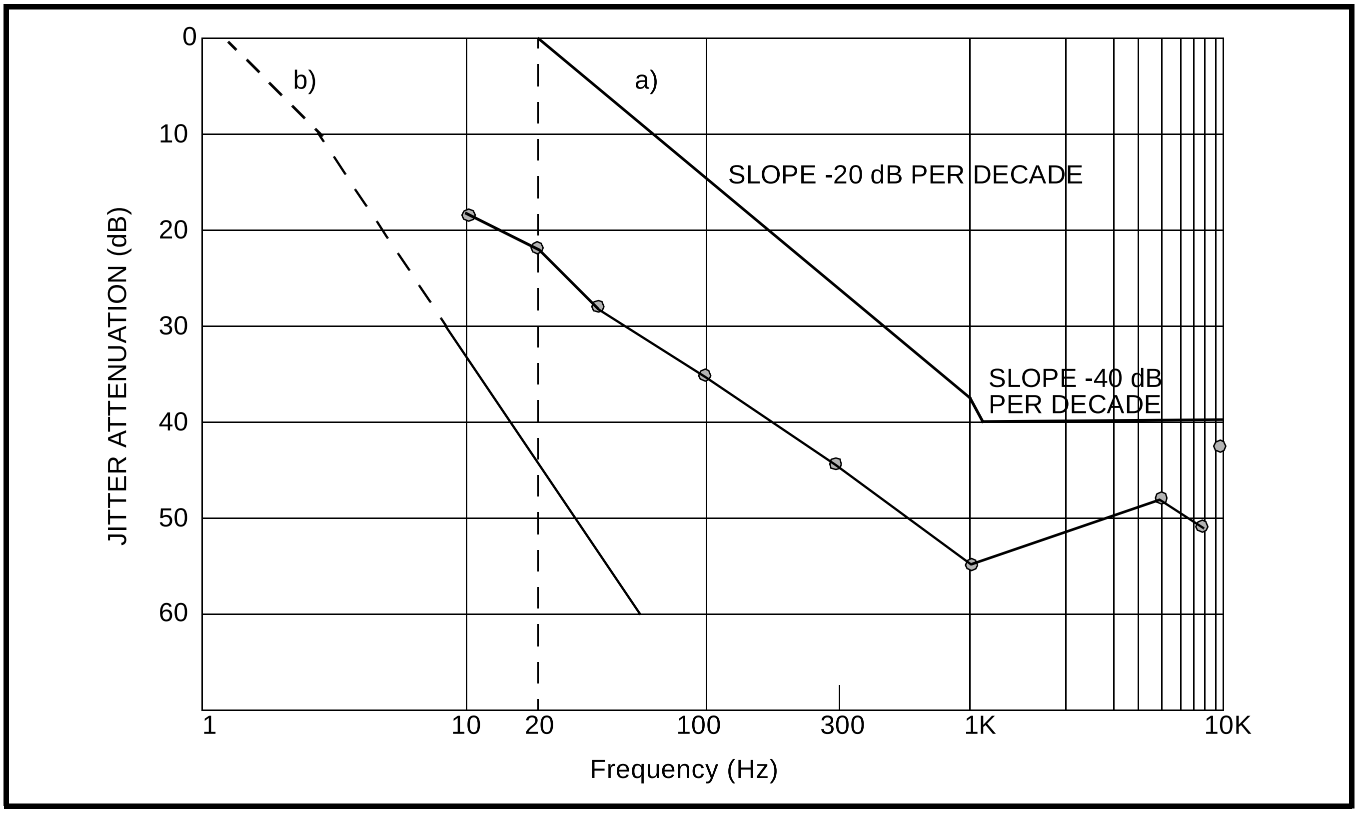

Figure 5 - Typical Jitter Attenuation for T1 Output

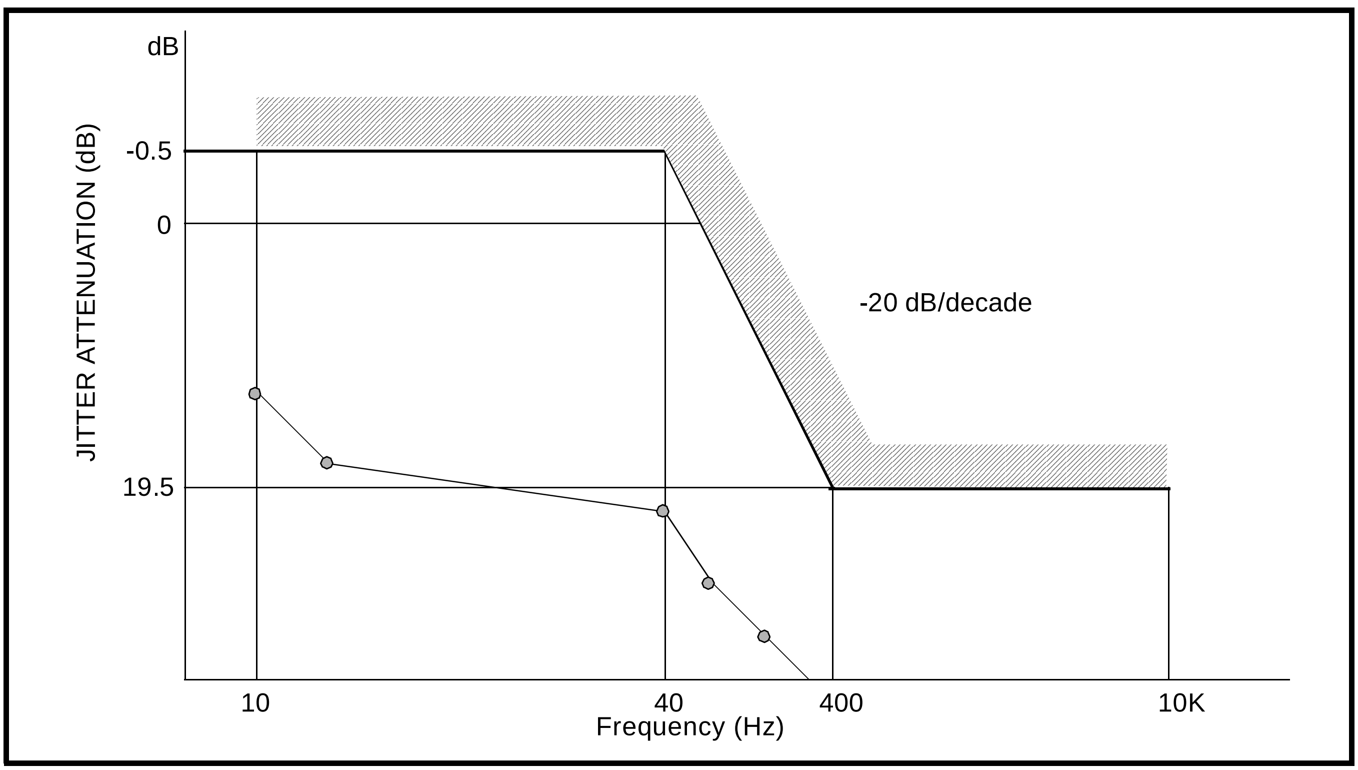

Figure 6 - Typical Jitter Attenuation for E1 Output

Absolute Maximum Ratings* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Input/Output Diode Current	$I_{IK/OK}$		±150	mA
4	Output Source or Sink Current	I_O		±150	mA
5	DC Supply or Ground Current	I_{DD}/I_{SS}		±300	mA
6	Storage Temperature	T_{ST}	-55	125	°C
7	Package Power Dissipation PLCC	P_D		900	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
2	Input HIGH Voltage	V_{IH}	2.0		V_{DD}	V	
3	Input LOW Voltage	V_{IL}	V_{SS}		0.8	V	
4	Operating Temperature	T_A	-40	25	85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

V_{DD} =5.0 V±10%; V_{SS} =0V; T_A =-40 to 85°C.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUP	Supply Current	I_{DD}		55		mA	Under operating condition
2	IN	Input HIGH voltage	V_{IH}	2.0			V	
3	IN	Input LOW voltage	V_{IL}			0.8	V	
4	OUT	Output current HIGH	I_{OH}	-4			mA	V_{OH}=2.4 V
5	OUT	Output current LOW	I_{OL}	4			mA	V_{OL}=0.4 V
6		Leakage current on all inputs	I_{IL}			10	µA	$V_{IN}=V_{SS}$

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics (see Fig. 7)† -Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	INPUTS	8 kHz reference clock period	t_{P8R}		125		µs	
2		1.544 MHz reference clock period	t_{P15R}		648		ns	
3		2.048 MHz reference clock period	t_{P20R}		488		ns	
4		Input to output propagation delay with an 8 kHz reference clock	t_{PD8}		183		ns	MCLKi = 20.000 000MHz
5		Input to output propagation delay with a 1.544 MHz reference clock	t_{PD15}		243		ns	MCLKi = 20.000 000MHz
6		Input to output propagation delay with a 2.048 MHz reference clock	t_{PD20}		183		ns	MCLKi = 20.000 000MHz
7		Input rise time (except MCLKi and GTi)				8	ns	
8		Input fall time (except MCLKi and GTi)				8	ns	
9	OUTPUTS	Delay between C1.5 and C2	$t_{D-20-15}$		18		ns	
10		Frame pulse $\overline{F0o}$ output pulse width	t_{W-F0o}		244		ns	
11		Frame pulse $\overline{F0o}$ output rise time	t_{R-F0o}		5	9	ns	Load = 85pF
12		Frame pulse $\overline{F0o}$ output fall time	t_{F-F0o}		5	9	ns	Load = 85pF
13		Frame pulse FP8-STB output pulse width	$t_{W-FP8STB}$		122		ns	
14		Frame pulse FP8-STB output rise time	$t_{R-FP8STB}$		5	9	ns	Load = 85pF
15		Frame pulse FP8-STB output fall time	$t_{F-FP8STB}$		5	9	ns	Load = 85pF
16		Frame pulse FP8-GCI output pulse width	$t_{W-FP8GCI}$		122		ns	
17		Frame pulse FP8-GCI output rise time	$t_{R-FP8GCI}$		5	9	ns	Load = 85pF
18		Frame pulse FP8-GCI output fall time	$t_{F-FP8GCI}$		5	9	ns	Load = 85pF
19		C1.5 clock period	$t_{P-C1.5}$		648		ns	
20		C1.5 clock output rise time	$t_{RC1.5}$		5	9	ns	Load = 85pF
21		C1.5 clock output fall time	$t_{FC1.5}$		5	9	ns	Load = 85pF
22		C1.5 clock output duty cycle			50		%	
23		$\overline{C3}$ clock period	t_{P-C3}		324		ns	
24		$\overline{C3}$ clock output rise time	t_{RC3}		5	9	ns	Load = 85pF
25		$\overline{C3}$ clock output fall time	t_{FC3}		5	9	ns	Load = 85pF
26		$\overline{C3}$ clock output duty cycle			50		%	
27		C2 clock period	t_{P-C2}		488		ns	
28		C2 clock output rise time	t_{RC2}		5	9	ns	Load = 85pF

AC Electrical Characteristics (see Fig. 7)† -Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
29	OUTPUTS	C2 clock output fall time	t_{FC2}		5	9	ns	Load = 85pF
30		C2 clock output duty cycle			50		%	
31		$\overline{C4}$ clock period	t_{P-C4}		244		ns	
32		$\overline{C4}$ clock output rise time	t_{RC4}		5	9	ns	Load = 85pF
33		$\overline{C4}$ clock output fall time	t_{FC4}		5	9	ns	Load = 85pF
34		$\overline{C4}$ clock output duty cycle			50		%	
35		C8 clock period	t_{P-C8}		122		ns	
36		C8 clock output rise time	t_{RC8}		5	9	ns	Load = 85pF
37		C8 clock output fall time	t_{FC8}		5	9	ns	Load = 85pF
38		C8 clock output duty cycle			50		%	
39		C16 clock period	t_{P-C16}		61		ns	
40		C16 clock output rise time	t_{RC16}		5	9	ns	Load = 85pF
41		C16 clock output fall time	t_{FC16}		5	9	ns	Load = 85pF
42		C16 clock output duty cycle		43	50	55	%	Duty cycle on MCLKi =50%

† -Timing is over recommended temperature & power supply voltages.
‡ -Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

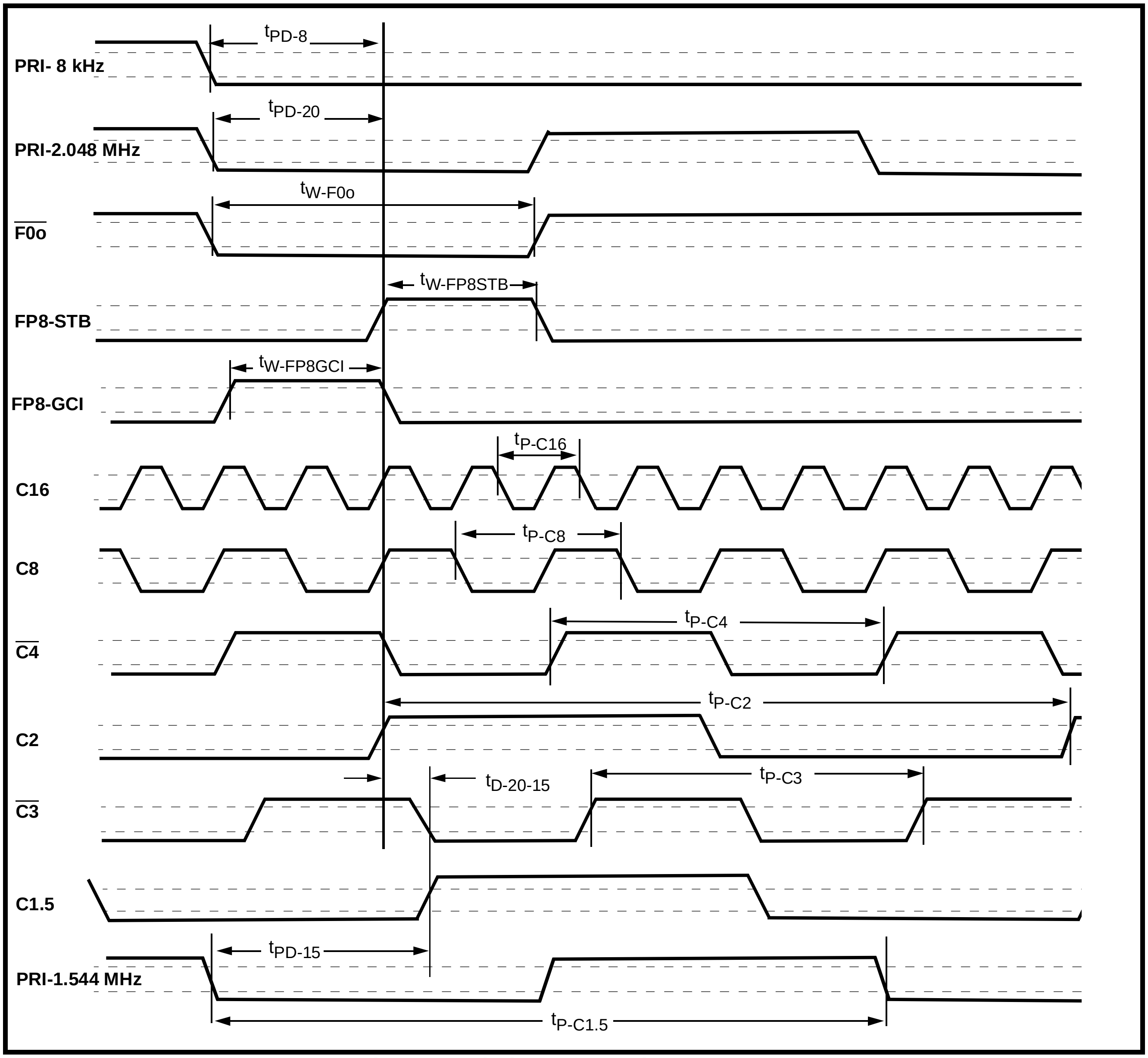

Figure 7 - Timing Information for MT9042

AC Electrical Characteristics (see Fig. 8)† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	CLOCK	Master clock input rise time	t_{rMCLKi}			4	ns	
2		Master clock input fall time	t_{fMCLKi}			4	ns	
3		Master clock frequency	t_{pMCLKi}	19.99936	20	20.000640	MHz	
4		Duty Cycle of the master clock		40	50	60	%	

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

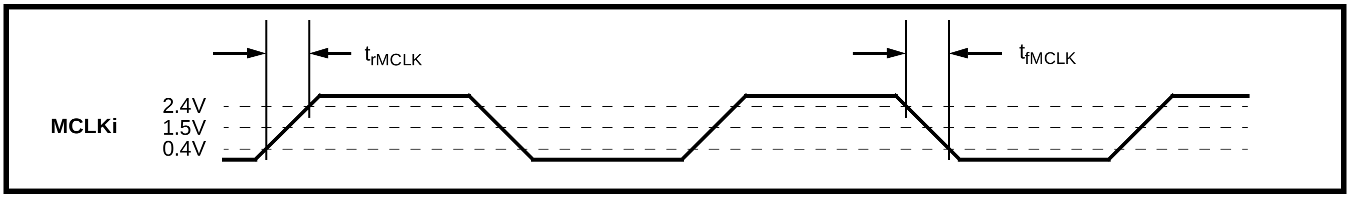

Figure 8 - Master Clock Input

Notes: