SONY

CXA3107N

IF Amplifier for M-ary FSK Pagers

Description

The CXA3107N is a low current consumption FM IF amplifier which employs the newest bipolar process. It is suitable for M-ary FSK pagers.

Features

- Low current consumption: 570 µA (typ. at V_{CC}=1.4 V)
- Low voltage operation: V_{CC}=1.1 to 4.0 V
- Small package 20-pin SSOP
- Needless of IF decoupling capacitor
- Reference power supply for operational amplifier and comparator
- Bit rate filter with variable cut-off
- Misoperation prevention function for continuous data
- RSSI function
- IF input, Vcc standard

Applications

- M-ary FSK pagers

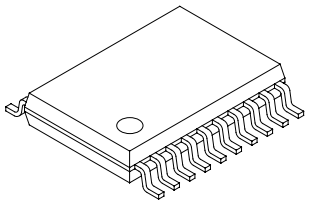
Function

Plastic

Structure

Bipolar silicon monolithic IC

20 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

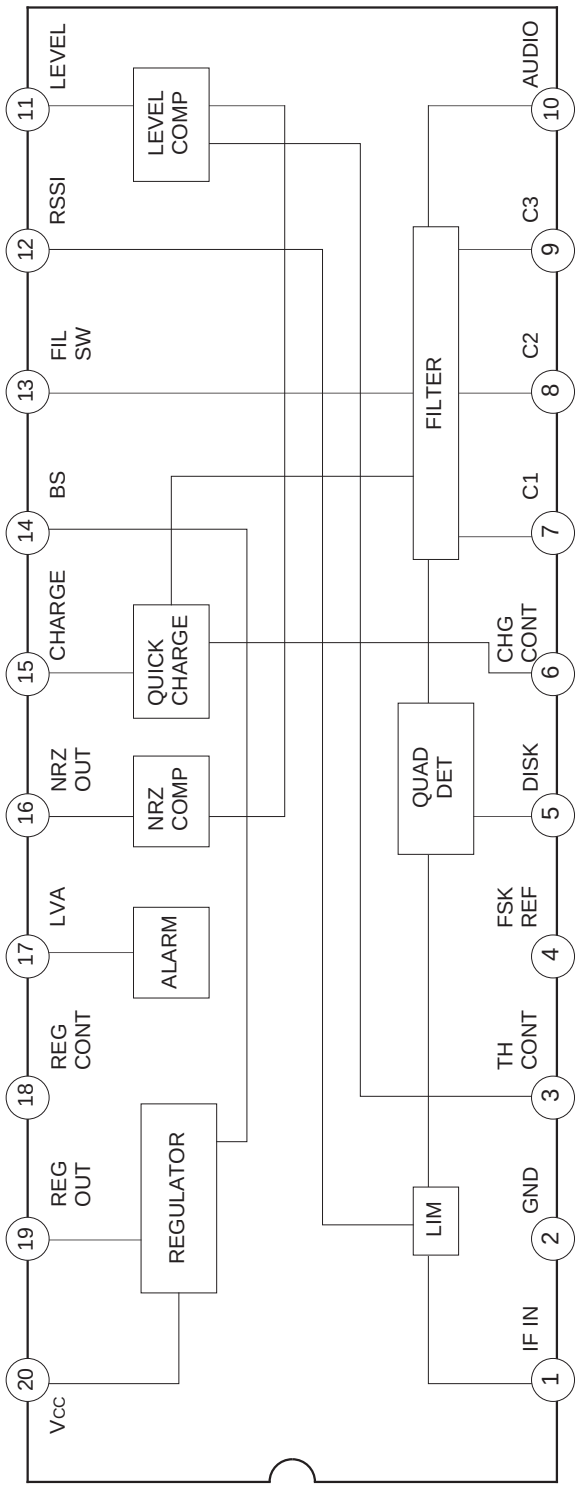
• Supply voltage	V_{CC}	7.0	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C

Operating Condition

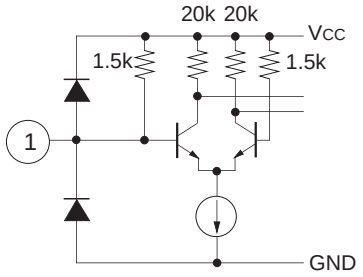
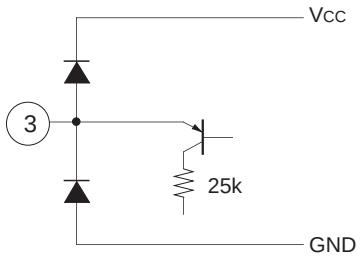
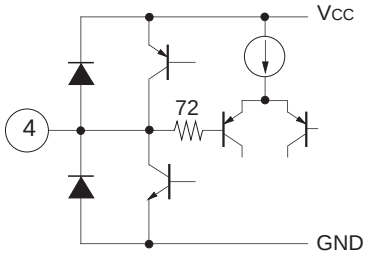
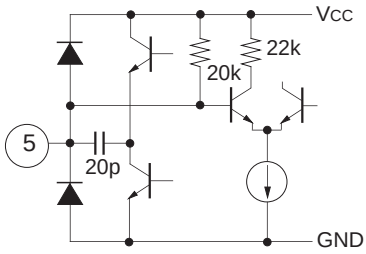
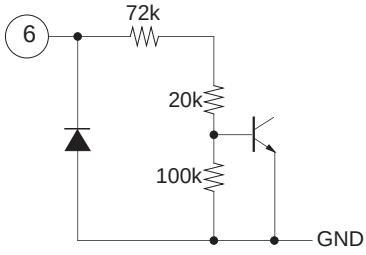
Supply voltage	V_{CC}	1.1 to 4.0	V

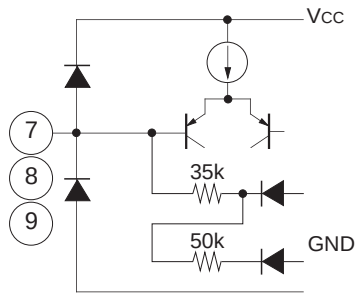
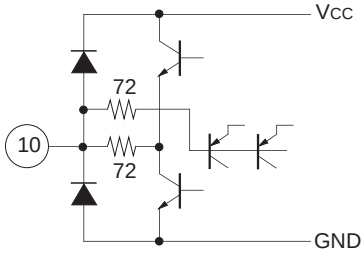
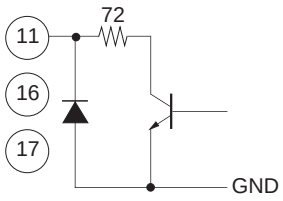
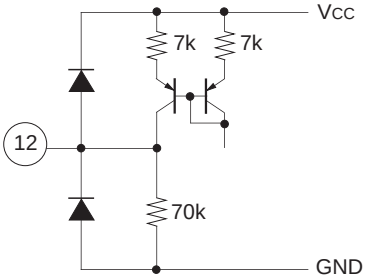
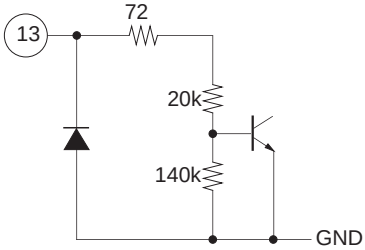
E96303A8Z

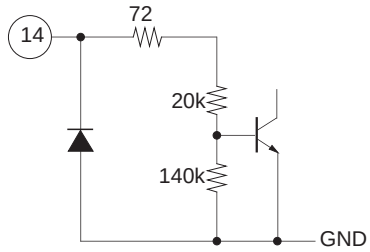
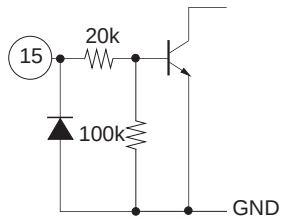
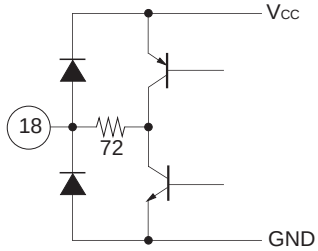
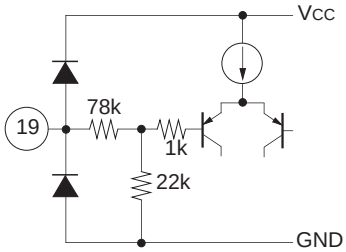
Block Diagram



Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	IF IN	1.4 V		IF limiter amplifier input.
2	GND	—		Ground.
3	TH CONT	—		Determines the level comparator threshold value. The threshold value can be adjusted by inserting the resistor between Pin 3 and Vcc. Normally, short to Vcc.
4	FSK REF	0.2 V		Connects the capacitor that determines the low cut-off frequency for the entire system.
5	DISK	1.4 V		Connects the phase shifter of FM detector circuit.
6	CHG OFF	—		Sets off the quick charge circuit current. The charge current is off by setting Pin 15 low and Pin 6 high.

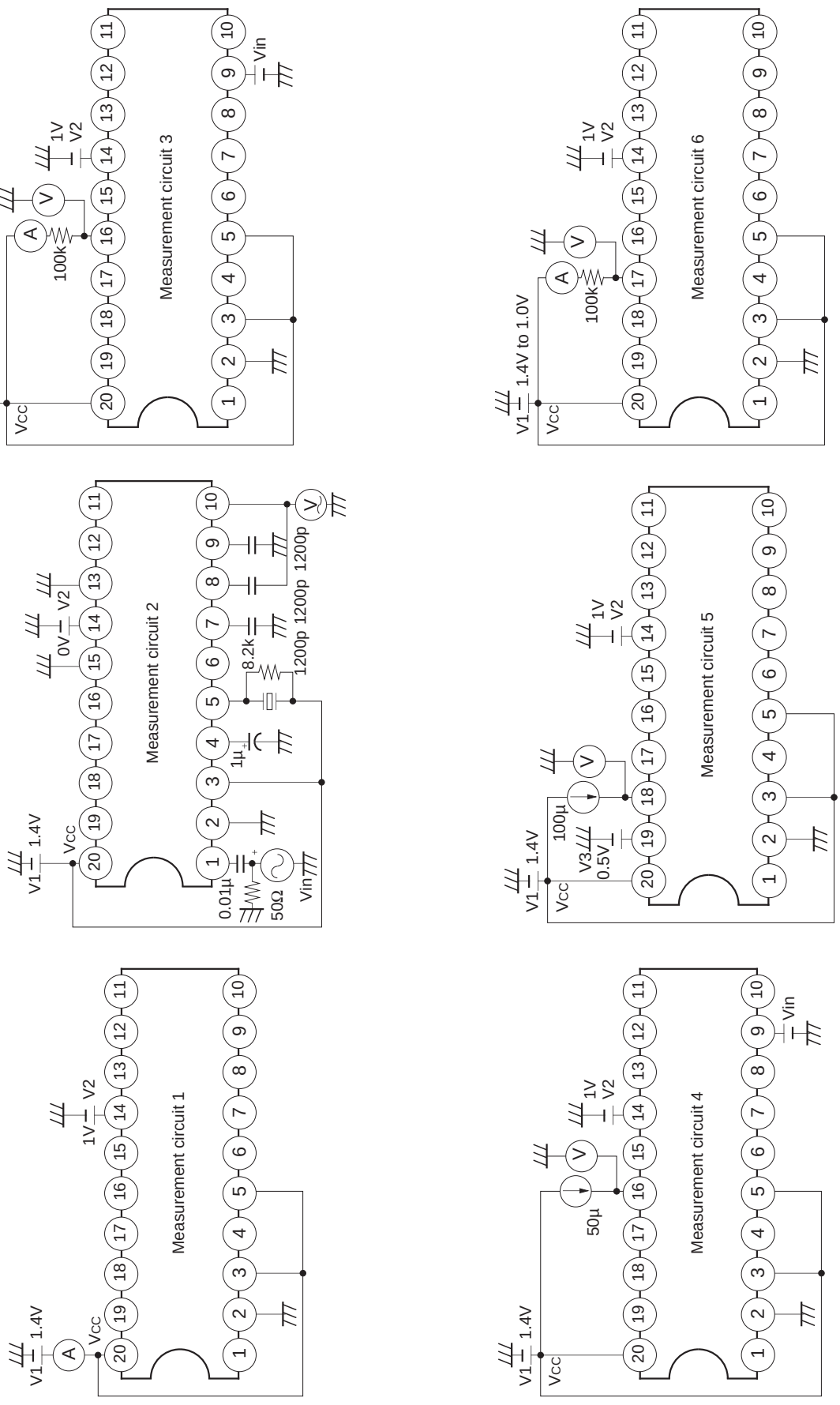
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
7 8 9	C1 C2 C3	0.2 V		Connects the capacitor that determines the LPF cut-off.
10	AUDIO	0.2 V		Level comparator and NRZ comparator inputs. The operational amplifier output is connected.
11 16 17	LEVEL NRZ OUT LVA OUT	— — —		Level comparator, NRZ comparator and LVA comparator outputs. They are open collectors. (Applied voltage range: –0.5 V to +7.0 V)
12	RSSI	0.1 V		RSSI circuit output.
13	FIL SW	—		Switches the LPF cut-off. Cut-off is decreased by setting this pin high. (Applied voltage range: –0.5 V to +7.0 V)

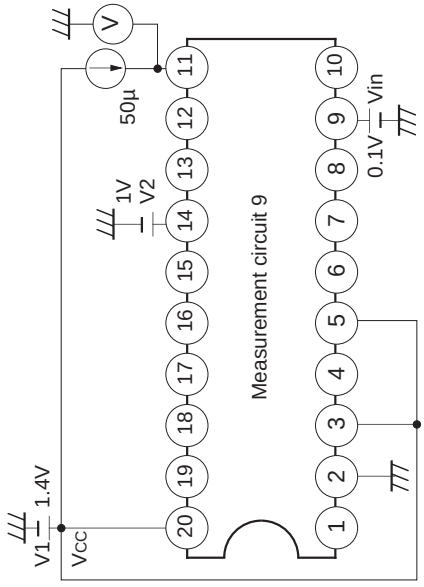
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14	B.S.	—		Controls the battery saving. Setting this pin low suspends the operation of IC. (Applied voltage range: –0.5 V to +7.0 V)
15	CHARGE	—		Controls the charge speed of the quick charge circuit. Set this pin high to execute the quick charge. (Applied voltage range: –0.5 V to +7.0 V)
18	REG CONT	—		Output for internal constant-voltage source amplifier. Connects the base of PNP transistor. (Current capacity: 100 µA)
19	REG OUT	1.0 V		Constant-voltage source output. Controlled to maintain 1.0 V.
20	Vcc			Power supply.

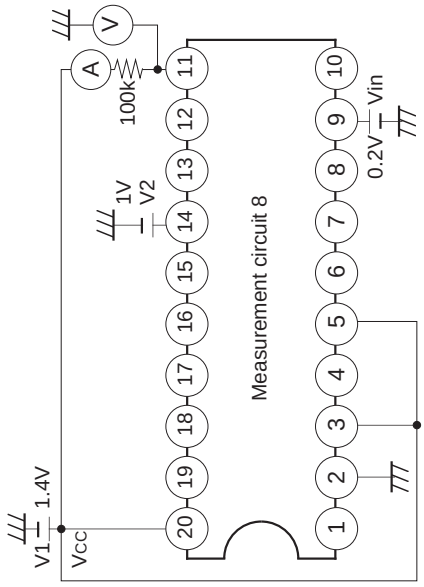
Electrical Characteristics (V_{CC}=1.4 V, Ta=25 °C, F_S=455 kHz, F_{MOD}=1.6 kHz, F_{DEV}=4.8 kHz, AM_{MOD}=30 %)

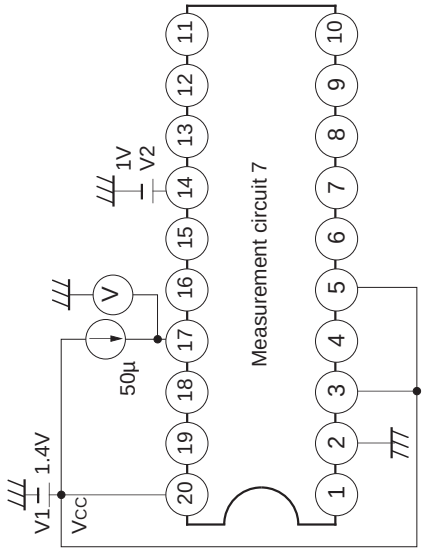
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	Measurement circuit 1 V2=1.0 V	390	570	780	µA
Current consumption	I_{CCS}	Measurement circuit 1 V2=0 V	—	6	20	µA
AM rejection ratio	AMRR	Measurement circuit 2 30 k LPF	25	—	—	dB
NRZ output saturation voltage	V_{SATNRZ}	Measurement circuit 4 Vin=0.3 V	—	—	0.4	V
NRZ output leak current	I_{LNRZ}	Measurement circuit 3 Vin=0.1 V	—	—	5.0	µA
NRZ hysteresis width	V_{TWNRZ}	Measurement circuit 3 Vin=0.1 to 0.3 V	5	10	20	mV
VB output current	I_{OUT}	Measurement circuit 5	100	—	—	µA
VB output saturation current	V_{SATVB}	Measurement circuit 5	—	—	0.4	V
REG OUT voltage	V_{REG}	Output current 0 µA	0.92	0.96	1.02	V
LVA operating voltage	V_{LVA}	Measurement circuit 6 V1=1.4 to 1.0 V	1.00	1.05	1.10	V
LVA output leak current	I_{LLVA}	Measurement circuit 6 1=1.0 V	—	—	5.0	µA
LVA output saturation voltage	V_{SATLVA}	Measurement circuit 7	—	—	0.4	V
Detector output voltage	V_{ODET}	Measurement circuit 2	50	63	80	mVrms
Logic input voltage high level	V_{THBSV}	—	0.9	—	—	V
Logic input voltage low level	V_{TLBSV}	—	—	—	0.35	V
Limiting sensitivity	$V_{IN\ (LIM)}$	Measurement circuit 2, data filter fc=2.4 kHz	—	–83	—	dBm
Detector output level ratio deviation to level comparator window width	V_{LCWR}	—	–15	0	+15	%
Level comparator output saturation voltage	V_{SATLC}	Measurement circuit 9	—	—	0.4	V
Level comparator output leak current	I_{LLC}	Measurement circuit 8	—	—	5.0	µA
RSSI output offset	V_{ORSSI}	Measurement circuit 10	—	100	250	mV
IF limiter input resistance	R_{INLIM}	—	1.2	1.5	1.8	kΩ

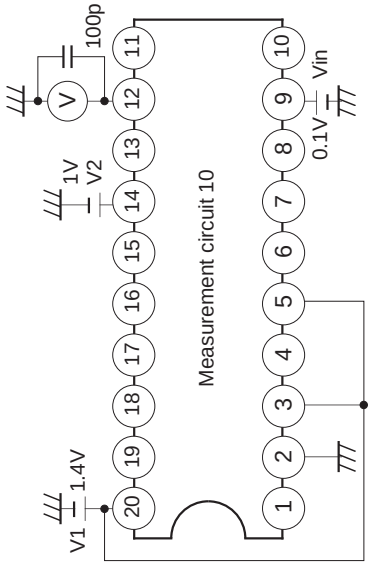
Electrical Characteristics Measurement Circuit



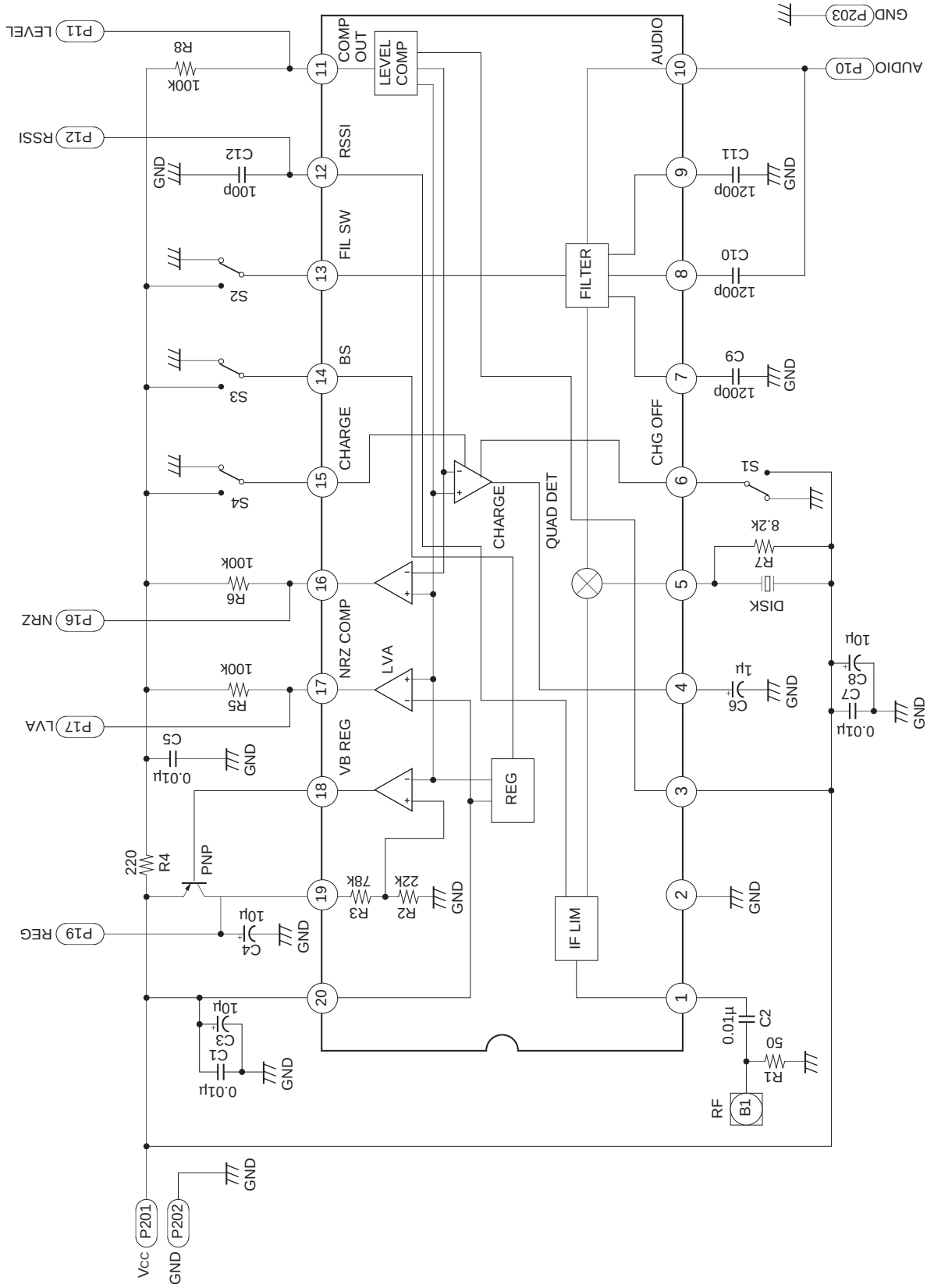

V1 1.4V
Vcc
50µ
V
1V
V2
Measurement circuit 9
0.1V
Vin


V1 1.4V
Vcc
A
100k
V
1V
V2
Measurement circuit 8
0.2V
Vin


V1 1.4V
Vcc
50µ
V
1V
V2
Measurement circuit 7


V1 1.4V
V
100p
1V
V2
Measurement circuit 10
0.1V
Vin

Block Diagram and Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Note

1) Power Supply

The CXA3107N, with built-in regulator, is designed to permit stable operation at wide range of supply voltage from 1.1 to 4.0 V. Decouple the wiring to V_{CC} (Pin 20) as close to the pin as possible.

2) IF Limiter Amplifier

The gain of this IF limiter amplifier is approximately 100 dB. Take notice of the following points in making connection to the IF limiter amplifier input pin (Pin 1).

a) Wiring to the IF limiter amplifier input (Pin 1) should be as short as possible.
b) As the IF limiter amplifier output appears at QUAD (Pin 5), wiring to the ceramic discriminator connected to QUAD should be as short as possible to reduce the interface with the mixer output and IF limiter amplifier input.

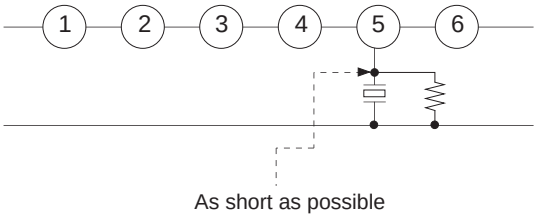


Fig. 1

3) Quick Charge

In order to hasten the rising time from when power is turned on, the CXA3107N features a quick charge circuit. Therefore, the quick charge circuit eliminates the need to insert a capacitor between the detector output and the LPF as is the case with conventional ICs. But a capacitor should be connected to Pin 4 to determine the average signal level during steady-state reception. The capacitance value connected to Pin 4 should be chosen such that the voltage does not vary much due to discharge during battery saving.

Connect a signal for controlling the quick charge circuit to Pin 15. Setting this pin high enables the quick charge mode, and setting this pin low enables the steady-state reception mode. Quick charge is used when the power supply is turned on. The battery saving must be set high at the time.

Connect Pin 15 to GND when quick charge is not being used.

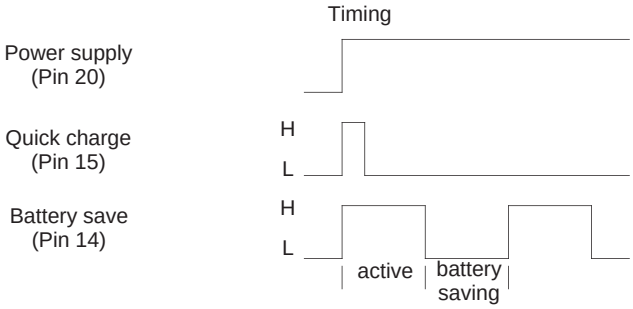


Fig. 2

4) Detector

The detector is of quadrature type. To perform phase shift, connect a ceramic discriminator to Pin 5.
The phase shifting capacitor for the quadrature detector is incorporated. The FM (FSK) signal demodulated with the detector will be output to AUDIO (Pin 10) through the internal LPF.
The AUDIO output is the anti-phase output to NRZ OUT.

The CDBM455C50 (MURATA MFG. CO., LTD) ceramic discriminator is recommended for the CXA3107N.
For the 2-level system, the CDBM455C28 can also used.

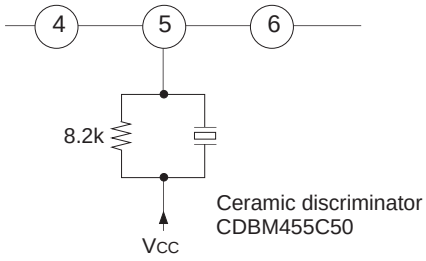


Fig. 3

5) Filter Buffer, Level Comparator and NRZ Comparator

The LPF circuit is built in this IC.
The LPF output is connected internally to the NRZ comparator, level comparator and quick charge circuit.

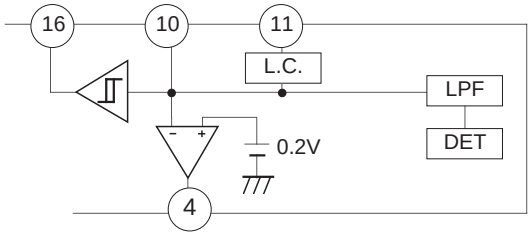


Fig. 4

Using the LPF, remove noise from the demodulated signal and input the signal to the above three circuits.
The level comparator and the NRZ comparator shape waveform of this input signal and output it as a square wave. The comparator output stage is for open collector.
Thus, if the CPU is of CMOS type and the supply voltage is different, a direct interface as illustrated in the figure below can be implemented.

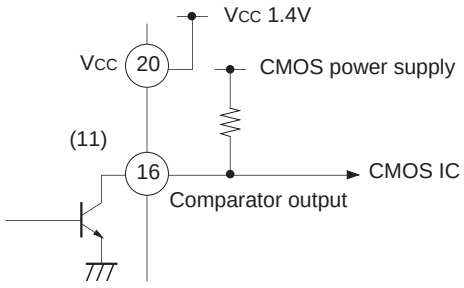


Fig. 5

6) REG CONT

Controls the base bias of the external transistors.

7) LVA OUT

The pin goes high (open) when the supply voltage becomes low. Since the output is an open collector, it can be used to directly drive CMOS device. The setting voltage of the LVA is 1.05 V (typ.), and it possesses a hysteresis with respect to the supply voltage. The hysteresis width is 50 mV (typ.).

8) B.S.

Operation of the CXA3107N can be halted by setting this pin low. This pin can be connected directly to CMOS device. The current consumption for battery saving is 20 µA or less (at 1.4 V).

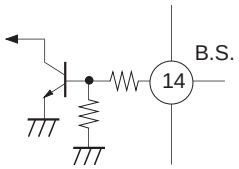
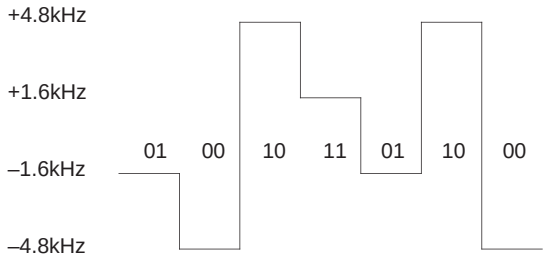


Fig. 6

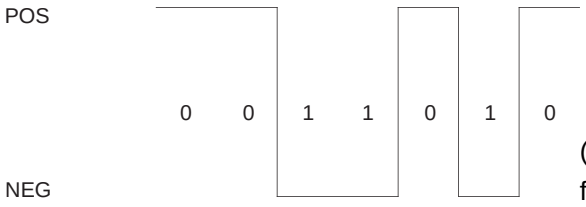
9) M-ary (M = 2- or 4-level) FSK Demodulation System

Polarity discrimination output and MSB comparator output are used to demodulate the 4-level waveform shown below.

[4-level FSK demodulating waveform]

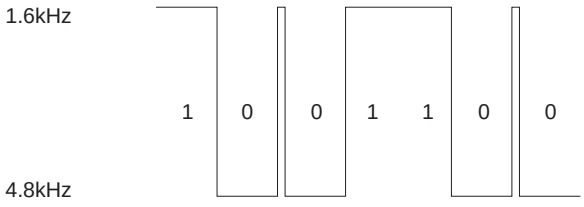


[NRZ OUT] Polarity discrimination output (When the input frequency is higher than the local frequency)



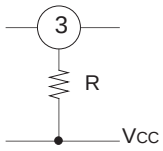
(The polarity can be inverted by setting the local frequency higer than the input frequency.)

[L.C. OUT] MSB comparator output



The 4-level FSK demodulating data is divided into NRZ OUT and L.C. OUT shown above. Here, NRZ OUT corresponds to a conventional NRZ comparator output. L.C. OUT is made comparing the demodulated waveform amplitude to the IC internal reference voltage levels. When the threshold value of L.C. OUT is not appropriate to the detector output, the resistance value on Pin 5 should be varied for the detector output level adjustment or the resistor should be inserted between Pin 3 and V_{CC} for the level comparator threshold value adjustment.

For the 2-level FSK demodulation, it corresponds to a conventional NRZ comparator output.



10) Principle of Quick Charge Operation

BUF in Fig. 7 is the detector buffer amplifier and AMP is the operational amplifier used to construct the LPF. COMP is the level comparator or the NRZ comparator. The CXA3107N has a feedback loop from the comparator input to the input circuit of the detector output buffer. This equalizes the average value of the comparator input voltage to the reference voltage, with the quick charge circuit of CHG being set in the feedback loop. Switching the current of the quick charge circuit enables reduction of the rise time.

In this block, CHG is a comparator which compares input voltages and outputs a current based on this comparison. The current on CHG is switched between high and low at Pin 15. When the power is turned on, switch the current to high to increase the charge current at C in Fig. 7 and shorten the time constant. During steady-state reception mode, switch the current to low, lengthening the charge time constant and allowing for stable data retrieval. Also, controlling Pin 6 can make the current off. This is effective when the same data are received continuously.

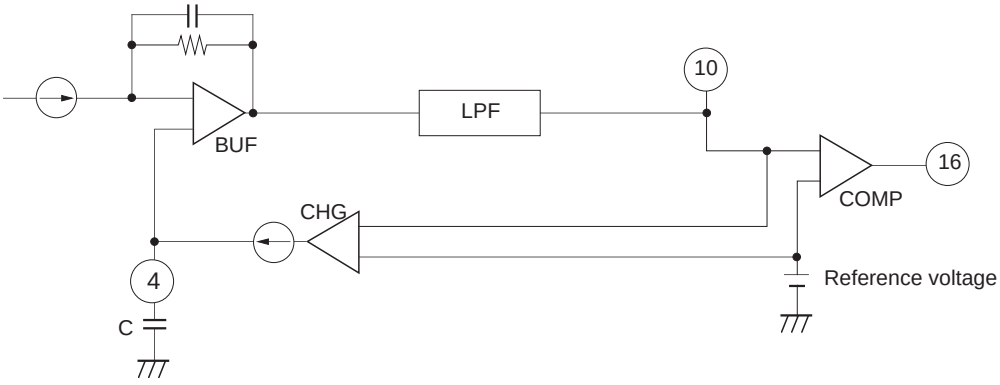


Fig. 7

11) S Curve Characteristics

Even if the IF IN input signal frequency is deviated, the feedback is applied to the DETOUT operating point so as to match it to the comparator reference voltage by the quick charge operation shown in Fig. 7. Therefore, this feedback must be halted in order to evaluate the S curve characteristics.

To execute the evaluation, measure the average voltage on Pin 10 first and input this voltage to Pin 4 from the external power supply.

12) Control Pins

The function controls are as shown below.

PIN No.	13	6	14	15
Symbol	FIL SW	CHG OFF	BS	CHARGE
Function	Data filter cut-off control	Pin 4 charge current control	Battery saving mode control	Pin 4 charge speed control
Input high	fc: Low	Slow charge off	IC operation*	Quick charge
Input low	fc: High*	Slow charge operation*	Sleep	Slow charge*

Note) Pin 6 control should be performed with Pin 15 low.

When each function is not controlled externally, set it to the state with asterisk (∗).

13) LPF Constant

The data filter cut-off (fc) is expressed with the following equation.

$$fc \approx \frac{1}{2\pi CR}$$

C: External capacitance
R: IC internal resistance

R is approximately 55 kΩ ± 20 % when Pin 13 is low. The table below shows the example of constant to data rate.

		Capacitance (pF)	fc (Hz)	Data rate
Pin 13 filter switch	H	6800	—	—
	L		430	512 bps (2 levels)
	H	1500	950	1200 bps (2 levels)
	L		1900	2400 bps (2 levels)
	H	1200	1200	1600 bps (2 levels)
	L		2400	3200 bps (2 levels)
	H	1200	1200	3200 bps (2 levels)
	L		2400	6400 bps (2 levels)

14) Misoperation Prevention Function for Continuous Data

The offset to the comparator threshold value of the detector output is canceled with the feedback loop indicated in the paragraph 10). This operation assumes that “0” and “1” are in equal numbers in the data. The offset is occurred when the “0” or “1” data are received continuously. In this case, setting Pin 6 high to make the charge current off prevents the offset occurrence.

Without using this function, the stability for the same data continuously received depends on the capacitance value on Pin 4 shown in the paragraph 10). When this capacitance value is increased, the data is demodulated more stably; however, it takes more time for the IC to rise. If this function is not used, be sure to connect Pin 6 to GND.

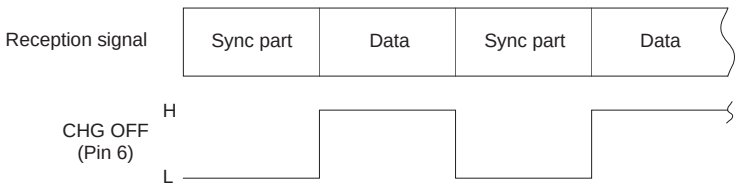
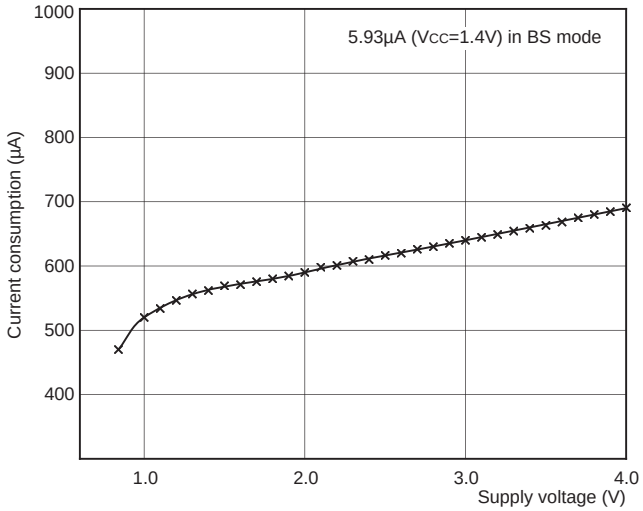


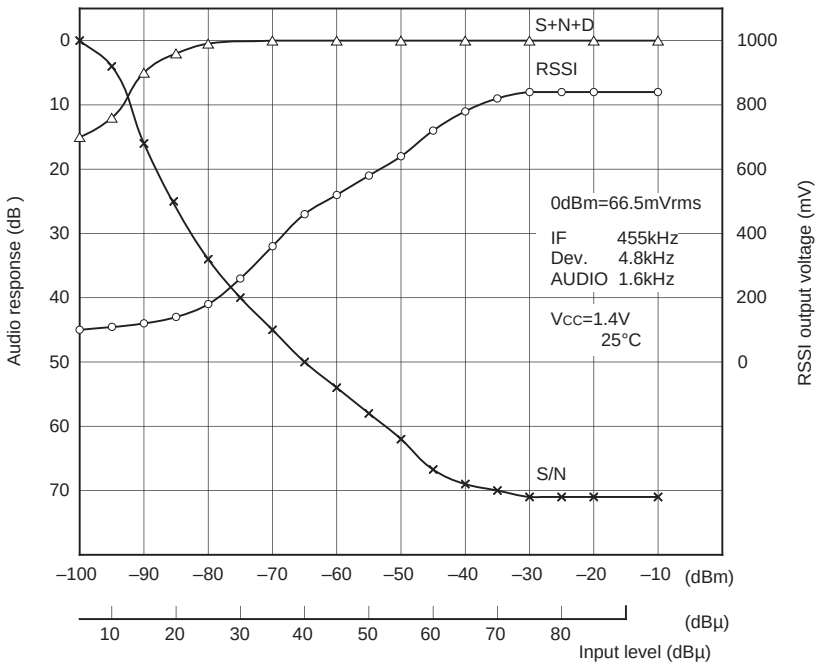
Fig. 8

Example of Representative Characteristics

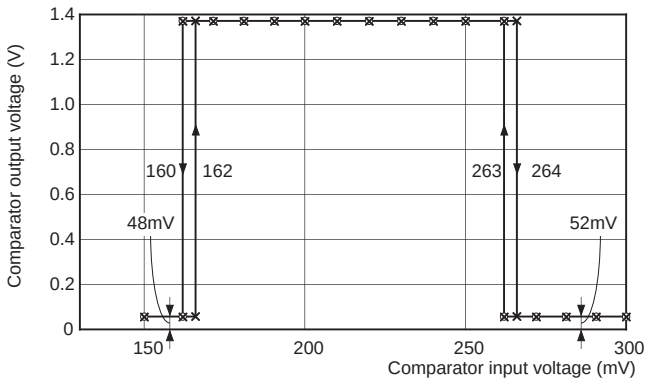
Supply voltage vs. Current consumption



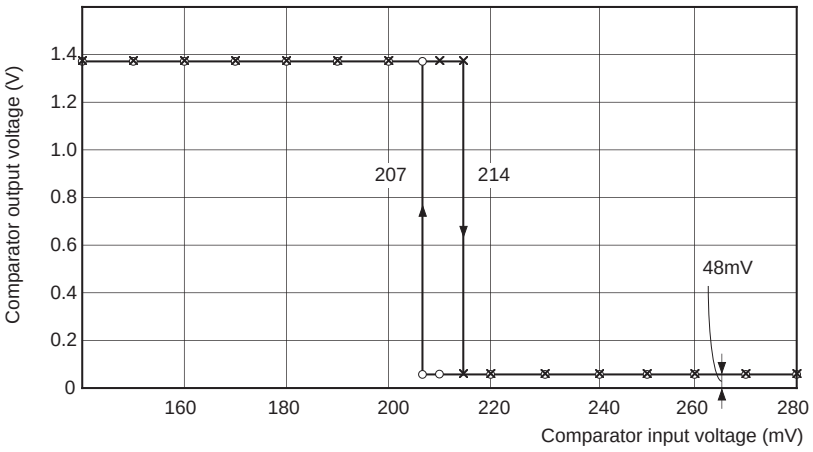
Audio respnse and RSSI output voltage characteristics



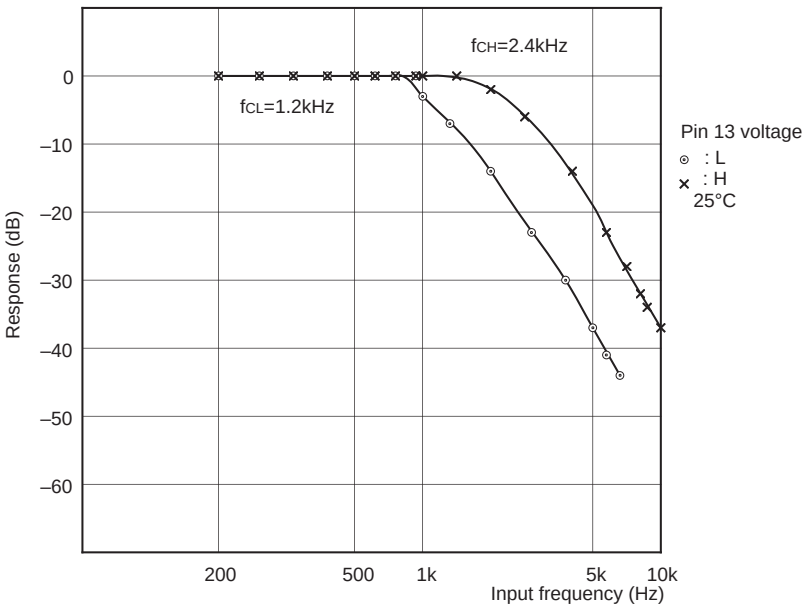
Level comparator characteristics



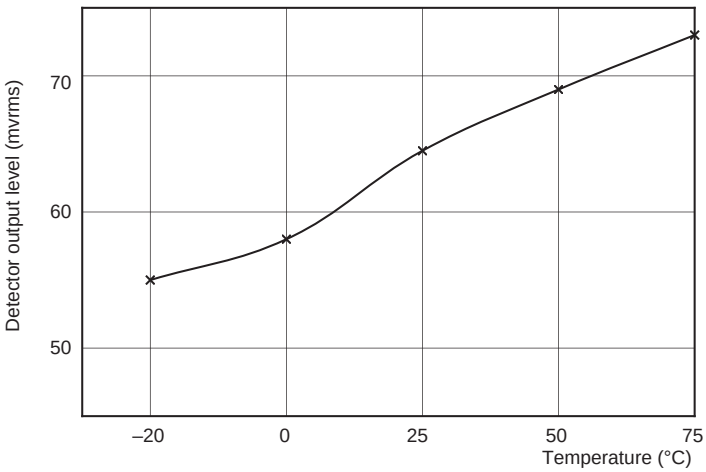
NRZ comparator characteristics



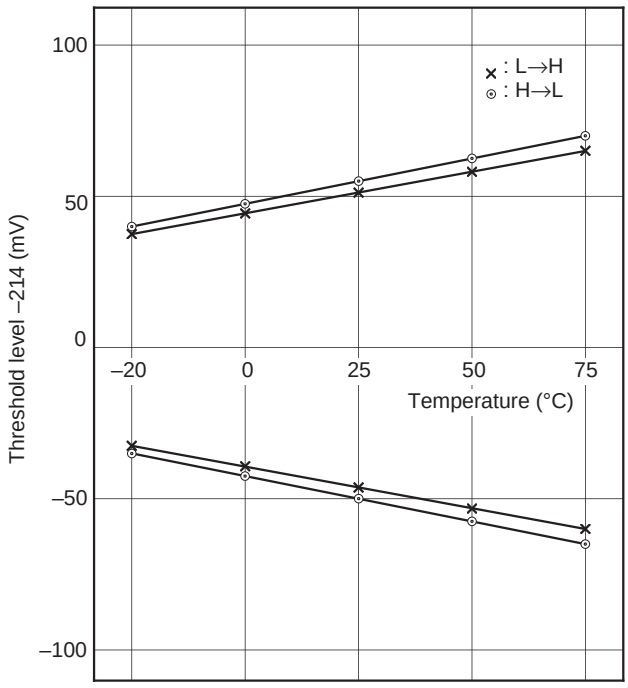
Variable cut-off characteristics of audio filter



Detector output level temperature characteristics

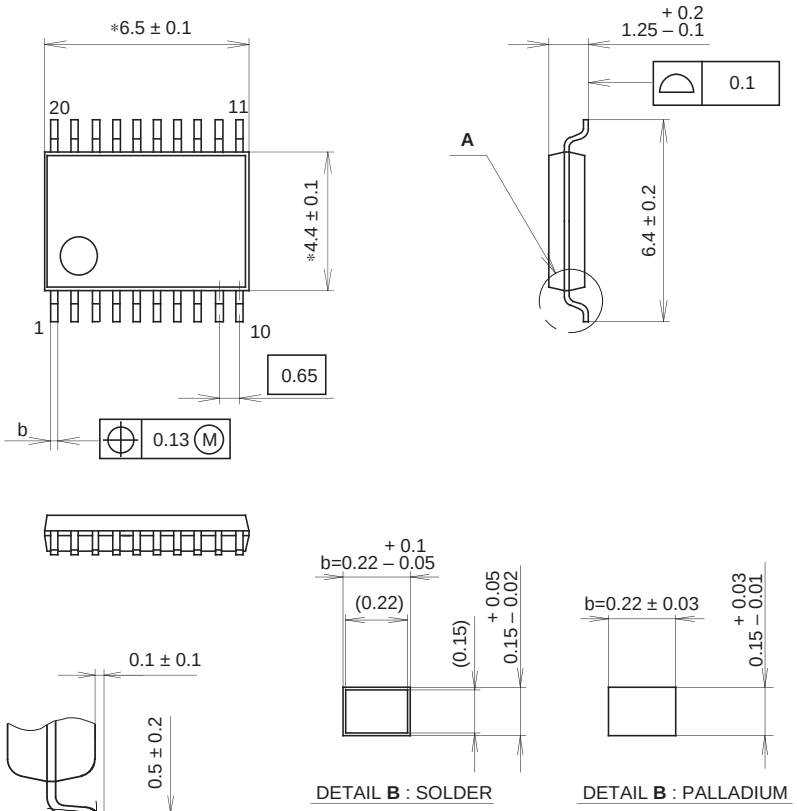


Threshold level characteristics



Package Outline Unit : mm

20PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).