

SANYO

No. ※ 5076A

LC11012-141**Computer Image Signal Processing
Full-Color Gray-Scale Processor****Preliminary****Overview**

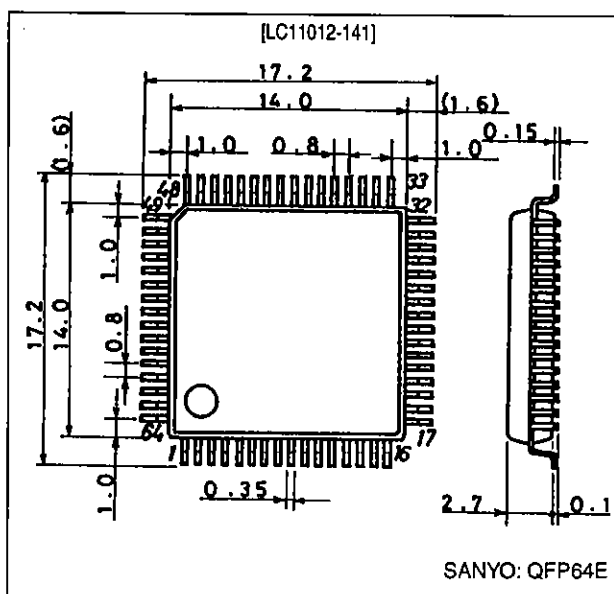
The LC11012-141 is a pseudo gray-scale processor for TFT-LCD panel displays. It allows TFT-LCD panels with 3- or 4-bit input digital drivers to display the equivalent of 16.7 million colors.

Features

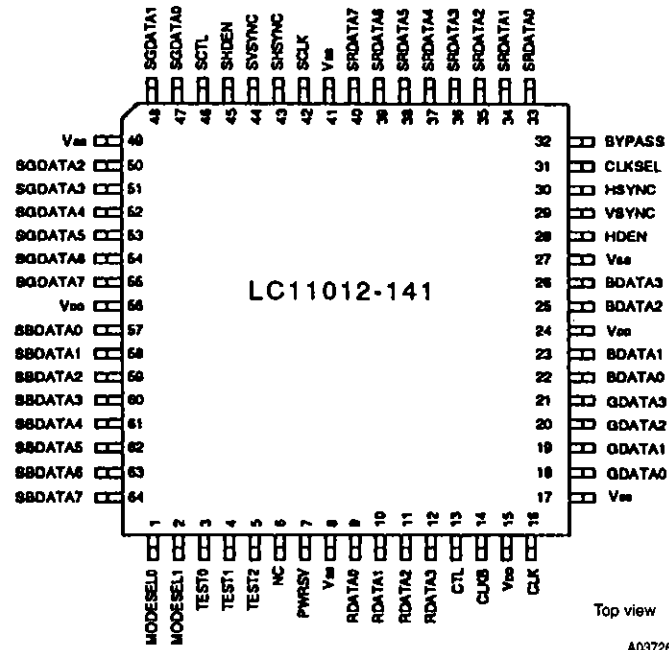
- Handles 8 bits of input data (256-level gray scale data) for each of the RGB colors
- Realizes reduced resolution loss (as compared to dithering techniques) by using intra-frame and inter-frame error diffusion processing
- Incorporates a new full-coloration algorithm, formerly best done using computers
- Operating mode selection of outputs for 3- or 4-bit drivers
- Supports both 5V and low-voltage 3.3V operation
- Operates with arbitrary clock frequencies up to 40MHz (5V supply) and 30MHz (3.3V supply)
- Can operate independently of the number of displayed pixels since internal operation is controlled by the horizontal and vertical synchronization signals.
- Power-save function to stop the internal operation processing circuits, and output the clock, sync signals and control signals

Package Dimensions

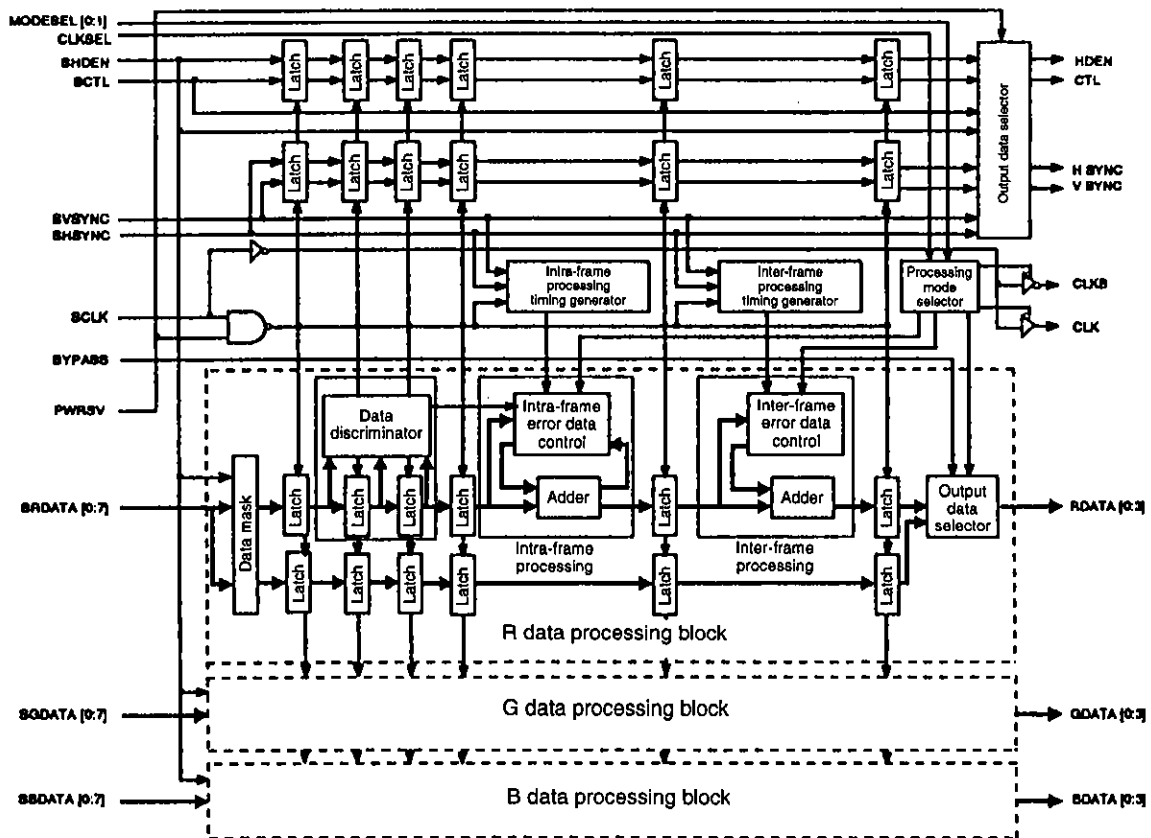
unit: mm

3159-QFP64E

Pin Assignment



Block Diagram



A03727

Pin Functions

| Symbol | Pin No. | I/O ¹ | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------|--|------------------|---|-----------------|----------|---|---|---|---|----------|--|---|---|---|---|----------|--|---|---|---|---|------------|------------------------|-----|-----|-----|----------|------------------------|-----|-----|----|----------------------------|--|---|---|---|--|-----------------------|--|---|---|---|--|------------------------------|------------|---|---|---|---|---|--|
| V _{DD} | 15, 24, 56 | | Power supply (+5V) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V _{SS} | 8, 17, 27, 41, 49 | | Ground (0V) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NC | 6 | | Must be left open. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MODESEL [0:1] | 1, 2 | I | <p>Mode selection signals [0:1] for the gray-scale mode. The setting process for the mode selection lines is described below. MODESEL0 is the LSB and MODESEL1 is the MSB. Note that the mode number (0 to 3) and the gray-scale processing differ from existing devices.</p> <table border="1"> <thead> <tr> <th colspan="2">Gray-scale mode</th> <th>0</th> <th>1</th> <th>2</th> <th>3</th> </tr> </thead> <tbody> <tr> <td colspan="2">MODESEL0</td> <td>L</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td colspan="2">MODESEL1</td> <td>L</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td rowspan="2">Processing</td> <td>Intra-frame processing</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td rowspan="2">Reserved</td> </tr> <tr> <td>Inter-frame processing</td> <td>Yes</td> <td>Yes</td> <td>No</td> </tr> <tr> <td colspan="2">Number of valid input bits</td> <td>8</td> <td>8</td> <td>8</td> <td></td> </tr> <tr> <td colspan="2">Number of output bits</td> <td>3</td> <td>4</td> <td>4</td> <td></td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Gray-scale mode¹</th> <th>LCD module</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Operating mode for TFT LCD modules with 3-bit source driver</td> </tr> <tr> <td>1</td> <td>Operating mode for TFT LCD modules with 4-bit source driver</td> </tr> <tr> <td>2</td> <td>Operating mode for TFT LCD modules with 3-bit source driver that perform FRC or other inter-frame processing</td> </tr> </tbody> </table> <p>1. Do not use gray-scale modes 0 and 1 with TFT LCD modules that perform FRC or other inter-frame processing.</p> | Gray-scale mode | | 0 | 1 | 2 | 3 | MODESEL0 | | L | H | L | H | MODESEL1 | | L | L | H | H | Processing | Intra-frame processing | Yes | Yes | Yes | Reserved | Inter-frame processing | Yes | Yes | No | Number of valid input bits | | 8 | 8 | 8 | | Number of output bits | | 3 | 4 | 4 | | Gray-scale mode ¹ | LCD module | 0 | Operating mode for TFT LCD modules with 3-bit source driver | 1 | Operating mode for TFT LCD modules with 4-bit source driver | 2 | Operating mode for TFT LCD modules with 3-bit source driver that perform FRC or other inter-frame processing |
| Gray-scale mode | | 0 | 1 | 2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MODESEL0 | | L | H | L | H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MODESEL1 | | L | L | H | H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Processing | Intra-frame processing | Yes | Yes | Yes | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Inter-frame processing | Yes | Yes | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Number of valid input bits | | 8 | 8 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Number of output bits | | 3 | 4 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Gray-scale mode ¹ | LCD module | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Operating mode for TFT LCD modules with 3-bit source driver | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Operating mode for TFT LCD modules with 4-bit source driver | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | Operating mode for TFT LCD modules with 3-bit source driver that perform FRC or other inter-frame processing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BYPASS | 32 | I | Gray-scale processing bypass pin. When a low-level input on this pin is sampled on the falling edge of the clock, the IC will begin the output of unchanged data five clock cycles later. Data is output via the internal latch circuit. Data is not output, however, when the SCLK clock signal is not input. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TEST [0:2] | 3, 4, 5 | I | Test pins [0:2]; left open for normal operation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SCLK | 42 | I | Display dot clock signal input. Data is processed according to this clock signal. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SRDATA [0:7] | 33 to 40 | I | Input pins for red, green and blue gray-scale data. SRDATA7, SGDATA7 and SBDA7 are the MSBs. SRDATA0, SGDATA0 and SBDA0 are the LSBs. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SGDATA [0:7] | 47, 48, 50 to 55 | I | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SBDATA [0:7] | 57 to 64 | I | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SHSYNC | 43 | I | Horizontal and vertical synchronization signal inputs. These are the sources for the HSYNC and VSYNC signals. They are also used to control data processing. Active-low signals. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SVSYNC | 44 | I | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SHDEN | 45 | I | Horizontal data valid-period signal input. Set this pin high during periods when the horizontal data is valid. If this signal is not used, tie it high and set the input data to 0 during the horizontal blanking period. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SCTL | 46 | I | LCD control signal input. Input control signal that must be matched to the data signal timing. This is the source for the CTL signal. If the CTL signal is not used, there is no need to input the SCTL signal. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CLKSEL | 31 | I | CLKSEL is the dot clock output select pin. It is used to select the output mode of the dot clock signal output pin. If CLKSEL is low: A signal with the opposite phase from the SCLK pin is output from the CLK pin. If CLKSEL is high: A signal with the same phase as the SCLK pin is output from the CLKB pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CLK | 16 | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CLKB | 14 | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RDATA [0:3] | 9 to 12 | O | Red, green and blue gray-scale data output pins. These are delayed by five clock cycles with respect to the input data. RDATA3, GDATA3 and BDATA3 are the MSBs. In mode 0: RDATA1, GDATA1 and BDATA1 are the LSBs. In this mode RDATA0, GDATA0 and BDATA0 are set low. In modes 1 and 2: RDATA0, GDATA0 and BDATA0 are the LSBs. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GDATA [0:3] | 18 to 21 | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BDATA [0:3] | 22, 23, 25, 26 | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSYNC | 29 | O | Vertical and horizontal synchronization signal outputs. To match the data signal timing, these outputs are delayed by five clock cycles with respect to their input signals. When PWRSV is low, these signals are output without being latched internally. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HSYNC | 30 | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LC11012-141

| Symbol | Pin No. | I/O ¹ | Function |
|--------|---------|------------------|--|
| HDEN | 28 | O | Horizontal data valid-period signal output. To match the data signal timing, this output is delayed by five clock cycles with respect to the SHDEN input signal. When PWRSV is low, this signal is output without being latched internally. |
| CTL | 13 | O | LCD control signal output. To match the data signal timing, this output is delayed by five clock cycles with respect to the SCTL input signal. When PWRSV is low, this signal is output without being latched internally. |
| PWRSV | 7 | I | Power-save control input. When this input goes low, the internal clock stops and the LSI enters power-save mode. Output data are held high. VSYNC, HSYNC, HDEN and CTL control signals, and either CLK or CLKB are output without being latched internally. Tie high or leave open for normal operation. |

1. I = input, O = output

Specifications (Electrical characteristics values are provisional only and are subject to change.)

Absolute Maximum Ratings at $V_{SS} = 0V$

| Parameter | Symbol | Ratings | Unit |
|------------------------|---------------|------------------------|------|
| Maximum supply voltage | $V_{DD\ max}$ | -0.3 to +7.0 | V |
| Input/output voltage | V_i, V_o | -0.3 to $V_{DD} + 0.3$ | V |
| Operating temperature | T_{opr} | 0 to +70 | °C |
| Storage temperature | T_{stg} | -40 to +125 | °C |

Electrical Characteristics at an operating voltage of 5.0V

Allowable Operating Ranges at $T_a = 0$ to +70°C

| Parameter | Symbol | min | typ | max | Unit |
|-----------------|-----------|-----|-----|----------|------|
| Supply voltage | V_{DD} | 4.5 | 5.0 | 5.5 | V |
| Input voltage | V_{IN} | 0 | - | V_{DD} | V |
| Clock frequency | f_{clk} | - | - | 40 | MHz |

DC Characteristics at $T_a = 0$ to +70°C, $V_{DD} = 4.5$ to 5.5V, $V_{SS} = 0V$

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------------|-----------|-----------------|-----|-----|-----|------|
| High-level input voltage | V_{IH} | TTL compatible | 2.2 | - | - | V |
| Low-level input voltage | V_{IL} | TTL compatible | - | - | 0.8 | V |
| High-level output voltage | V_{OH} | $I_{OH} = -2mA$ | 2.4 | - | - | V |
| Low-level output voltage | V_{OL} | $I_{OL} = 2mA$ | - | - | 0.4 | V |
| Current dissipation (1) | I_{CC} | Note 1 | - | 45 | 70 | mA |
| Current dissipation (2) | I_{CPS} | Note 2 | - | 9 | 12 | mA |
| Current dissipation (3) | I_{CST} | Note 3 | - | - | 200 | μA |

- Notes. 1. $f_{clk} = 25.175MHz$, $V_{DD} = 5.0V$, $C_L = 15pF$, (measured with VGA timing)
 2. PWRSV = low, $f_{clk} = 25.175MHz$, $V_{DD} = 5.0V$, $C_L = 15pF$ (control signals)
 3. $V_{DD} = 5.0V$, all output pins = open, all input pins = V_{DD} or V_{SS}

Switching Characteristics at $T_a = 0$ to +70°C, $V_{DD} = 4.5$ to 5.5V, $V_{SS} = 0V$, $C_L = 15pF$

| Parameter | Symbol | min | typ | max | Unit |
|-----------------------------|------------|-------------|-----|-----|------|
| Dot clock cycle time | T_{dclk} | 25 | - | - | ns |
| Hsync low-level pulse width | T_{hpw} | $2T_{dclk}$ | - | - | ns |
| Vsync low-level pulse width | T_{vpw} | $2T_{dclk}$ | - | - | ns |
| Data setup time | T_{dsu} | 5 | - | - | ns |
| Data hold time | T_{dhd} | 5 | - | - | ns |
| Control signal setup time | T_{csu} | 5 | - | - | ns |

LC11012-141

| Parameter | Symbol | min | typ | max | Unit |
|---------------------------------------|--------|-----------|-----------|------------|------|
| Control signal hold time | Tchd | 5 | – | – | ns |
| CLK propagation delay time | Tdhh | 4 | 6 | 12 | ns |
| CLK propagation delay time | Tdll | 4 | 6 | 13 | ns |
| CLKB propagation delay time | Tdhl | 4 | 7 | 13 | ns |
| CLKB propagation delay time | Tdhlh | 4 | 6 | 12 | ns |
| Control signal propagation delay time | Ttcl | 5Tclk + 4 | 5Tclk + 7 | 5Tclk + 13 | ns |
| Data output propagation delay time | Ttdata | 5Tclk + 4 | 5Tclk + 7 | 5Tclk + 14 | ns |

Electrical Characteristics at an operating voltage of 3.3V

Allowable Operating Ranges at Ta = 0 to +70°C

| Parameter | Symbol | min | typ | max | Unit |
|-----------------|------------------|-----|-----|-----------------|------|
| Supply voltage | V _{DD} | 3.0 | 3.3 | 3.6 | V |
| Input voltage | V _{IN} | 0 | – | V _{DD} | V |
| Clock frequency | f _{clk} | – | – | 30 | MHz |

DC Characteristics at Ta = 0 to +70°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V

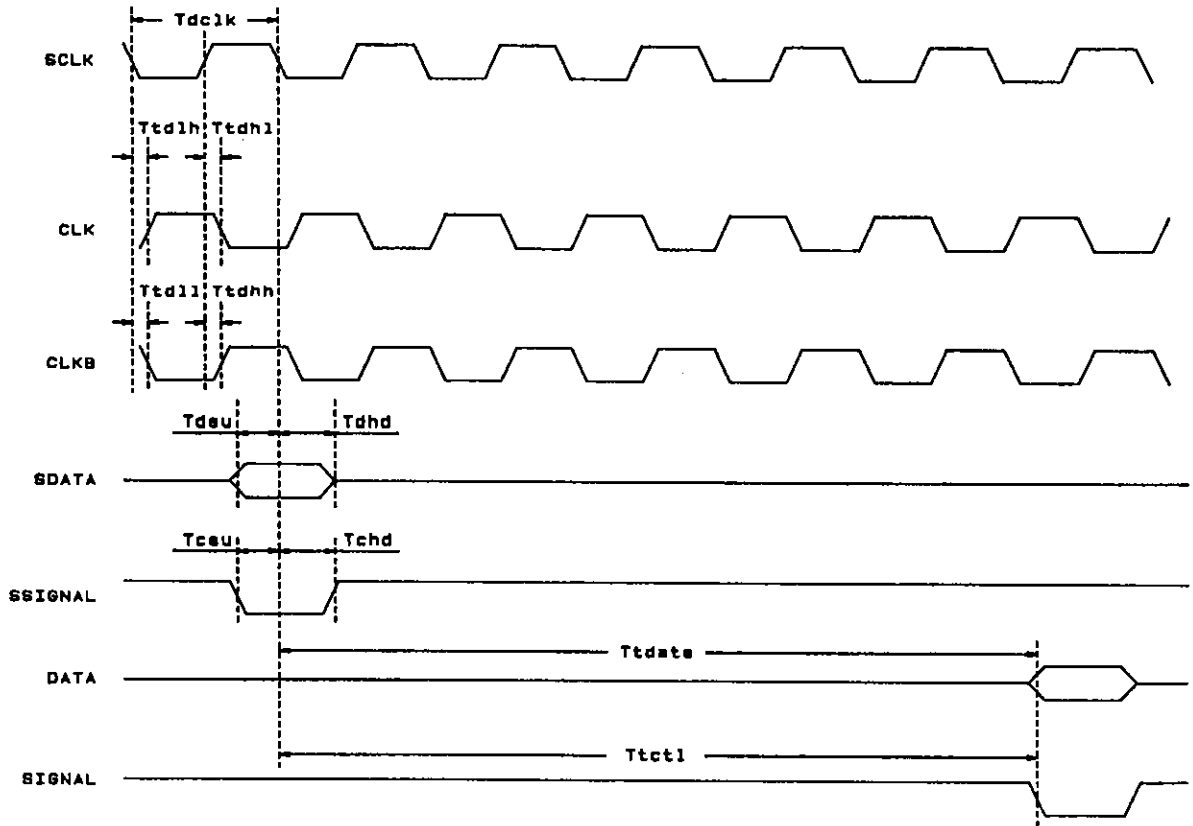
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------------|------------------|------------------------|-----|-----|-----|------|
| High-level input voltage | V _{IH} | | 2.0 | – | – | V |
| Low-level input voltage | V _{IL} | | – | – | 0.5 | V |
| High-level output voltage | V _{OH} | I _{OH} = –1mA | 2.4 | – | – | V |
| Low-level output voltage | V _{OL} | I _{OL} = 1mA | – | – | 0.4 | V |
| Current dissipation (1) | I _{CC} | Note 1 | – | 30 | 45 | mA |
| Current dissipation (2) | I _{CPS} | Note 2 | – | 5 | 8 | mA |
| Current dissipation (3) | I _{CST} | Note 3 | – | – | 160 | μA |

Notes. 1. f_{clk} = 25.175MHz, V_{DD} = 3.3V, C_L = 15pF, (measured with VGA timing)
 2. PWRSV = low, f_{clk} = 25.175MHz, V_{DD} = 3.3V, C_L = 15pF (control signals)
 3. V_{DD} = 3.3V, all output pins = open, all input pins = V_{DD} or V_{SS}

Switching Characteristics at Ta = 0 to +70°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, C_L = 15pF

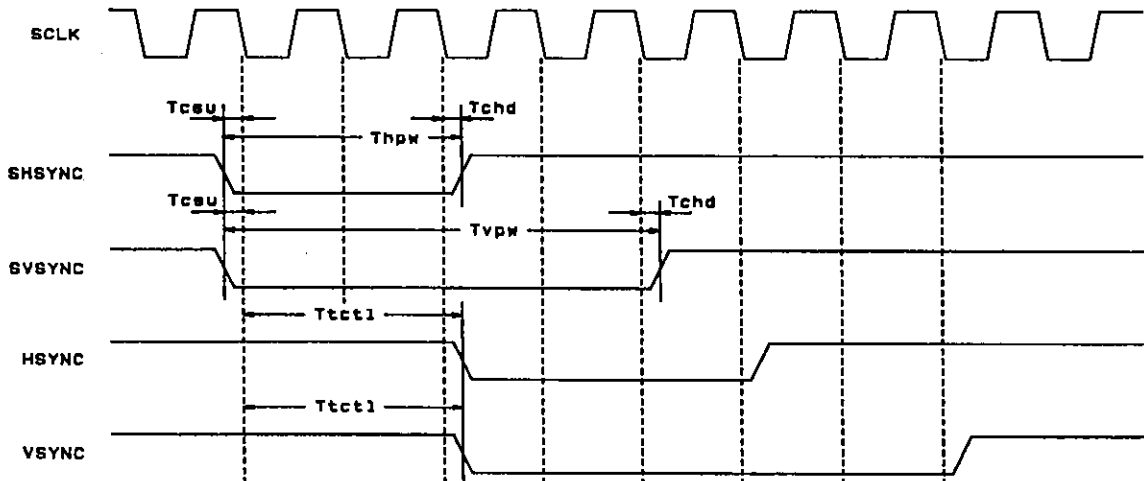
| Parameter | Symbol | min | typ | max | Unit |
|---------------------------------------|--------|-----------|------------|------------|------|
| Dot clock cycle time | Tdclk | 33 | – | – | ns |
| Hsync low-level pulse width | Thpw | 2Tdclk | – | – | ns |
| Vsync low-level pulse width | Tvpw | 2Tdclk | – | – | ns |
| Data setup time | Tdsu | 10 | – | – | ns |
| Data hold time | Tdhd | 10 | – | – | ns |
| Control signal setup time | Tcsu | 10 | – | – | ns |
| Control signal hold time | Tchd | 10 | – | – | ns |
| CLK propagation delay time | Tdhh | 5 | 10 | 23 | ns |
| CLK propagation delay time | Tdll | 5 | 10 | 23 | ns |
| CLKB propagation delay time | Tdhl | 5 | 11 | 25 | ns |
| CLKB propagation delay time | Tdhlh | 5 | 10 | 22 | ns |
| Control signal propagation delay time | Ttcl | 5Tclk + 5 | 5Tclk + 10 | 5Tclk + 25 | ns |
| Data output propagation delay time | Ttdata | 5Tclk + 5 | 5Tclk + 11 | 5Tclk + 27 | ns |

Timing Diagrams



A03728

SSIGNAL refers to the SHDEN, SCTL, BYPASS and PWRSV signals.
SIGNAL refers to the HDEN and CTL signals.



A03729

Usage Note

Since this LSI performs spatial modulation using an error diffusion algorithm, patterns that differ from the original images may be displayed for certain display pattern and gray-scale mode combinations.

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees, jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of March, 1996. Specifications and information herein are subject to change without notice.