

M66313FP

32-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

DESCRIPTION

The M66313FP is a semiconductor integrated circuit for LED array driver with 32-bit serial-input, parallel-output shift register, equipped with direct set input and output latches.

The M66313FP guarantees sufficient 24mA output current to drive anode common LED, allowing 32-bit simultaneous and continuous current output.

The parallel outputs are open-drain outputs.

The M66313FP employs CMOS technology, allowing considerable reduction of power dissipation, compared to previous BIPOLAR or Bi-CMOS products.

In addition, the pin configuration is suitable for easy wiring on the printed circuit board.

FEATURES

- High output current
All parallel output $I_{OL} = +24\text{mA}$, LEDs can be turned on simultaneously.
- Low power dissipation : 200 μW /package (max)
($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, quiescent state)
- High noise margin
Employment of Schmitt-trigger circuit on all inputs allows application with long wiring.
- Direct set input ($\overline{S_D}$)
- Open-drain output ($\overline{Q_1} \sim \overline{Q_{32}}$)
- Serial data output for cascading (SQ_{32})
- Wide operating temperature range ($T_a = -40 \sim +85^\circ\text{C}$)
- Pin configuration for easy layout on PCB.
(Pin configuration allows easy cascade connection or LED connection)

APPLICATION

LED array drive for eraser unit of a copying machine
LED array drive of a button telephone set
Various LED modules

FUNCTION

The employment of silicon gate CMOS process of the M66313FP guarantees low power dissipation and maintains high noise margin as well as high output current and high speed required to drive LEDs.

Each shift register bit consists of a flip-flop for shifting and an output latch.

The shift operation takes place when the clock input CK changes from low-level to high-level.

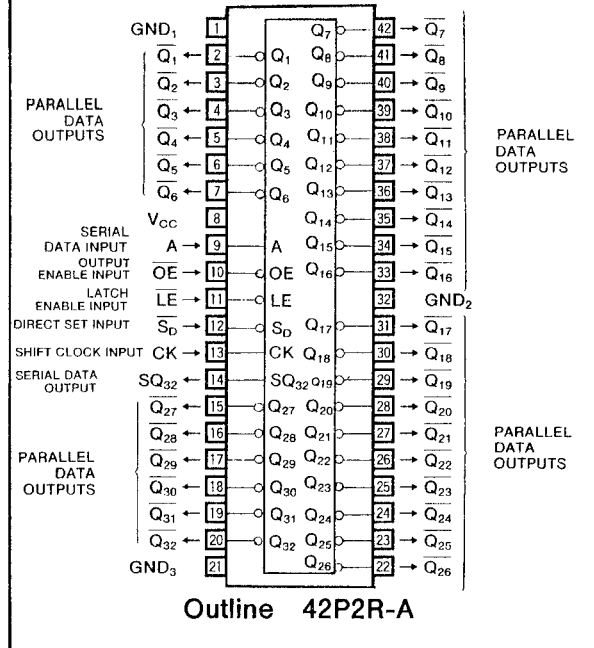
The serial data input A corresponds to the data input of the first-stage shift register, and the shift register is shifted in sequence when a pulse is applied to CK.

The parallel outputs $\overline{Q_1} \sim \overline{Q_{32}}$ are open-drain outputs.

If the latch-enable input \overline{LE} is turned high-level, the content of the shift register at that instant is latched.

To expand the number of bits, use the serial data output SQ_{32} which shows the output of the shift register of the

PIN CONFIGURATION (TOP VIEW)

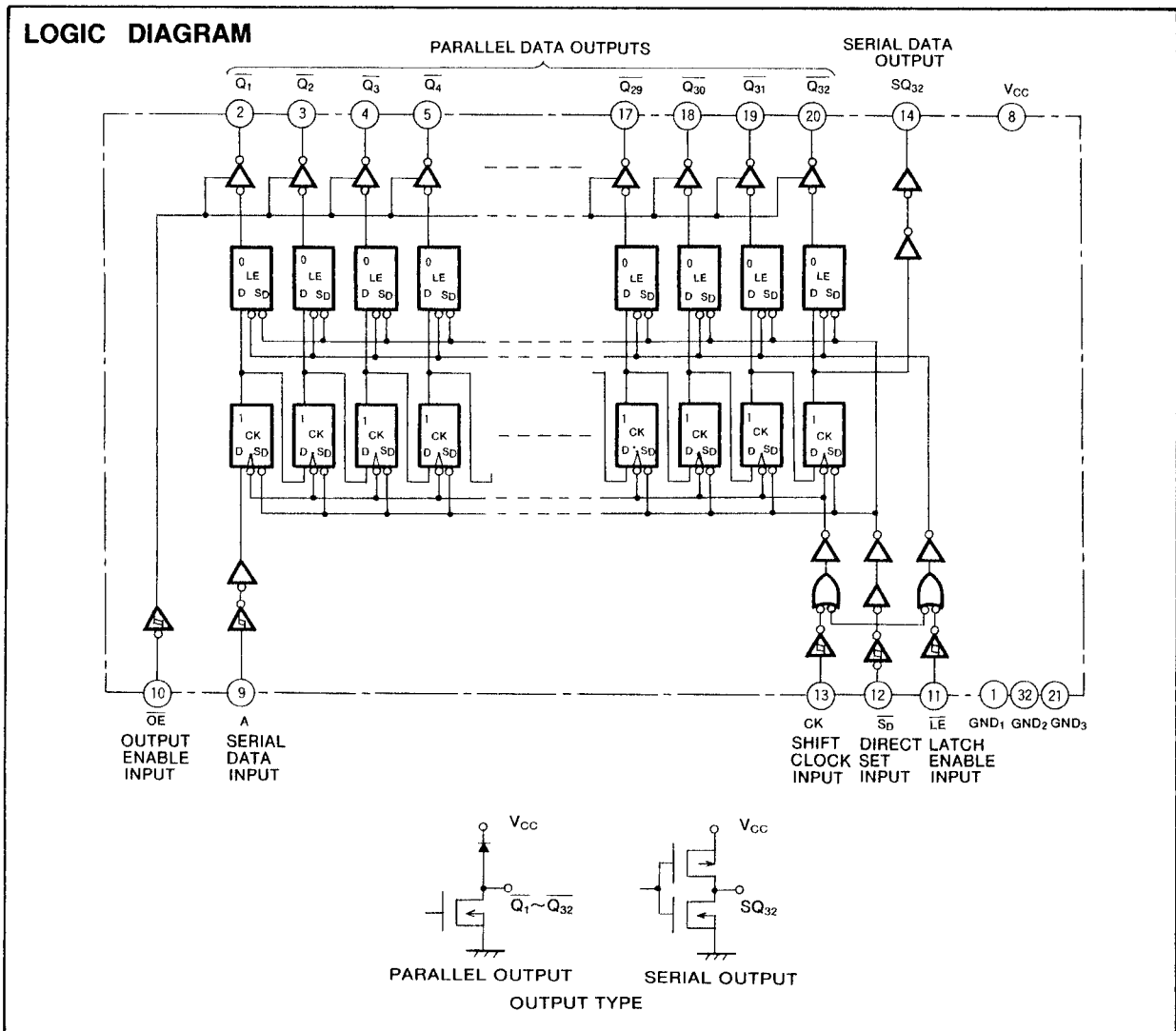


32nd bit.

If the direct set input $\overline{S_D}$ is turned low-level, shift register and latches are set.

If the high-level input is applied to the output enable input \overline{OE} , $\overline{Q_1} \sim \overline{Q_{32}}$ are set to the high-impedance state, but SQ_{32} is not set to the high-impedance state. The shift operation is not affected when \overline{OE} is changed.

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FUNCTIONAL TABLE (Note 1)

OPERATION MODE	INPUT					PARALLEL OUTPUTS																																SERIAL OUTPUT SQ32		
	S _D	CK	LE	A	OE	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	Q ₈	Q ₉	Q ₁₀	Q ₁₁	Q ₁₂	Q ₁₃	Q ₁₄	Q ₁₅	Q ₁₆	Q ₁₇	Q ₁₈	Q ₁₉	Q ₂₀	Q ₂₁	Q ₂₂	Q ₂₃	Q ₂₄	Q ₂₅	Q ₂₆	Q ₂₇	Q ₂₈	Q ₂₉	Q ₃₀	Q ₃₁	Q ₃₂			
SET	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
SHIFT	H	↑	L	H	L	L	Q ⁰ ₁	Q ⁰ ₂	Q ⁰ ₃	Q ⁰ ₄	Q ⁰ ₅	Q ⁰ ₆	Q ⁰ ₇	Q ⁰ ₈	Q ⁰ ₉	Q ⁰ ₁₀	Q ⁰ ₁₁	Q ⁰ ₁₂	Q ⁰ ₁₃	Q ⁰ ₁₄	Q ⁰ ₁₅	Q ⁰ ₁₆	Q ⁰ ₁₇	Q ⁰ ₁₈	Q ⁰ ₁₉	Q ⁰ ₂₀	Q ⁰ ₂₁	Q ⁰ ₂₂	Q ⁰ ₂₃	Q ⁰ ₂₄	Q ⁰ ₂₅	Q ⁰ ₂₆	Q ⁰ ₂₇	Q ⁰ ₂₈	Q ⁰ ₂₉	Q ⁰ ₃₀	Q ⁰ ₃₁	Q ⁰ ₃₂		
	H	↑	L	L	L	Z	q ⁰ ₁	q ⁰ ₂	q ⁰ ₃	q ⁰ ₄	q ⁰ ₅	q ⁰ ₆	q ⁰ ₇	q ⁰ ₈	q ⁰ ₉	q ⁰ ₁₀	q ⁰ ₁₁	q ⁰ ₁₂	q ⁰ ₁₃	q ⁰ ₁₄	q ⁰ ₁₅	q ⁰ ₁₆	q ⁰ ₁₇	q ⁰ ₁₈	q ⁰ ₁₉	q ⁰ ₂₀	q ⁰ ₂₁	q ⁰ ₂₂	q ⁰ ₂₃	q ⁰ ₂₄	q ⁰ ₂₅	q ⁰ ₂₆	q ⁰ ₂₇	q ⁰ ₂₈	q ⁰ ₂₉	q ⁰ ₃₀	q ⁰ ₃₁	q ⁰ ₃₂		
LATCH	H	X	H	X	L	Q ⁰ ₁	Q ⁰ ₂	Q ⁰ ₃	Q ⁰ ₄	Q ⁰ ₅	Q ⁰ ₆	Q ⁰ ₇	Q ⁰ ₈	Q ⁰ ₉	Q ⁰ ₁₀	Q ⁰ ₁₁	Q ⁰ ₁₂	Q ⁰ ₁₃	Q ⁰ ₁₄	Q ⁰ ₁₅	Q ⁰ ₁₆	Q ⁰ ₁₇	Q ⁰ ₁₈	Q ⁰ ₁₉	Q ⁰ ₂₀	Q ⁰ ₂₁	Q ⁰ ₂₂	Q ⁰ ₂₃	Q ⁰ ₂₄	Q ⁰ ₂₅	Q ⁰ ₂₆	Q ⁰ ₂₇	Q ⁰ ₂₈	Q ⁰ ₂₉	Q ⁰ ₃₀	Q ⁰ ₃₁	Q ⁰ ₃₂			
OUTPUT DIS-ABLE	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Q ₃₂

Note 1 ↑ : Transition from low-to-high-level.
 Q⁰ : Shows the status of output Q before CK input changes.
 X : Irrelevant
 q⁰ : The content of shift register before CK changes.
 q : The content of the shift register.
 Z : High-impedance state.

ABSOLUTE MAXIMUM RATINGS (T_a = -40~+85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{CC} +0.5	V
V _O	Output voltage		-0.5~V _{CC} +0.5	V
I _{IK}	Input protection diode current	V _I < 0V	-20	mA
		V _I > V _{CC}	20	
I _{OK}	Output parasitic diode current	V _O < 0V	-20	mA
		V _O > V _{CC}	20	
I _O	Output current	Q ₁ ~Q ₃₂	50	mA
		SQ ₃₂	±25	
I _{CC}	Supply/GND current	V _{CC} , GND	-920, +20	mA
P _d	Power dissipation		650	mW
T _{stg}	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
T _{opr}	Operating free-air ambient temperature range	-40		+85	°C

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ELECTRICAL CHARACTERISTICS (V_{CC}=4.5~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits					Unit	
			T _a =25°C			T _a =-40~+85°C			
			Min	Typ*	Max	Min	Max		
V _{T+}	Positive-going threshold voltage	V _O = 0.1V, V _{CC} -0.1V I _O = 20μA	0.35XV _{CC}	2.8	0.7XV _{CC}	0.35XV _{CC}	0.7XV _{CC}	V	
V _{T-}	Negative-going threshold voltage	V _O = 0.1V, V _{CC} -0.1V I _O = 20μA	0.2XV _{CC}	2	0.55XV _{CC}	0.2XV _{CC}	0.55XV _{CC}	V	
V _{OH}	High-level output voltage	SQ ₃₂ V _I = V _{T+} , V _{T-} V _{CC} =4.5V	I _{OH} =-20μA I _{OH} =-4mA	V _{CC} -0.1 3.83		V _{CC} -0.1 3.66		V	
V _{OL}	Low-level output voltage	Q ₁ ~Q ₃₂ V _I = V _{T+} , V _{T-} V _{CC} =4.5V	I _{OL} =20μA		0.1		0.1	V	
			I _{OL} =24mA		0.20		0.41		
			I _{OL} =28mA		0.25		0.48		0.55(Note 2)
			I _{OL} =20μA				0.1		0.1
	SQ ₃₂		I _{OL} =4mA			0.44		0.53	
I _{IH}	High-level input current	V _I =V _{CC} , V _{CC} =5.5V			0.5			5.0	μA
I _{IL}	Low-level input current	V _I =GND, V _{CC} =5.5V			-0.5			-5.0	μA
I _O	Maximum output leak current	V _I =V _{T+} , V _{T-} V _{CC} =5.5V	V _O =V _{CC} V _O =GND			1.0 -1.0		10.0 -10.0	μA
I _{CC}	Quiescent state dissipation current	V _I =V _{CC} , GND V _{CC} =5.5V			40.0			400.0	μA

* : All typical values are at V_{CC}=5V, T_a=25°C
 Note 2 : T_a=-40~+70°C

SWITCHING CHARACTERISTICS (V_{CC}= 5V)

Symbol	Parameter	Test conditions	Limits					Unit
			T _a =25°C			T _a =-40~+85°C		
			Min	Typ	Max	Min	Max	
f _{max}	Maximum clock frequency		5	30		4		MHz
t _{PZL}	Output enable time to low-level	CK-Q ₁ ~Q ₃₂ (Turned on)		35	150		200	ns
t _{PLZ}	Output disable time from low-level	CK-Q ₁ ~Q ₃₂ (Turned off)		35	200		250	ns
t _{PLH}	Low-to-high, high-to-low output propagation time	CK-SQ ₃₂		35	100		130	ns
t _{PHL}				40	100		130	ns
t _{PZL}	Output enable time to low-level	S _D -Q ₁ ~Q ₃₂ (Turned on)		35	150		200	ns
t _{PLH}	Low-to-high output propagation time	S _D -SQ ₃₂		40	100		130	ns
t _{PZL}	Output enable time to low-level	LE-Q ₁ ~Q ₃₂ (Turned on)		30	100		130	ns
t _{PLZ}	Output disable time from low-level	LE-Q ₁ ~Q ₃₂ (Turned off)		35	150		200	ns
t _{PZL}	Output enable time to low-level	OE-Q ₁ ~Q ₃₂ (Turned on)		30	100		130	ns
t _{PLZ}	Output disable time from low-level	OE-Q ₁ ~Q ₃₂ (Turned off)		35	150		200	ns
C _I	Input capacitance			3	10		10	pF
C _O	Output capacitance	OE=V _{CC}		6	15		15	pF
C _{PD}	Power dissipation capacitance(Note 4)			160				pF

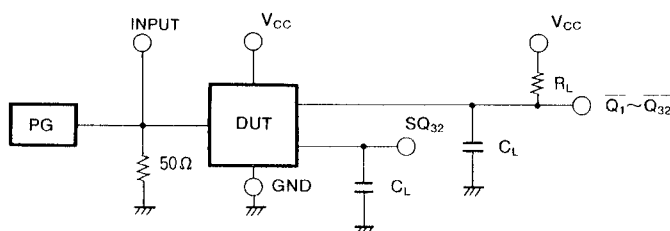
Note 4 : C_{PD} is the equivalent capacitance of IC calculated by the operating power dissipation without load. The operating power dissipation without load is given as follows:
 $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

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TIMING REQUIREMENT ($V_{CC}=5V$)

Symbol	Parameter	Test conditions	Limits					Unit
			$T_a=25^{\circ}C$			$T_a=-40\sim+85^{\circ}C$		
			Min	Typ	Max	Min	Max	
t_w	CK, LE, $\overline{S_D}$ pulse width	(Note 3)	100	16		130		ns
t_{su}	Setup time A to CK		100	27		130		ns
t_h	Hold time A to CK		10	5		15		ns
	Hold time LE to CK		50	15		70		
t_{rec}	Recovery time CK to $\overline{S_D}$		50	20		70		ns

Note 3 : Test circuit



- (1) Characteristics of pulse generator(PG): $t_r=6\text{ ns}$, $t_f=6\text{ ns}$
- (2) C_L includes probe and jig capacitance.

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TIMING DIAGRAM

