Hex Schmitt Trigger

The MC14106B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14106B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Increased Hysteresis Voltage Over the MC14584B
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace the MC14584B or MC14069UB

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

	<u> </u>		
Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 2.)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating: Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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DIAGRAMS



PDIP-14 P SUFFIX CASE 646



MARKING



SOIC-14 D SUFFIX CASE 751A





TSSOP-14 DT SUFFIX CASE 948G



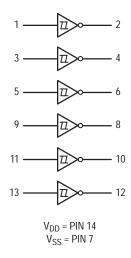
A = Assembly Location

WL or L = Wafer Lot YY or Y = Year WW or W = Work Week

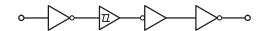
ORDERING INFORMATION

Device	Package	Shipping		
MC14106BCP	PDIP-14	2000/Box		
MC14106BD	SOIC-14	55/Rail		
MC14106BDR2	SOIC-14	2500/Tape & Reel		
MC14106BDT	TSSOP-14	96/Rail		
MC14106BDTR2	TSSOP-14	2500/Tape & Reel		

LOGIC DIAGRAM



EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

			V _{DD}	– 55°C			25°C		125°C		
Characteristic	С	Symbol	Vdc	Min	Max	Min	Тур (3.)	Max	Min	Max	Unit
Output Voltage V _{in} = V _{DD}	"0" Level	V _{OL}	5.0 10 15	_ _ _	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	_ _ _	0.05 0.05 0.05	Vdc
V _{in} = 0	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	_ _ _	Vdc
Hysteresis Voltage		V _H ^(6.)	5.0 10 15	0.3 1.2 1.6	2.0 3.4 5.0	0.3 1.2 1.6	1.1 1.7 2.1	2.0 3.4 5.0	0.3 1.2 1.6	2.0 3.4 5.0	Vdc
Threshold Voltage Positive–Going		V _{T+}	5.0 10 15	2.2 4.6 6.8	3.6 7.1 10.8	2.2 4.6 6.8	2.9 5.9 8.8	3.6 7.1 10.8	2.2 4.6 6.8	3.6 7.1 10.8	Vdc
Negative–Going		V _T	5.0 10 15	0.9 2.5 4.0	2.8 5.2 7.4	0.9 2.5 4.0	1.9 3.9 5.8	2.8 5.2 7.4	0.9 2.5 4.0	2.8 5.2 7.4	Vdc
Output Drive Current $ (V_{OH} = 2.5 \text{ Vdc}) $ $ (V_{OH} = 4.6 \text{ Vdc}) $ $ (V_{OH} = 9.5 \text{ Vdc}) $ $ (V_{OH} = 13.5 \text{ Vdc}) $	Source	I _{OH}	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	_ _ _ _	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	_ _ _ _	- 1.7 - 0.36 - 0.9 - 2.4	_ _ _ _	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I _{OL}	5.0 10 15	0.64 1.6 4.2	_ _ _	0.51 1.3 3.4	0.88 2.25 8.8	_ _ _	0.36 0.9 2.4	_ _ _	mAdc
Input Current		I _{in}	15	_	± 0.1	_	±0.00001	± 0.1	_	± 1.0	μAdc
Input Capacitance (V _{in} = 0)		C _{in}	_	_	_	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)		I _{DD}	5.0 10 15	_ _ _	0.25 0.5 1.0	_ _ _	0.0005 0.0010 0.0015	0.25 0.5 1.0	_ _ _	7.5 15 30	μAdc
Total Supply Current (4.) (Dynamic plus Quiese Per Package) (C _L = 50 pF on all out buffers switching)	cent,	I _T	5.0 10 15			$I_T = (3)$	I.8 μΑ/kHz) f 3.6 μΑ/kHz) f 5.4 μΑ/kHz) f	+ I _{DD}			μAdc

^{3.} Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

6. $V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less that $V_{T+} = V_{T-} = V_{T-}$

^{4.} The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

SWITCHING CHARACTERISTICS ($C_L = 50 \ pF, \ T_A = 25 \ ^{\circ}C)$

Characteristic	Symbol	V _{DD} Vdc	Min	Typ ^(7.)	Max	Unit
Output Rise Time	t _{TLH}	5.0 10 15		100 50 40	200 100 80	ns
Output Fall Time	t _{THL}	5.0 10 15		100 50 40	200 100 80	ns
Propagation Delay Time	t _{PLH} , t _{PHL}	5.0 10 15		125 50 40	250 100 80	ns

^{7.} Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

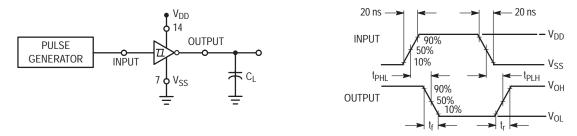


Figure 1. Switching Time Test Circuit and Waveforms

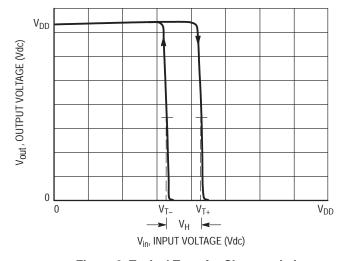
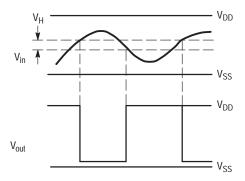
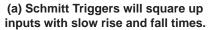


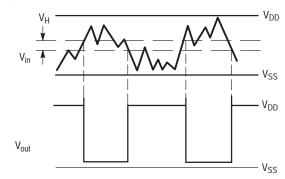
Figure 2. Typical Transfer Characteristics

APPLICATIONS



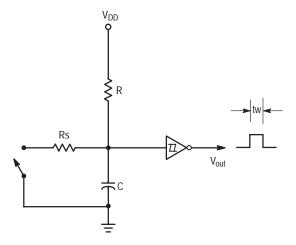


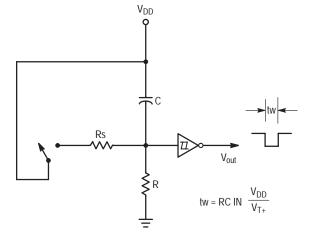




(b) A Schmitt trigger offers maximum noise immunity in gate applications.

Figure 3.





Useful as Pushbutton/Keyboard Debounce Circuit.

Figure 4. Monostable Multivibrator

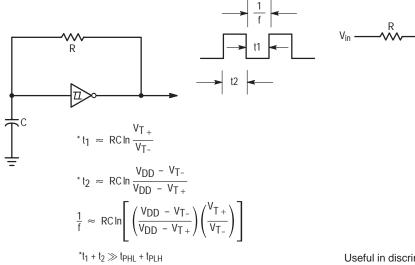


Figure 5. Astable Multivibrator

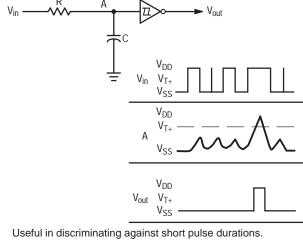
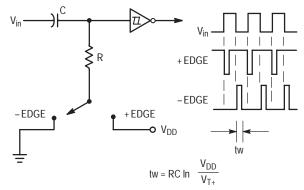


Figure 6. Integrator



Useful as an edge detector circuit.

Figure 7. Differentiator

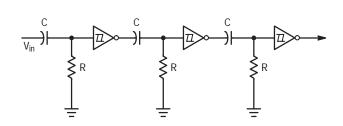
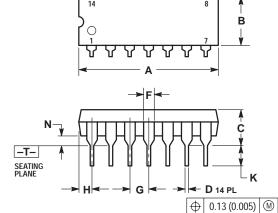


Figure 8. Positive Edge Time Delay Circuit

PACKAGE DIMENSIONS

P SUFFIX

PLASTIC DIP PACKAGE CASE 646-06 **ISSUE M**

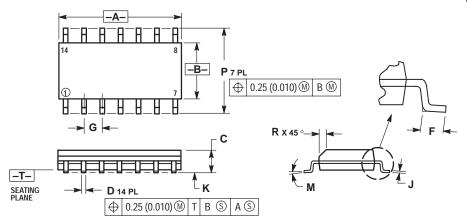




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- 5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.715	0.770	18.16	18.80
В	0.240	0.260	6.10	6.60
С	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100	BSC	2.54 BSC	
Н	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M		10°		10°
N	0.015	0.039	0.38	1.01

D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
 Y14.5M, 1982.

- Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

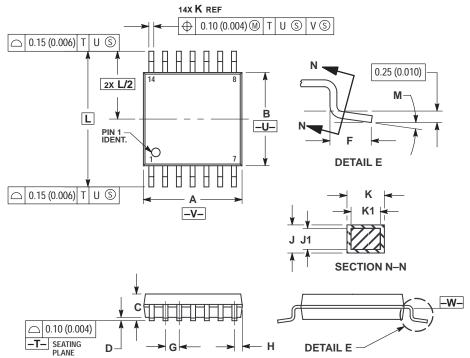
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		INC	HES
MIN	MAX	MIN	MAX
8.55	8.75	0.337	0.344
3.80	4.00	0.150	0.157
1.35	1.75	0.054	0.068
0.35	0.49	0.014	0.019
0.40	1.25	0.016	0.049
1.27	1.27 BSC		BSC
0.19	0.25	0.008	0.009
0.10	0.25	0.004	0.009
0 °	7°	0°	7°
5.80	6.20	0.228	0.244
0.25	0.50	0.010	0.019
	MIN 8.55 3.80 1.35 0.35 0.40 1.27 0.19 0.10 0 ° 5.80	8.55 8.75 3.80 4.00 1.35 1.75 0.35 0.49 0.40 1.25 1.27 BSC 0.19 0.25 0.0 0.25 0 0 7° 5.80 6.20	MIN MAX MIN 8.55 8.75 0.337 3.80 4.00 0.150 1.35 1.75 0.054 0.35 0.49 0.014 0.40 1.25 0.016 1.27 BSC 0.055 0.05 0.19 0.25 0.008 0.10 0.25 0.004 0 ° 7 ° 0 ° 7 ° 0 ° 5 5.80 6.20 0.228

PACKAGE DIMENSIONS

DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948G-01 ISSUE O



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (N DOA) PEP SIDE.
- 0.15 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED

 0.25 (0.010) PER SIDE.
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE

DETERMINED AT DATUM PLANE -W						
	MILLIMETERS		INCHES			
DIM	MIN	MAX	MIN	MAX		
Α	4.90	5.10	0.193	0.200		
В	4.30	4.50	0.169	0.177		
С		1.20		0.047		
D	0.05	0.15	0.002	0.006		
F	0.50	0.75	0.020	0.030		
G	0.65 BSC		0.026 BSC			
Н	0.50	0.60	0.020	0.024		
J	0.09	0.20	0.004	0.008		
J1	0.09	0.16	0.004	0.006		
K	0.19	0.30	0.007	0.012		
K1	0.19	0.25	0.007	0.010		
L	6.40 BSC		0.252	BSC		
M	0°	8°	0°	8°		

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