MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Document order number: MC33887
Rev 9.0, 10/2004

5.0 A H-Bridge with Load Current Feedback

33887

5.0 A H-BRIDGE WITH LOAD CURRENT FEEDBACK

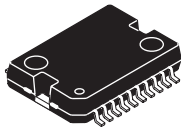
The 33887 is a monolithic H-Bridge Power IC with a load current feedback feature making it ideal for closed-loop DC motor control. The IC incorporates internal control logic, charge pump, gate drive, and low $R_{DS(ON)}$ MOSFET output circuitry. The 33887 is able to control inductive loads with continuous DC load currents up to 5.0 A, and with peak current active limiting between 5.2 A and 7.8 A. Output loads can be pulse width modulated (PWM-ed) at frequencies up to 10 kHz. The load current feedback feature provides a proportional (1/375th of the load current) constant-current output suitable for monitoring by a microcontroller's A/D input. This feature facilitates the design of closed-loop torque/speed control as well as open load detection.

A Fault Status output terminal reports undervoltage, short circuit, and overtemperature conditions. Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two disable inputs force the H-Bridge outputs to tri-state (exhibit high impedance).

The 33887 is parametrically specified over a temperature range of $-40°C \le T_A \le 125°C$ and a voltage range of $5.0\ V \le V+ \le 28\ V$. The IC can also be operated up to 40 V with derating of the specifications.

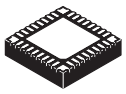
Features

- 5.0 V to 40 V Continuous Operation
- 120 mΩ $R_{DS(ON)}$ H-Bridge MOSFETs
- TTL/CMOS Compatible Inputs
- PWM Frequencies up to 10 kHz
- Active Current Limiting (Regulation) via Internal Constant OFF-Time PWM (with Temperature-Dependent Threshold Reduction)
- Output Short Circuit Protection (Short to V+ or Short to GND)
- Undervoltage Shutdown
- Fault Status Reporting
- Sleep Mode with Current Draw ≤50 μA (Inputs Floating or Set to Match Default Logic States)
- Pb-Free Packaging Designated by Suffix Codes VW and PNB

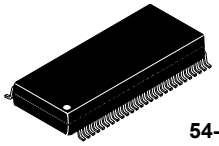


DH SUFFIX
VW (Pb-FREE) SUFFIX
CASE 979-04
20-TERMINAL HSOP

PNB (Pb-FREE) SUFFIX
CASE 1503-01
36-TERMINAL PQFN



Bottom View

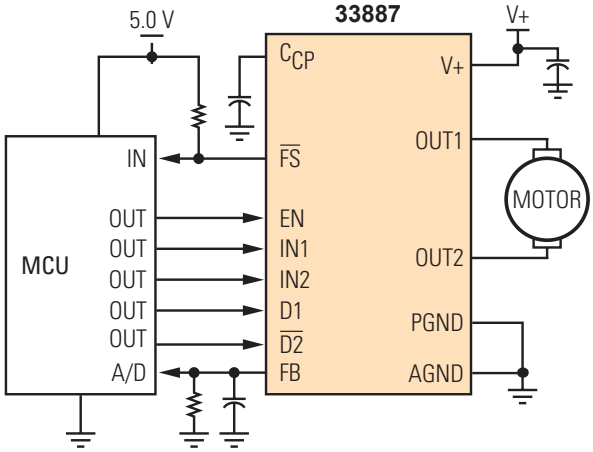


DWB SUFFIX
CASE 1390-01
54-TERMINAL SOICW-EP

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33887DH/R2	-40°C to 125°C	20 HSOP
PC33887VW/R2		
MC33887PNB/R2		36 PQFN
MC33887DWB/R2		54 SOICW-EP

33887 Simplified Application Diagram



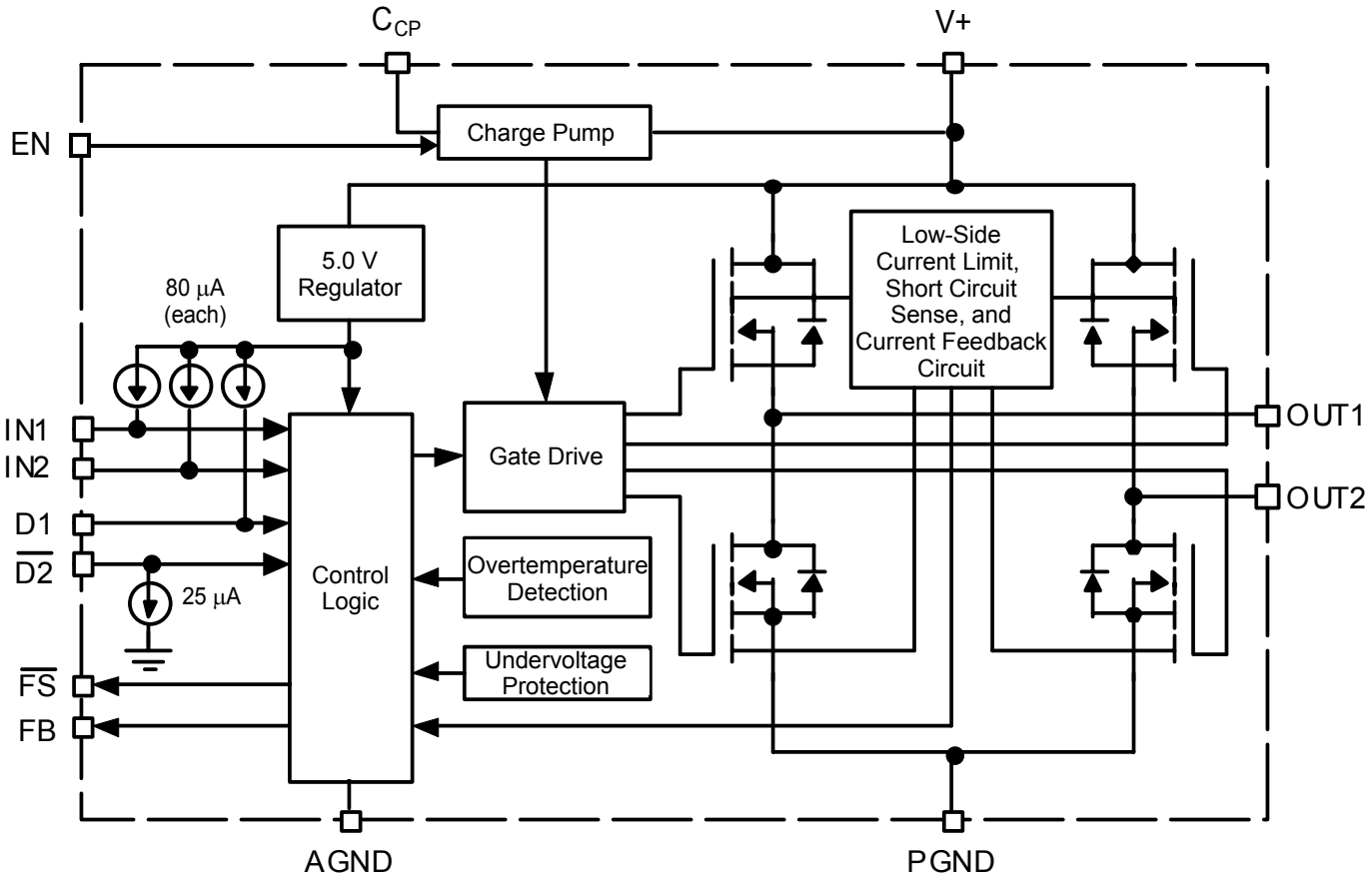
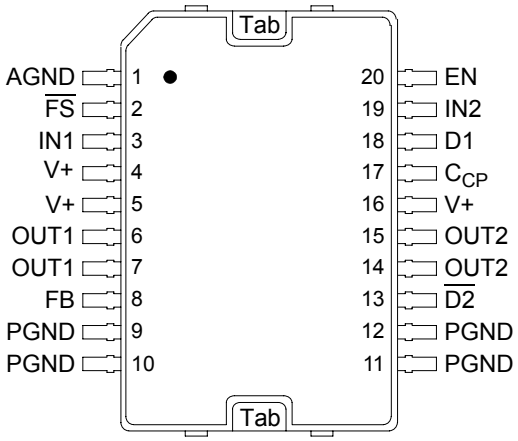


Figure 1. 33887 Simplified Internal Block Diagram

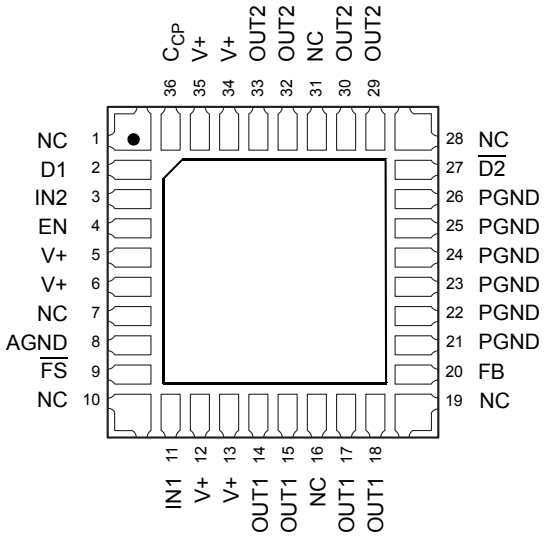


HSOP TERMINAL DEFINITIONS

A functional description of each terminal can be found in the System/Application Information section, page 19.

Terminal	Terminal Name	Formal Name	Definition
1	AGND	Analog Ground	Low-current analog signal ground.
2	$\overline{FS}$	Fault Status for H-Bridge	Open drain active LOW Fault Status output requiring a pullup resistor to 5.0 V.
3	IN1	Logic Input Control 1	Logic input control of OUT1 (i.e., IN1 logic HIGH = OUT1 HIGH).
4, 5, 16	V+	Positive Power Supply	Positive supply connections
6, 7	OUT1	H-Bridge Output 1	Output 1 of H-Bridge.
8	FB	Feedback for H-Bridge	Current sensing feedback output providing ground referenced 1/375th (0.00266) of H-Bridge high-side current.
9–12	PGND	Power Ground	High-current power ground.
13	$\overline{D2}$	Disable 2	Active LOW input used to simultaneously tri-state disable both H-Bridge outputs. When $\overline{D2}$ is Logic LOW, both outputs are tri-stated.
14, 15	OUT2	H-Bridge Output 2	Output 2 of H-Bridge.
17	C_{CP}	Charge Pump Capacitor	External reservoir capacitor connection for internal charge pump capacitor.
18	D1	Disable 1	Active HIGH input used to simultaneously tri-state disable both H-Bridge outputs. When D1 is Logic HIGH, both outputs are tri-stated.
19	IN2	Logic Input Control 2	Logic input control of OUT2 (i.e., IN2 logic HIGH = OUT2 HIGH).
20	EN	Enable	Logic input Enable control of device (i.e., EN logic HIGH = full operation, EN logic LOW = Sleep Mode).
Tab/Pad	Thermal Interface	Exposed Pad Thermal Interface	Exposed pad thermal interface for sinking heat from the device. **Note** Must be DC-coupled to analog ground and power ground via very low impedance path to prevent injection of spurious signals into IC substrate.

Transparent Top View of Package

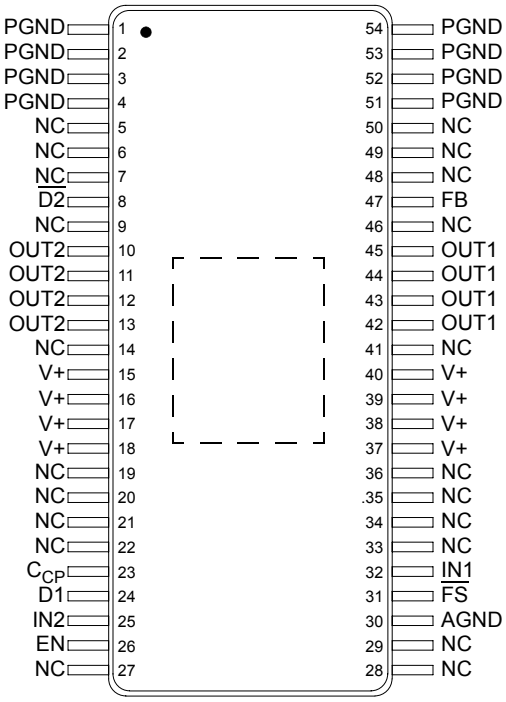


PQFN TERMINAL DEFINITIONS

A functional description of each terminal can be found in the System/Application Information section, page 19.

Terminal	Terminal Name	Formal Name	Definition
1, 7, 10, 16, 19, 28, 31	NC	No Connect	No internal connection to this terminal.
2	D1	Disable 1	Active HIGH input used to simultaneously tri-state disable both H-Bridge outputs. When D1 is Logic HIGH, both outputs are tri-stated.
3	IN2	Logic Input Control 2	Logic input control of OUT2 (i.e., IN2 logic HIGH = OUT2 HIGH).
4	EN	Enable	Logic input Enable control of device (i.e., EN logic HIGH = full operation, EN logic LOW = Sleep Mode).
5, 6, 12, 13, 34, 35	V+	Positive Power Supply	Positive supply connections.
8	AGND	Analog Ground	Low-current analog signal ground.
9	$\overline{FS}$	Fault Status for H-Bridge	Open drain active LOW Fault Status output requiring a pullup resistor to 5.0 V.
11	IN1	Logic Input Control 1	Logic input control of OUT1 (i.e., IN1 logic HIGH = OUT1 HIGH).
14, 15, 17, 18	OUT1	H-Bridge Output 1	Output 1 of H-Bridge.
20	FB	Feedback for H-Bridge	Current feedback output providing ground referenced 1/375th ratio of H-Bridge high-side current.
21–26	PGND	Power Ground	High-current power ground.
27	$\overline{D2}$	Disable 2	Active LOW input used to simultaneously tri-state disable both H-Bridge outputs. When $\overline{D2}$ is Logic LOW, both outputs are tri-stated.
29, 30, 32, 33	OUT2	H-Bridge Output 2	Output 2 of H-Bridge.
36	C_{CP}	Charge Pump Capacitor	External reservoir capacitor connection for internal charge pump capacitor.
Pad	Thermal Interface	Exposed Pad Thermal Interface	Exposed pad thermal interface for sinking heat from the device. **Note** Must be DC-coupled to analog ground and power ground via very low impedance path to prevent injection of spurious signals into IC substrate.

Transparent Top View of Package



SOICW-EP TERMINAL DEFINITIONS

A functional description of each terminal can be found in the System/Application Information section, page 19.

Terminal	Terminal Name	Formal Name	Definition
1–4, 51–54	PGND	Power Ground	High-current power ground.
5–7, 9, 14, 19–22, 27–29, 33–36, 41, 46, 48–50	NC	No Connect	No internal connection to this terminal.
8	$\overline{D2}$	Disable 2	Active LOW input used to simultaneously tri-state disable both H-Bridge outputs. When $\overline{D2}$ is Logic LOW, both outputs are tri-stated.
10–13	OUT2	H-Bridge Output 2	Output 2 of H-Bridge.
15–18, 37–40	V+	Positive Power Supply	Positive supply connections.
23	C_{CP}	Charge Pump Capacitor	External reservoir capacitor connection for internal charge pump capacitor.
24	D1	Disable 1	Active HIGH input used to simultaneously tri-state disable both H-Bridge outputs. When D1 is Logic HIGH, both outputs are tri-stated.
25	IN2	Logic Input Control 2	Logic input control of OUT2 (i.e., IN2 logic HIGH = OUT2 HIGH).
26	EN	Enable	Logic input Enable control of device (i.e., EN logic HIGH = full operation, EN logic LOW = Sleep Mode).
30	AGND	Analog Ground	Low-current analog signal ground.
31	$\overline{FS}$	Fault Status for H-Bridge	Open drain active LOW Fault Status output requiring a pullup resistor to 5.0 V.
32	IN1	Logic Input Control 1	Logic input control of OUT1 (i.e., IN1 logic HIGH = OUT1 HIGH).
42–45	OUT1	H-Bridge Output 1	Output 1 of H-Bridge.
47	FB	Feedback for H-Bridge	Current feedback output providing ground referenced 1/375th ratio of H-Bridge high-side current.
Pad	Thermal Interface	Exposed Pad Thermal Interface	Exposed pad thermal interface for sinking heat from the device. **Note** Must be DC-coupled to analog ground and power ground via very low impedance path to prevent injection of spurious signals into IC substrate.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage	V+	40	V
Input Voltage (Note 1)	V_{IN}	-0.3 to 7.0	V
$\overline{FS}$ Status Output (Note 2)	$V_{\overline{FS}}$	7.0	V
Continuous Current (Note 3)	I_{OUT}	5.0	A
DH Suffix HSOP ESD Voltage			V
Human Body Model (Note 4)			
Each Terminal to AGND	V_{ESD1}	±1000	
Each Terminal to PGND	V_{ESD1}	±1500	
Each Terminal to V+	V_{ESD1}	±2000	
Each I/O to All Other I/Os	V_{ESD1}	±2000	
Machine Model (Note 5)	V_{ESD2}	±200	
VW Suffix HSOP ESD Voltage			V
Human Body Model (Note 4)	V_{ESD1}	±2000	
Machine Model (Note 5)	V_{ESD2}	±200	
PQFN ESD Voltage			V
Human Body Model (Note 4)	V_{ESD1}	±2000	
Machine Model (Note 5)	V_{ESD2}	±200	
SOICW-EP ESD Voltage			V
Human Body Model (Note 4)	V_{ESD1}	±1600	
Machine Model (Note 5)	V_{ESD2}	±200	
THERMAL RATINGS			
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature (Note 6)			°C
Ambient	T_A	-40 to 125	
Junction	T_J	-40 to 150	
Peak Package Reflow Temperature During Solder Mounting (Note 7)	T_{SOLDER}		°C
HSOP		220	
PQFN		260	
SOICW-EP		240	

Notes

1. Exceeding the input voltage on IN1, IN2, EN, D1, or $\overline{D2}$ may cause a malfunction or permanent damage to the device.
2. Exceeding the pullup resistor voltage on the open Drain $\overline{FS}$ terminal may cause permanent damage to the device.
3. Continuous current capability so long as junction temperature is ≤ 150°C.
4. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
5. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
6. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking provided. Brief nonrepetitive excursions of junction temperature above 150°C can be tolerated as long as duration does not exceed 30 seconds maximum. (nonrepetitive events are defined as not occurring more than once in 24 hours.)
7. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

MAXIMUM RATINGS (continued)

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
THERMAL RESISTANCE (AND PACKAGE DISSIPATION) RATINGS (Note 8), (Note 9), (Note 10), (Note 11)			
Junction-to-Board (Bottom Exposed Pad Soldered to Board) HSOP (6.0 W) PQFN (4.0 W) SOICW-EP (2.0 W)	$R_{\theta JB}$	 ~5.0 ~4.3 ~8.0	°C/W
Junction-to-Ambient, Natural Convection, Single-Layer Board (1s) (Note 12) HSOP (6.0 W) PQFN (4.0 W) SOICW-EP (2.0 W)	$R_{\theta JA}$	 ~41 ~TBD ~62	°C/W
Junction-to-Ambient, Natural Convection, Four-Layer Board (2s2p) (Note 13) HSOP (6.0 W) PQFN (4.0 W) SOICW-EP (2.0 W)	$R_{\theta JMA}$	 ~30 ~21.3 ~TBD	°C/W
Junction-to-Case (Exposed Pad) (Note 14) HSOP (6.0 W) PQFN (4.0 W) SOICW-EP (2.0 W)	$R_{\theta JC}$	 ~0.5 ~0.9 ~1.5	°C/W

Notes

8. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
9. Exposed heatsink pad plus the power and ground terminals comprise the main heat conduction paths. The actual $R_{\theta JB}$ (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace thickness. Maximum current at maximum die temperature represents ~16 W of conduction loss heating in the diagonal pair of output MOSFETs. Therefore, the $R_{\theta JC}$-total must be less than 5.0 °C/W for maximum load at 70°C ambient. Module thermal design must be planned accordingly.
10. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
11. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
12. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
13. Per JEDEC JESD51-6 with the board horizontal.
14. Indicates the average thermal resistance between the die and the exposed pad surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 5.0 V ≤ V+ ≤ 28 V and -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range (Note 15)	V+	5.0	–	40	V
Sleep State Supply Current (Note 16) I_{OUT} = 0 A, V_{EN} = 0 V	$I_{Q(sleep)}$	– –	25 –	50 –	µA
Standby Supply Current I_{OUT} = 0 A, V_{EN} = 5.0 V	$I_{Q(standby)}$	– –	– –	20 –	mA
Threshold Supply Voltage Switch-OFF Switch-ON Hysteresis	 $V+_{(thres-OFF)}$ $V+_{(thres-ON)}$ $V+_{(hys)}$	 4.15 4.5 150	 4.4 4.75 –	 4.65 5.0 –	 V V mV
CHARGE PUMP					
Charge Pump Voltage V+ = 5.0 V 8.0 V ≤ V+ ≤ 40 V	V_{CP} - V+	 3.35 –	 – –	 – 20	V
CONTROL INPUTS					
Input Voltage (IN1, IN2, D1, $\overline{D2}$) Threshold HIGH Threshold LOW Hysteresis	 V_{IH} V_{IL} V_{HYS}	 3.5 – 0.7	 – – 1.0	 – 1.4 –	V
Input Current (IN1, IN2, D1) V_{IN} - 0.0 V	I_{INP}	 -200	 -80	 –	µA
Input Current ($\overline{D2}$, EN) $V_{\overline{D2}}$ = 5.0 V	I_{INP}	 –	 25	 100	µA

Notes

15. Specifications are characterized over the range of 5.0 V ≤ V+ ≤ 28 V. Operation >28 V will cause some parameters to exceed listed min/max values. Refer to typical operating curves to extrapolate values for operation >28 V but ≤ 40 V.
16. $I_{Q(sleep)}$ is with sleep mode function enabled.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 5.0 V ≤ V+ ≤ 28 V and -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUTS (OUT1, OUT2)					
Output ON-Resistance (Note 17)	$R_{DS(ON)}$				mΩ
5.0 V ≤ V+ ≤ 28 V, T_J = 25°C		–	120	–	
8.0 V ≤ V+ ≤ 28 V, T_J = 150°C		–	–	225	
5.0 V ≤ V+ ≤ 8.0 V, T_J = 150°C		–	–	300	
Active Current Limiting Threshold (via Internal Constant OFF-Time PWM) on Low-Side MOSFETs (Note 18)	I_{LIM}	5.2	6.5	7.8	A
High-Side Short Circuit Detection Threshold	I_{SCH}	11	–	–	A
Low-Side Short Circuit Detection Threshold	I_{SCL}	8.0	–	–	A
Leakage Current (Note 19)	$I_{OUT(leak)}$				μA
V_{OUT} = V+		–	100	200	
V_{OUT} = Ground		–	30	60	
Output MOSFET Body Diode Forward Voltage Drop	V_F				V
I_{OUT} = 3.0 A		–	–	2.0	
Overtemperature Shutdown					°C
Thermal Limit	T_{LIM}	175	–	225	
Hysteresis	T_{HYS}	10	–	30	
HIGH-SIDE CURRENT SENSE FEEDBACK					
Feedback Current	I_{FB}				
I_{OUT} = 0 mA		–	–	600	μA
I_{OUT} = 500 mA		1.07	1.33	1.68	mA
I_{OUT} = 1.5 A		3.6	4.0	4.62	mA
I_{OUT} = 3.0 A		7.2	8.0	9.24	mA
I_{OUT} = 6.0 A		14.4	16	18.48	mA
FAULT STATUS (Note 20)					
Fault Status Leakage Current (Note 21)	$I_{\overline{FS}(leak)}$				μA
$V_{\overline{FS}}$ = 5.0 V		–	–	10	
Fault Status SET Voltage (Note 22)	$V_{\overline{FS}(LOW)}$				V
$I_{\overline{FS}}$ = 300 μA		–	–	1.0	

Notes

17. Output-ON resistance as measured from output to V+ and ground.
18. Active current limitation applies only for the low-side MOSFETs.
19. Outputs switched OFF with D1 or $\overline{D2}$.
20. Fault Status output is an open Drain output requiring a pullup resistor to 5.0 V.
21. Fault Status Leakage Current is measured with Fault Status HIGH and *not* SET.
22. Fault Status Set Voltage is measured with Fault Status LOW and SET with $I_{\overline{FS}}$ = 300 μA.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 5.0 V ≤ V+ ≤ 28 V and -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TIMING CHARACTERISTICS					
PWM Frequency (Note 23)	f_{PWM}	–	10	–	kHz
Maximum Switching Frequency During Active Current Limiting (Note 24)	f_{MAX}	–	–	20	kHz
Output ON Delay (Note 25) V+ = 14 V	$t_{d(ON)}$	– 	– 	18 	µs
Output OFF Delay (Note 25) V+ = 14 V	$t_{d(OFF)}$	– 	– 	18 	µs
I_{LIM} Output Constant-OFF Time for Low-Side MOSFETs (Note 26), (Note 27)	t_a	15	20.5	26	µs
I_{LIM} Blanking Time for Low-Side MOSFETs (Note 28), (Note 27)	t_b	12	16.5	21	µs
Output Rise and Fall Time (Note 29) V+ = 14 V, I_{OUT} = 3.0 A	t_f, t_r	 2.0	 5.0	 8.0	µs
Disable Delay Time (Note 30)	$t_{d(disable)}$	–	–	8.0	µs
Power-ON Delay Time (Note 31)	t_{pod}	–	1.0	5.0	ms
Wake-Up Delay Time (Note 31)	t_{wud}	–	1.0	5.0	ms
Output MOSFET Body Diode Reverse Recovery Time (Note 32)	t_{rr}	100	–	–	ns

Notes

23. The outputs can be PWM-controlled from an external source. This is typically done by holding one input high while applying a PWM pulse train to the other input. The maximum PWM frequency obtainable is a compromise between switching losses and switching frequency. See Typical Switching Waveforms, Figures 11 through 18, pp. 15–16.
24. The Maximum Switching Frequency during active current limiting is internally implemented. The internal current limit circuitry produces a constant-OFF-time pulse-width modulation of the output current. The output load's inductance, capacitance, and resistance characteristics affect the total switching period (OFF-time + ON-time) and thus the PWM frequency during current limit.
25. Output Delay is the time duration from the midpoint of the IN1 or IN2 input signal to the 10% or 90% point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning HIGH-to-LOW, the delay is from the midpoint of the input signal to the 90% point of the output response signal. If the output is transitioning LOW-to-HIGH, the delay is from the midpoint of the input signal to the 10% point of the output response signal. See Figure 2, page 11.
26. I_{LIM} Output Constant-OFF Time is the time during which the internal constant-OFF time PWM current regulation circuit has tri-stated the output bridge.
27. Load currents ramping up to the current regulation threshold become limited at the I_{LIM} value. The short circuit currents possess a di/dt that ramps up to the I_{SCH} or I_{SCL} threshold during the I_{LIM} blanking time, registering as a short circuit event detection and causing the shutdown circuitry to force the output into an immediate tri-state latch-OFF. See Figures 6 and 7, page 12. Operation in Current Limit mode may cause junction temperatures to rise. Junction temperatures above ~160°C will cause the output current limit threshold to progressively "fold back", or decrease with temperature, until ~175°C is reached, after which the T_{LIM} thermal latch-OFF will occur. Permissible operation within this foldback region is limited to nonrepetitive transient events of duration not to exceed 30 seconds. See Figure 5, page 11.
28. I_{LIM} Blanking Time is the time during which the current regulation threshold is ignored so that the short-circuit detection threshold comparators my have time to act.
29. Rise Time is from the 10% to the 90% level and Fall Time is from the 90% to the 10% level of the output signal. See Figure 4, page 11.
30. Disable Delay Time is the time duration from the midpoint of the D (disable) input signal to 10% of the output tri-state response. See Figure 3, page 11.
31. Parameter has been characterized but not production tested.
32. Parameter is guaranteed by design but not production tested.

Timing Diagrams

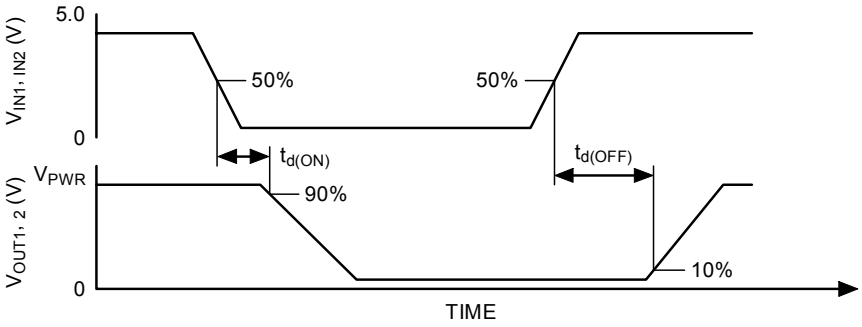


Figure 2. Output Delay Time

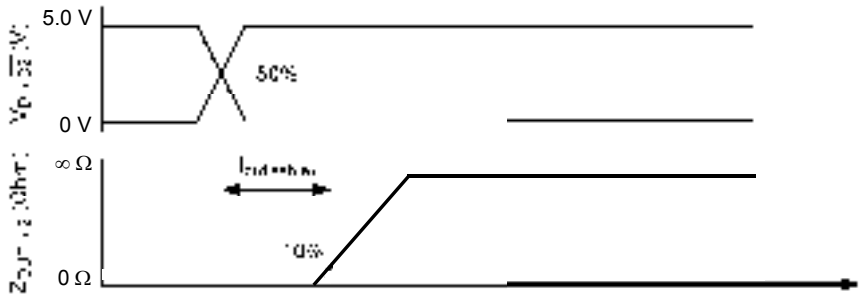


Figure 3. Disable Delay Time

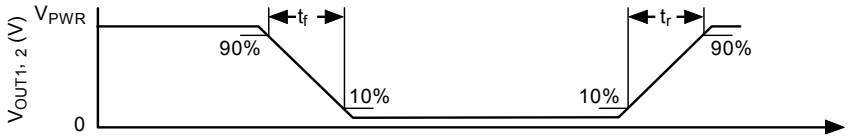


Figure 4. Output Switching Time

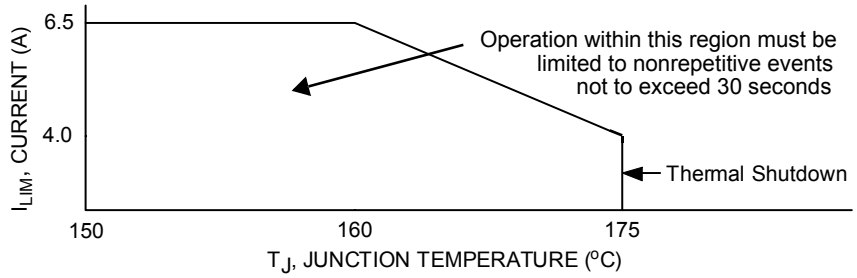


Figure 5. Active Current Limiting Versus Temperature (Typical)

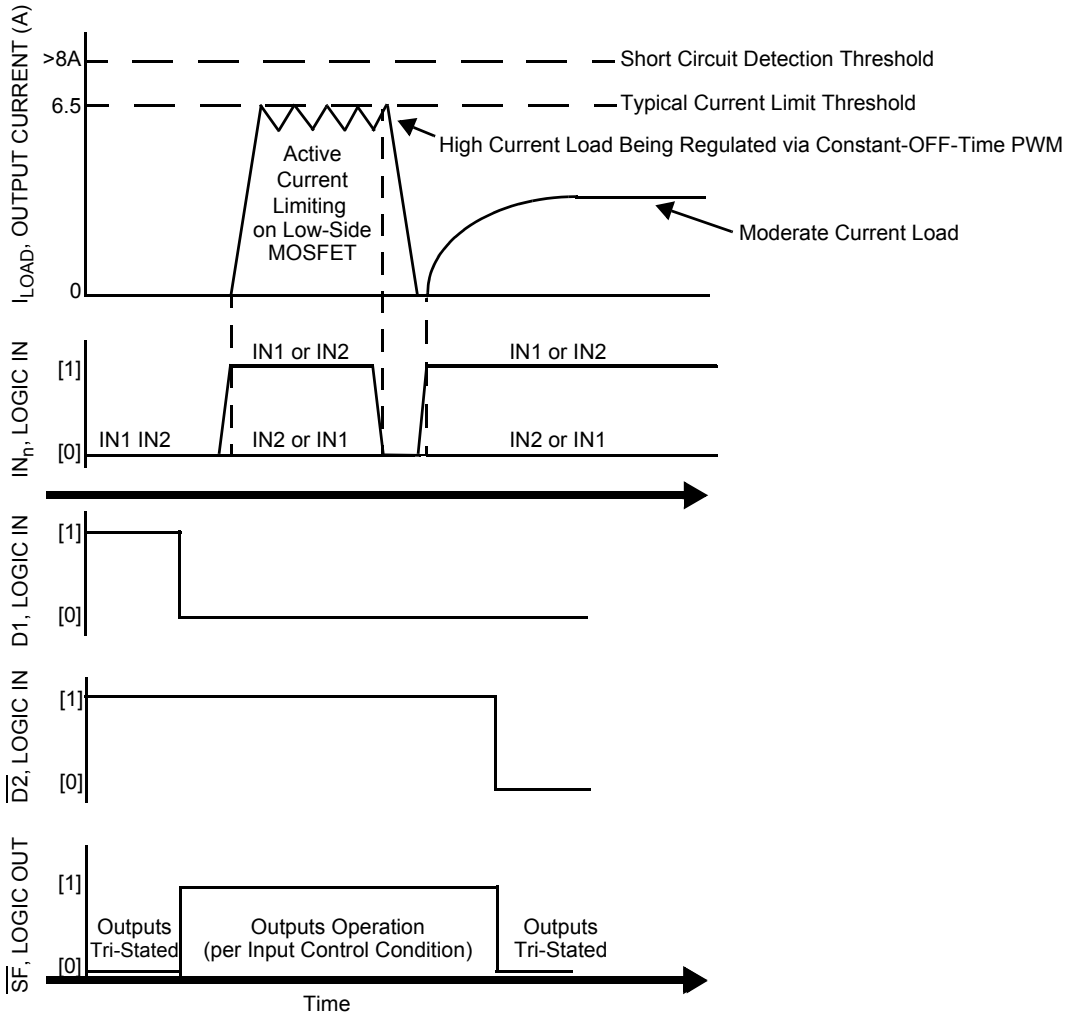


Figure 6. Operating States

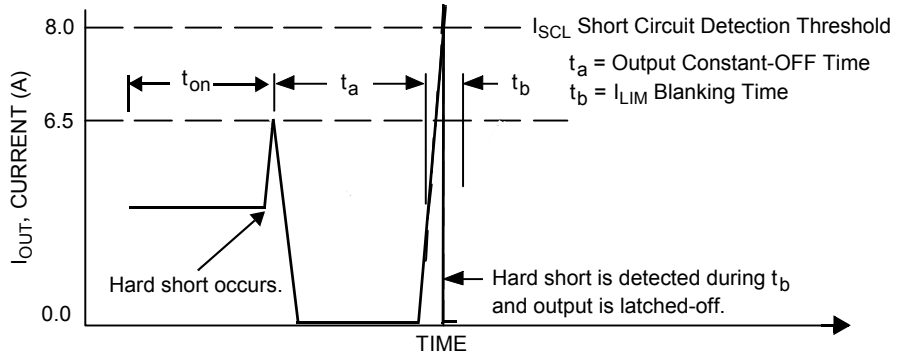


Figure 7. Example Short Circuit Detection Detail on Low-Side MOSFET

Electrical Performance Curves

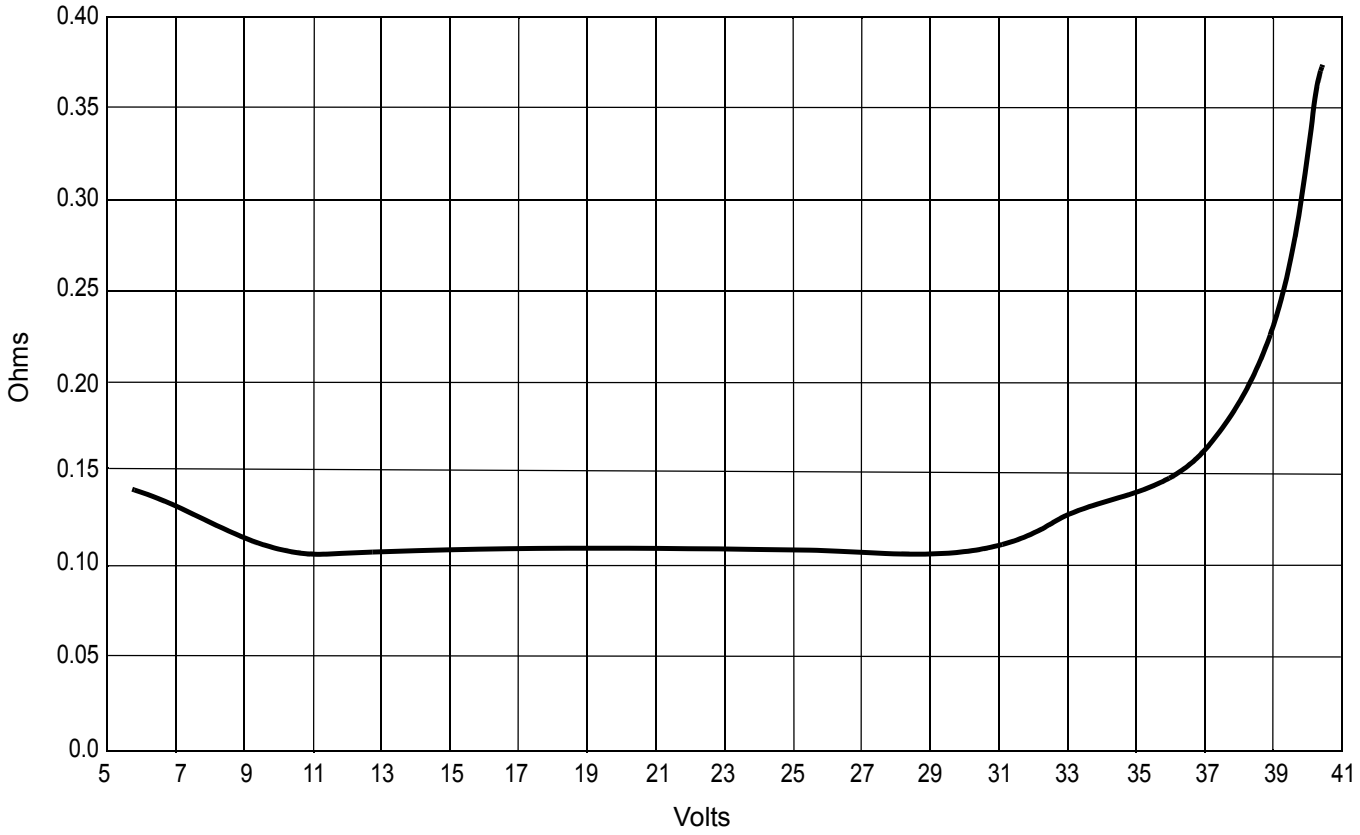


Figure 8. Typical High-Side $R_{DS(ON)}$ Versus V+

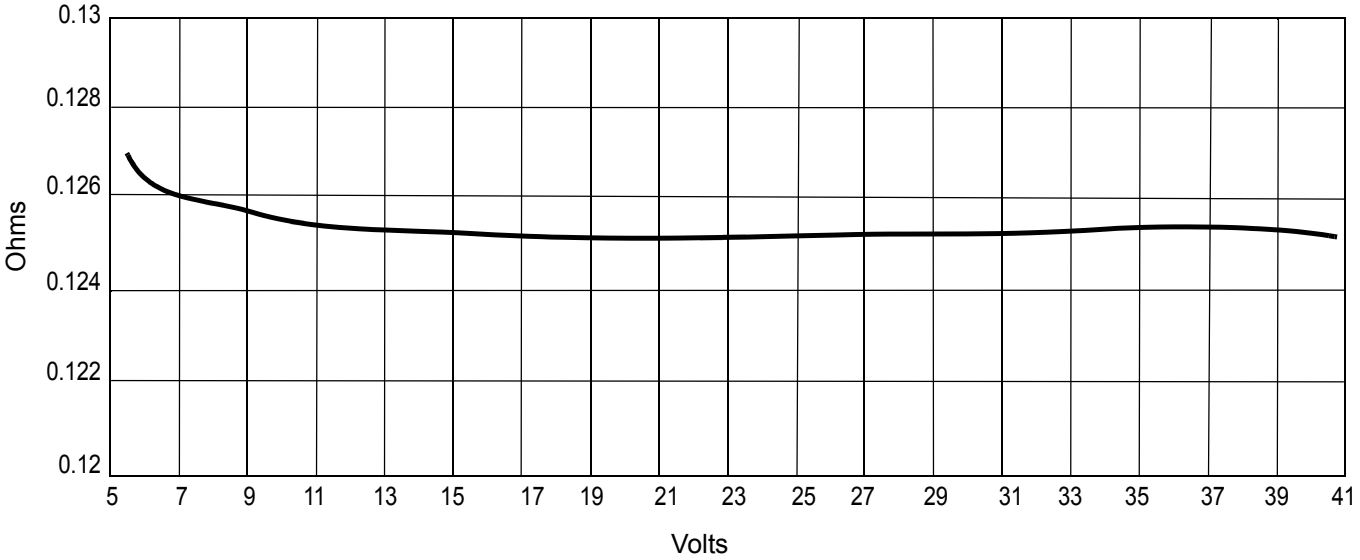


Figure 9. Typical Low-Side $R_{DS(ON)}$ Versus V+

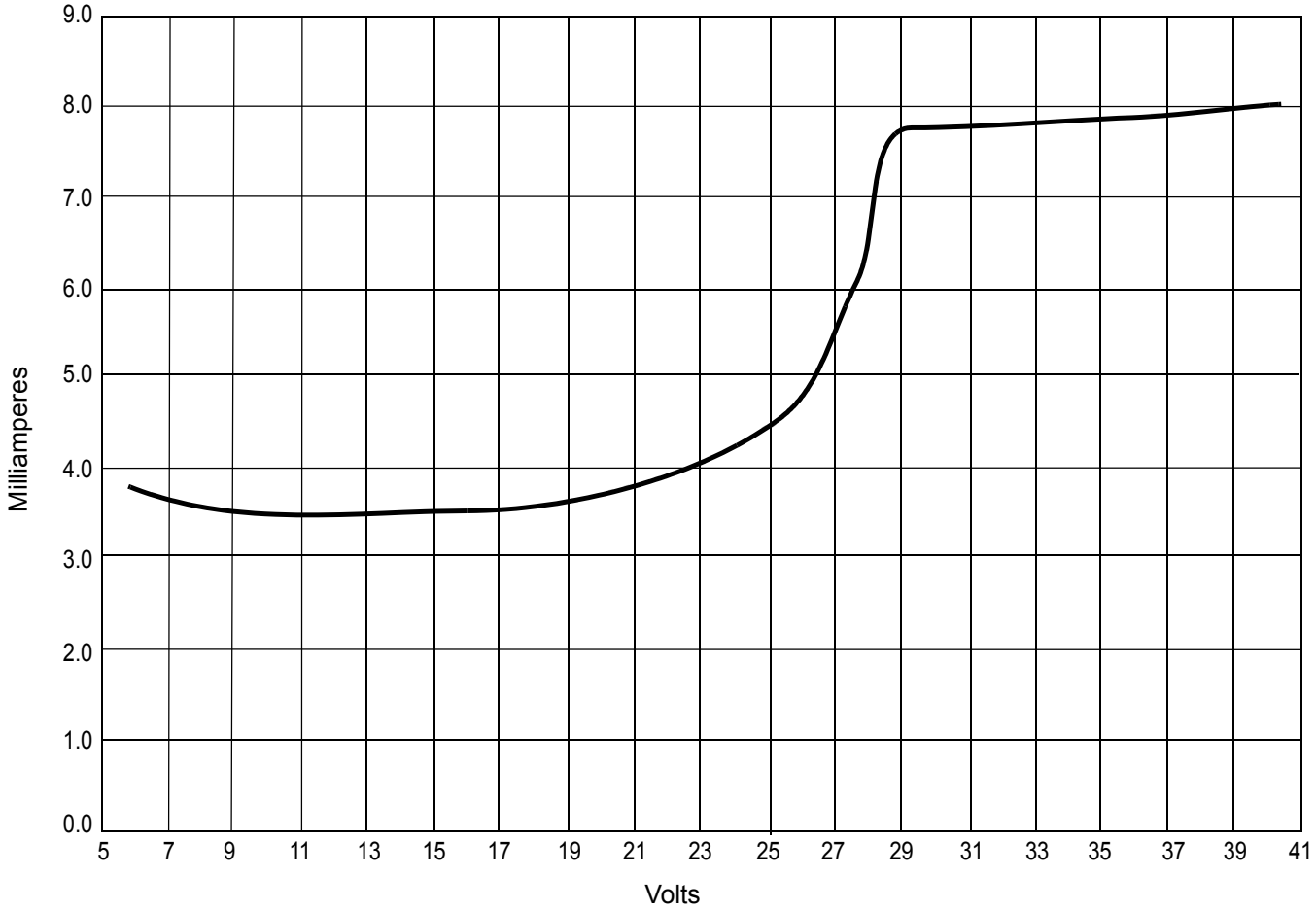


Figure 10. Typical Quiescent Supply Current Versus V+

Typical Switching Waveforms

Important For all plots, the following applies:

- Ch2=2.0 A per division
- L_{LOAD}=533 μH @ 1.0 kHz
- L_{LOAD}=530 μH @ 10.0 kHz
- R_{LOAD}=4.0 Ω

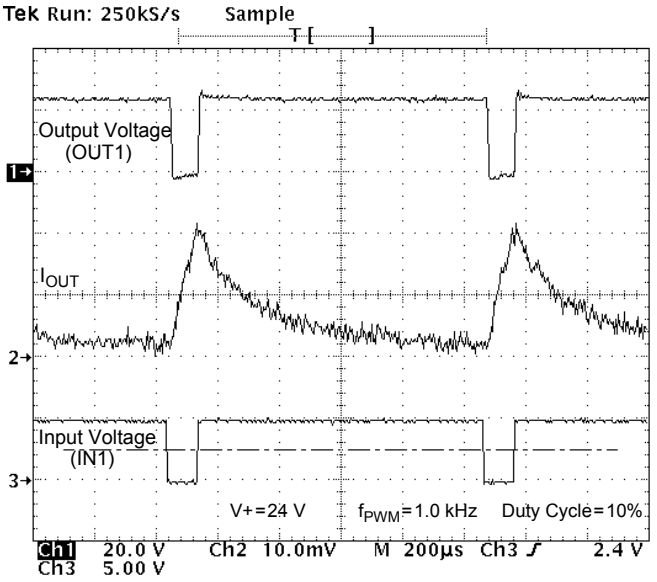


Figure 11. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 10%

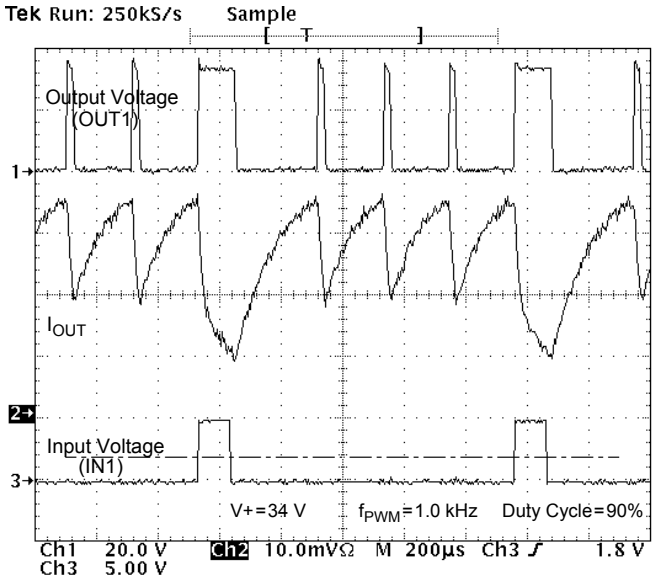


Figure 13. Output Voltage and Current vs. Input Voltage at V+ = 34 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 90%, Showing Device in Current Limiting Mode

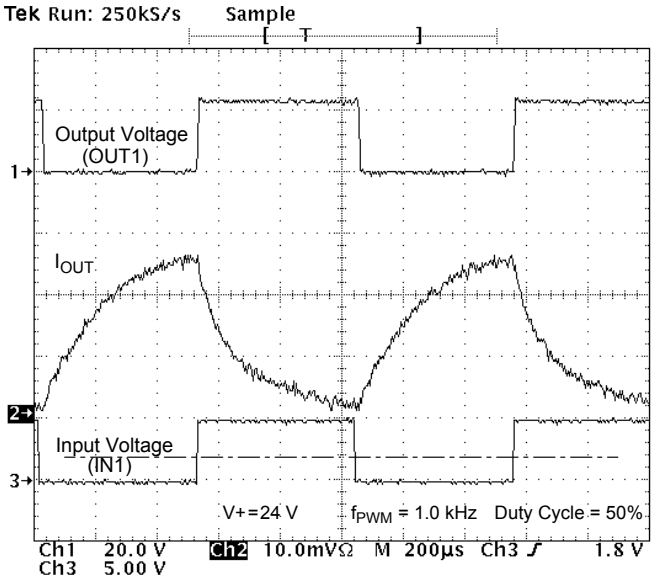


Figure 12. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 50%

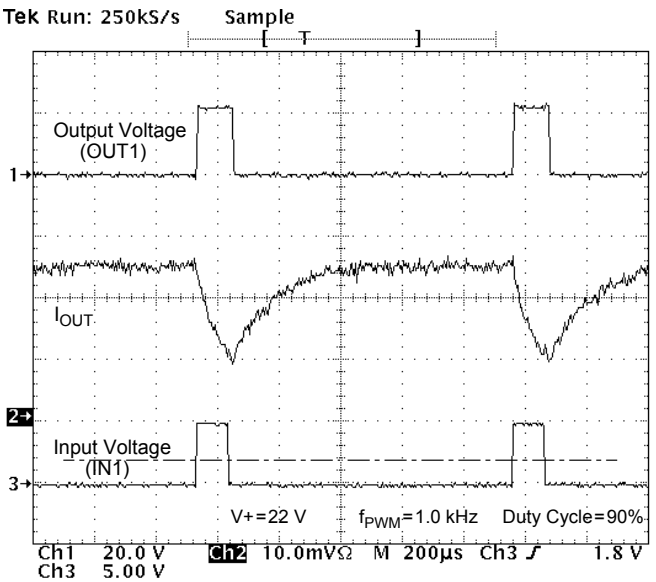


Figure 14. Output Voltage and Current vs. Input Voltage at V+ = 22 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 90%

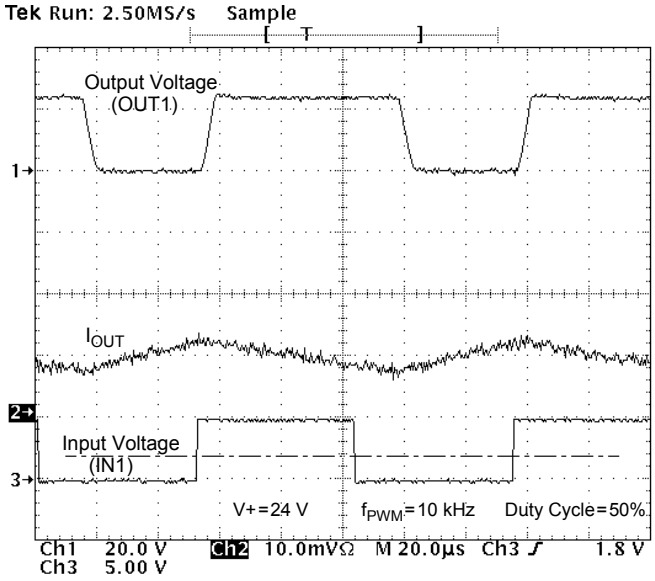


Figure 15. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 10 kHz, and Duty Cycle of 50%

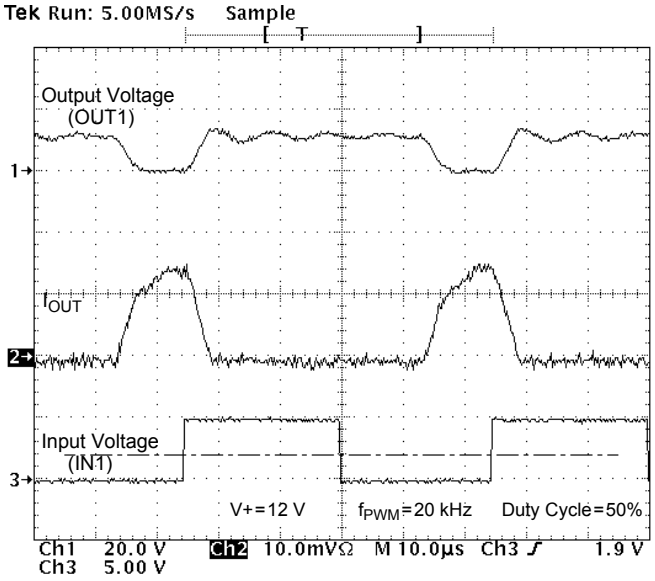


Figure 17. Output Voltage and Current vs. Input Voltage at V+ = 12 V, PMW Frequency of 20 kHz, and Duty Cycle of 50% for a Purely Resistive Load

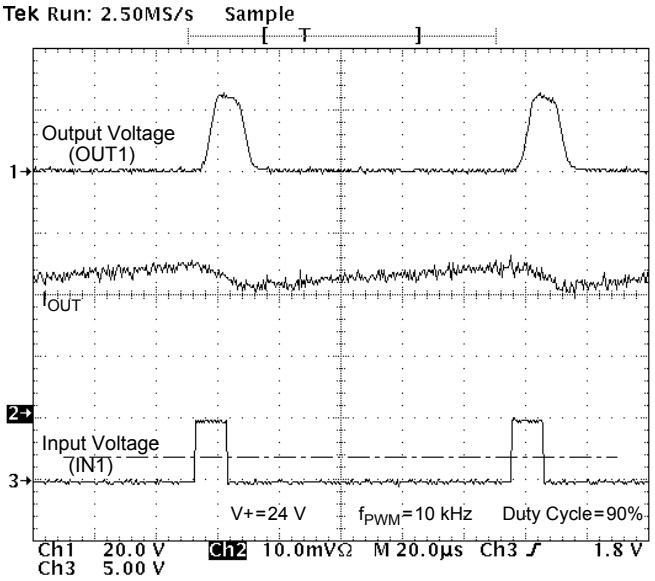


Figure 16. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 10 kHz, and Duty Cycle of 90%

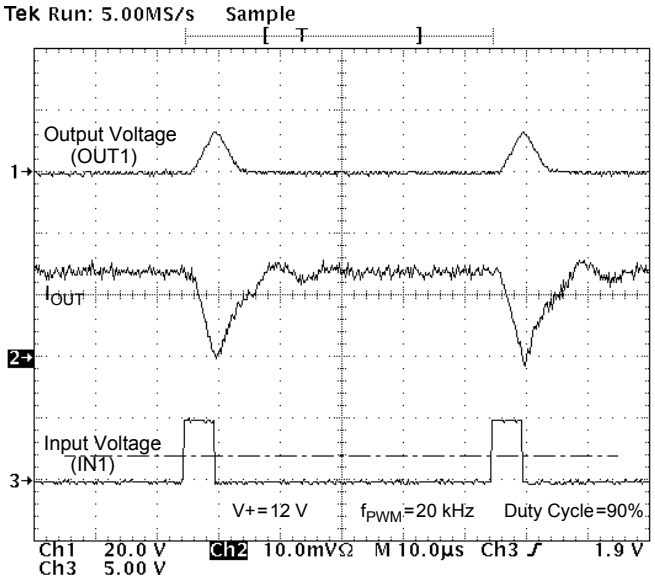


Figure 18. Output Voltage and Current vs. Input Voltage at V+ = 12 V, PMW Frequency of 20 kHz, and Duty Cycle of 90% for a Purely Resistive Load

Table 1. Truth Table

The tri-state conditions and the fault status are reset using D1 or $\overline{D2}$. The truth table uses the following notations: L = LOW, H = HIGH, X = HIGH or LOW, and Z = High impedance (all output power transistors are switched off).

Device State	Input Conditions					Fault Status Flag	Output States	
	EN	D1	$\overline{D2}$	IN1	IN2	$\overline{FS}$	OUT1	OUT2
Forward	H	L	H	H	L	H	H	L
Reverse	H	L	H	L	H	H	L	H
Freewheeling Low	H	L	H	L	L	H	L	L
Freewheeling High	H	L	H	H	H	H	H	H
Disable 1 (D1)	H	H	X	X	X	L	Z	Z
Disable 2 ($\overline{D2}$)	H	X	L	X	X	L	Z	Z
IN1 Disconnected	H	L	H	Z	X	H	H	X
IN2 Disconnected	H	L	H	X	Z	H	X	H
D1 Disconnected	H	Z	X	X	X	L	Z	Z
$\overline{D2}$ Disconnected	H	X	Z	X	X	L	Z	Z
Undervoltage (Note 33)	H	X	X	X	X	L	Z	Z
Overtemperature (Note 34)	H	X	X	X	X	L	Z	Z
Short Circuit (Note 34)	H	X	X	X	X	L	Z	Z
Sleep Mode EN	L	X	X	X	X	H	Z	Z
EN Disconnected	Z	X	X	X	X	H	Z	Z

Notes

33. In the case of an undervoltage condition, the outputs tri-state and the fault status is SET logic LOW. Upon undervoltage recovery, fault status is reset automatically or automatically cleared and the outputs are restored to their original operating condition.
34. When a short circuit or overtemperature condition is detected, the power outputs are tri-state latched-OFF independent of the input signals and the fault status flag is SET logic LOW.

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

Numerous protection and operational features (speed, torque, direction, dynamic braking, PWM control, and closed-loop control), in addition to the 5.0 A current capability, make the 33887 a very attractive, cost-effective solution for controlling a broad range of small DC motors. In addition, a pair of 33887 devices can be used to control bipolar stepper motors. The 33887 can also be used to excite transformer primary windings with a switched square wave to produce secondary winding AC currents.

As shown in Figure 1, Simplified Internal Block Diagram, page 2, the 33887 is a fully protected monolithic H-Bridge with Enable, Fault Status reporting, and High-Side current sense feedback to accommodate closed-loop PWM control. For a DC motor to run, the input conditions need be as follows: Enable input logic HIGH, D1 input logic LOW, $\overline{D2}$ input logic HIGH, $\overline{FS}$ flag cleared (logic HIGH), one IN logic LOW and the other IN logic HIGH (to define output polarity). The 33887 can execute dynamic braking by simultaneously turning on either both high-side MOSFETs or both low-side MOSFETs in the output H-Bridge; e.g., IN1 and IN2 logic HIGH or IN1 and IN2 logic LOW.

The 33887 outputs are capable of providing a continuous DC load current of 5.0 A from a 40 V V+ source. An internal charge pump supports PWM frequencies to 10 kHz. An external pullup resistor is required at the $\overline{FS}$ terminal for fault status reporting. The 33887 has an analog feedback (current mirror) output terminal (the FB terminal) that provides a constant-current source ratioed to the active high-side MOSFET. This can be used to provide “real time” monitoring of load current to facilitate closed-loop operation for motor speed/torque control.

Two independent inputs (IN1 and IN2) provide control of the two totem-pole half-bridge outputs. Two disable inputs (D1 and $\overline{D2}$) provide the means to force the H-Bridge outputs to a high-impedance state (all H-Bridge switches OFF). An EN terminal controls an enable function that allows the 33887 to be placed in a power-conserving sleep mode.

The 33887 has undervoltage shutdown with automatic recovery, active current limiting, output short-circuit latch-OFF, and overtemperature latch-OFF. An undervoltage shutdown, output short-circuit latch-OFF, or overtemperature latch-OFF fault condition will cause the outputs to turn OFF (i.e., become high impedance or tri-stated) and the fault output flag to be set LOW. Either of the Disable inputs or V+ must be “toggled” to clear the fault flag.

Active current limiting is accomplished by a constant OFF-time PWM method employing active current limiting threshold triggering. The active current limiting scheme is unique in that it incorporates a junction temperature-dependent current limit threshold. This means the active current limiting threshold is “ramped down” as the junction temperature increases above 160°C, until at 175°C the current will have been decreased to about 4.0 A. Above 175°C, the overtemperature shutdown (latch-OFF) occurs. This combination of features allows the device to remain in operation for 30 seconds at junction temperatures above 150°C for nonrepetitive unexpected loads.

FUNCTIONAL TERMINAL DESCRIPTION

PGND and AGND

Power and analog ground terminals should be connected together with a very low impedance connection.

V+

V+ terminals are the power supply inputs to the device. All V+ terminals must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between terminals.

V+ terminals have an undervoltage threshold. If the supply voltage drops below a V+ undervoltage threshold, the output power stage switches to a tri-state condition and the fault status flag is SET and the Fault Status terminal voltage switched to a logic LOW. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals and the fault status flag is automatically reset logic HIGH.

Fault Status ($\overline{FS}$)

The $\overline{FS}$ terminal is the device fault status output. This output is an active LOW open drain structure requiring a pullup resistor to 5.0 V. Refer to Table 1, Truth Table, page 17.

IN1, IN2, D1, and $\overline{D2}$

These terminals are input control terminals used to control the outputs. These terminals are 5.0 V CMOS-compatible inputs with hysteresis. The IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 and $\overline{D2}$ are complementary inputs used to tri-state disable the H-Bridge outputs.

When either D1 or $\overline{D2}$ is SET (D1 = logic HIGH or $\overline{D2}$ = logic LOW) in the disable state, outputs OUT1 and OUT2 are both tri-state disabled; however, the rest of the device circuitry is fully operational and the supply $I_{Q(standby)}$ current is reduced to a few milliamperes. Refer to Table 1, Truth Table, and STATIC ELECTRICAL CHARACTERISTICS table, page 8.

OUT1 and OUT2

These terminals are the outputs of the H-Bridge with integrated output MOSFET body diodes. The bridge output is controlled using the IN1, IN2, D1, and $\overline{D2}$ inputs. The low-side MOSFETs have active current limiting above the I_{LIM} threshold. The outputs also have thermal shutdown (tri-state latch-OFF) with hysteresis as well as short circuit latch-OFF protection.

A disable timer (time t_b) incorporated to detect currents that are higher than current limit is activated at each output activation to facilitate hard short detection (see Figure 7, page 12).

C_{CP}

A filter capacitor (up to 33 nF) can be connected from the charge pump output terminal and PGND. The device can operate without the external capacitor, although the C_{CP} capacitor helps to reduce noise and allows the device to perform at maximum speed, timing, and PWM frequency.

EN

The EN terminal is used to place the device in a sleep mode so as to consume very low currents. When the EN terminal voltage is a logic LOW state, the device is in the sleep mode. The device is enabled and fully operational when the EN terminal voltage is logic HIGH. An internal pulldown resistor maintains the device in sleep mode in the event EN is driven through a high impedance I/O or an unpowered microcontroller, or the EN input becomes disconnected.

FB

The 33887 has a feedback output (FB) for “real time” monitoring of H-Bridge high-side current to facilitate closed-loop operation for motor speed and torque control.

The FB terminal provides current sensing feedback of the H-Bridge high-side drivers. When running in the forward or reverse direction, a ground referenced 1/375th (0.00266) of load current is output to this terminal. Through the use of an external resistor to ground, the proportional feedback current can be converted to a proportional voltage equivalent and the controlling microcontroller can “read” the current proportional voltage with its analog-to-digital converter (ADC). This is intended to provide the user with motor current feedback for motor torque control. The resistance range for the linear operation of the FB terminal is 100 $< R_{FB} <$ 200 Ω.

If PWM-ing is implemented using the disable terminal inputs (either D1 or $\overline{D2}$), a small filter capacitor (1.0 μF or less) may be required in parallel with the external resistor to ground for fast spike suppression.

PERFORMANCE FEATURES

Short Circuit Protection

If an output short circuit condition is detected, the power outputs tri-state (latch-OFF) independent of the input (IN1 and IN2) states, and the fault status output flag is SET logic LOW. If the D1 input changes from logic HIGH to logic LOW, or if the $\overline{D2}$ input changes from logic LOW to logic HIGH, the output bridge will become operational again and the fault status flag will be reset (cleared) to a logic HIGH state.

The output stage will always switch into the mode defined by the input terminals (IN1, IN2, D1, and $\overline{D2}$), provided the device junction temperature is within the specified operating temperature range.

Active Current Limiting

The maximum current flow under normal operating conditions is internally limited to I_{LIM} (5.2 A to 7.8 A). When the maximum current value is reached, the output stages are tri-stated for a fixed time (t_a) of 20 μs typical. Depending on the time constant associated with the load characteristics, the current decreases during the tri-state duration until the next output ON cycle occurs (see Figures 7 and 13, page 12 and page 15, respectively).

The current limiting threshold value is dependent upon the device junction temperature. When $-40°C \le T_J \le 160°C$, I_{LIM} is between 5.2 A to 7.8 A. When T_J exceeds 160°C, the I_{LIM} current decreases linearly down to 4.0 A typical at 175°C. Above 175°C the device overtemperature circuit detects T_{LIM} and overtemperature shutdown occurs (see Figure 5, page 11). This feature allows the device to remain operational for a longer time but at a regressing output performance level at junction temperatures above 160°C.

Overtemperature Shutdown and Hysteresis

If an overtemperature condition occurs, the power outputs are tri-stated (latched-OFF) and the fault status flag is SET to logic LOW.

To reset from this condition, D1 must change from logic HIGH to logic LOW, or $\overline{D2}$ must change from logic LOW to logic HIGH. When reset, the output stage switches ON again, provided that the junction temperature is now below the overtemperature threshold limit minus the hysteresis.

Note Resetting from the fault condition will clear the fault status flag.

PACKAGE INFORMATION

The 33887 packages are designed for thermal performance. The significant feature of these packages is the exposed pad on which the power die is soldered. When soldered to a PCB, this pad provides a path for heat flow to the ambient environment. The more copper area and thickness on the PCB, the better the power dissipation and transient behavior will be.

Example Characterization on a double-sided PCB: bottom side area of copper is 7.8 cm^2; top surface is 2.7 cm^2 (see Figure 19); grid array of 24 vias 0.3 mm in diameter.

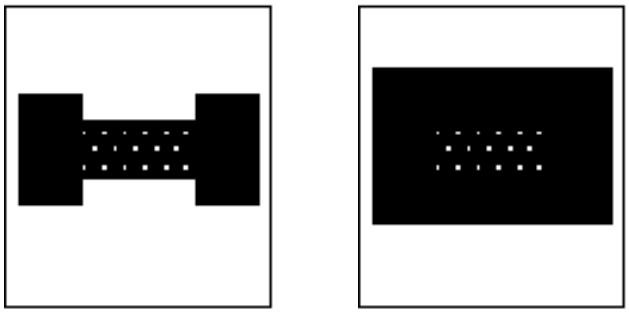


Figure 19. PCB Test Layout

Figure 20 shows the thermal response with the device in the HSOP package soldered on to the test PCB described in Figure 19.

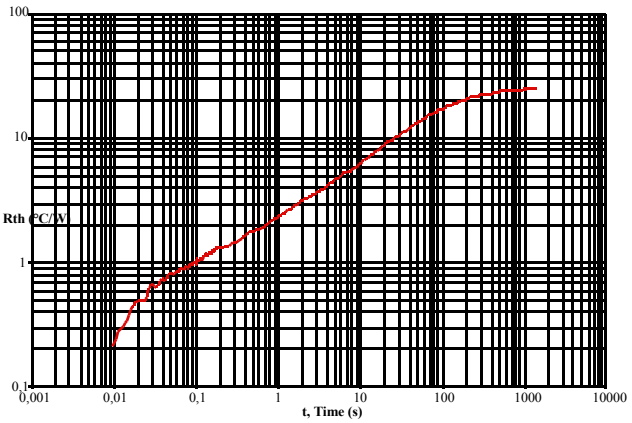


Figure 20. 33887 Thermal Response, HSOP Package

APPLICATIONS

Figure 21 shows a typical application schematic. For precision high-current applications in harsh, noisy environments, the V+ by-pass capacitor may need to be substantially larger.

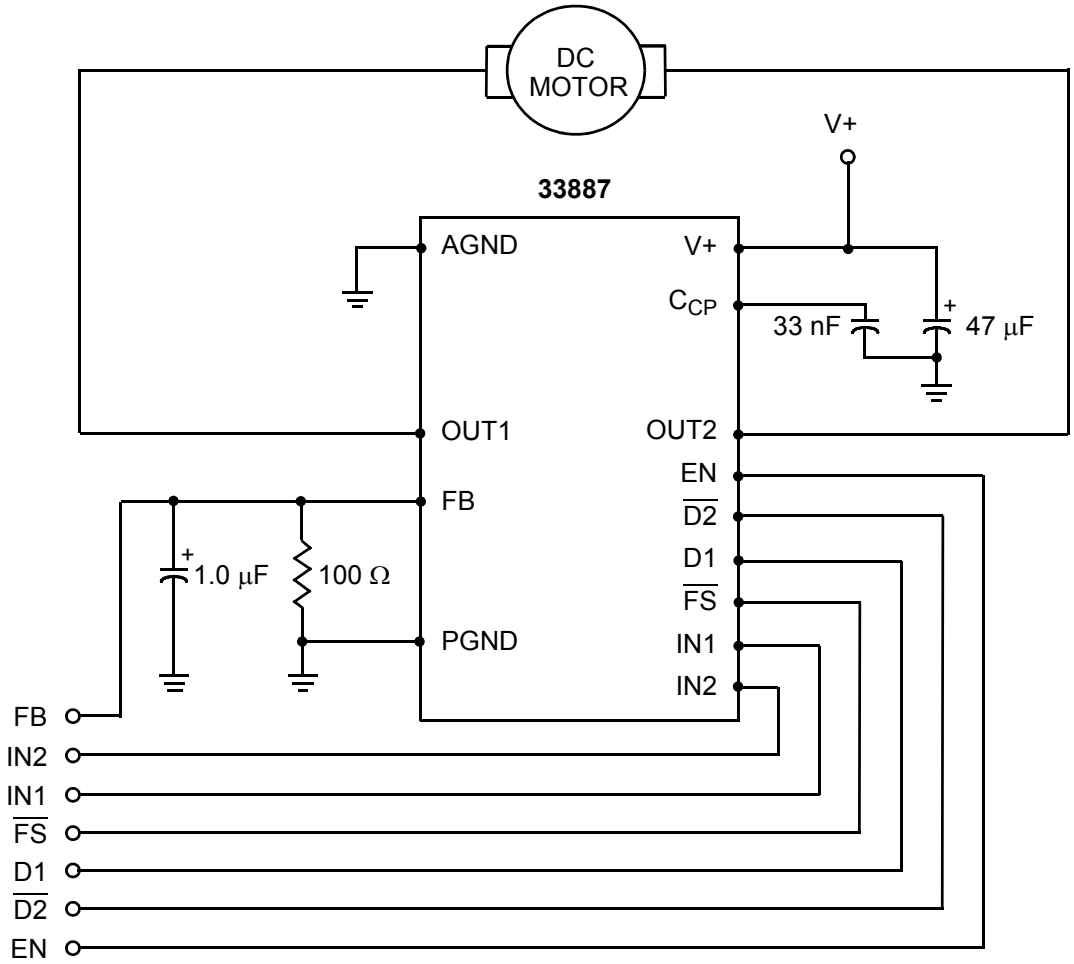
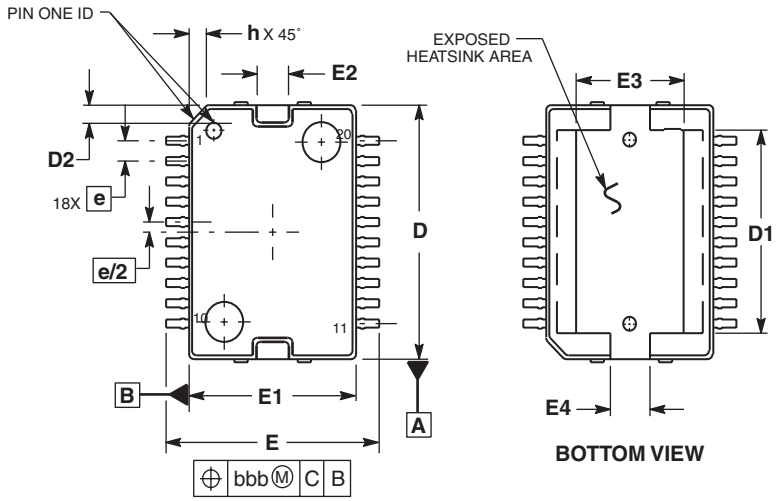
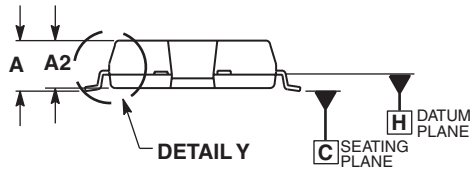


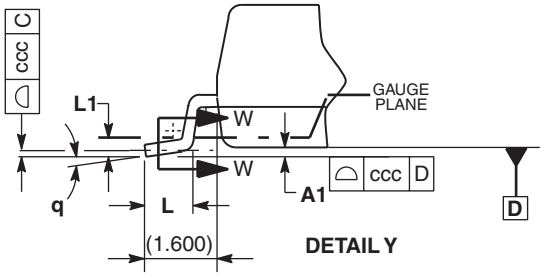
Figure 21. 33887 Typical Application Schematic

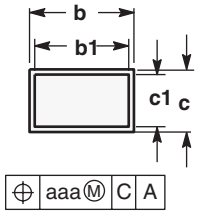
PACKAGE DIMENSIONS

DH SUFFIX
VW (Pb-FREE) SUFFIX
20-TERMINAL HSOP
PLASTIC PACKAGE
CASE 979-04
ISSUE C





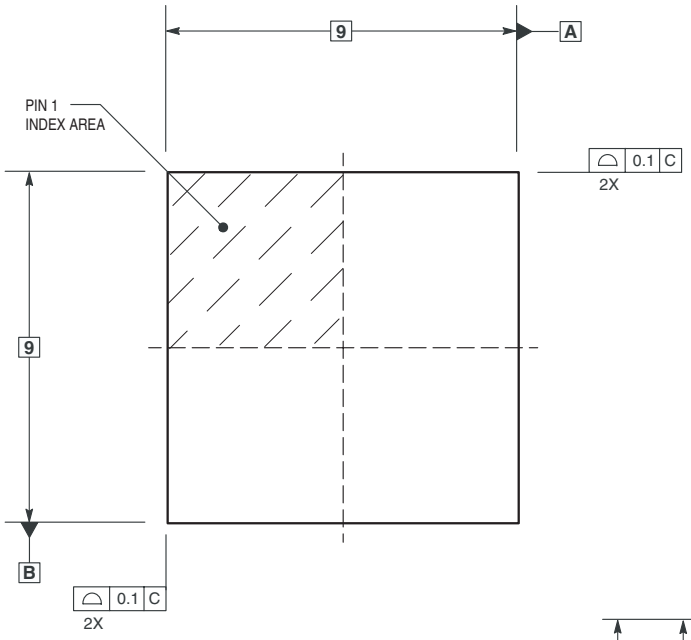


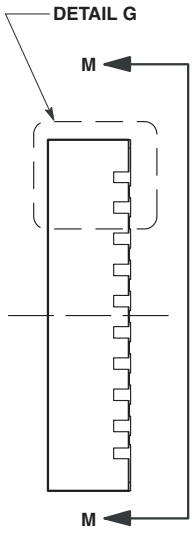


NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.178 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.

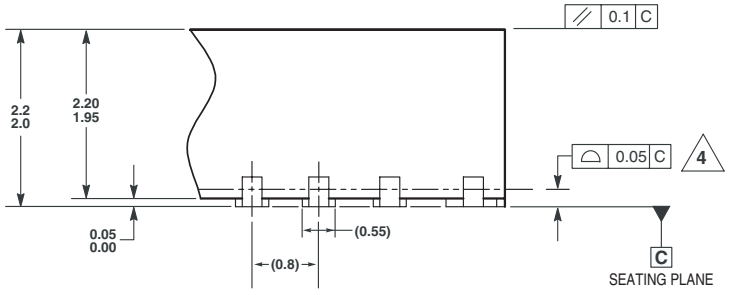
	MILLIMETERS	
DIM	MIN	MAX
A	3.100	3.350
A1	0.050 BSC	
A2	3.100	3.250
D	15.800	16.000
D1	12.270	12.470
D2	0.900	1.100
E	13.950	14.450
E1	10.900	11.100
E2	2.500	2.700
E3	7.000	7.200
E4	2.700	2.900
L	0.840	1.100
L1	0.350 BSC	
b	0.400	0.520
b1	0.400	0.482
c	0.230	0.310
c1	0.230	0.280
e	1.270 BSC	
h	---	1.100
q	0	8
aaa	0.200	
bbb	0.200	
ccc	0.100	

PNB (Pb-FREE) SUFFIX
36-TERMINAL PQFN
NON-LEADED PACKAGE
CASE 1503-01
ISSUE O

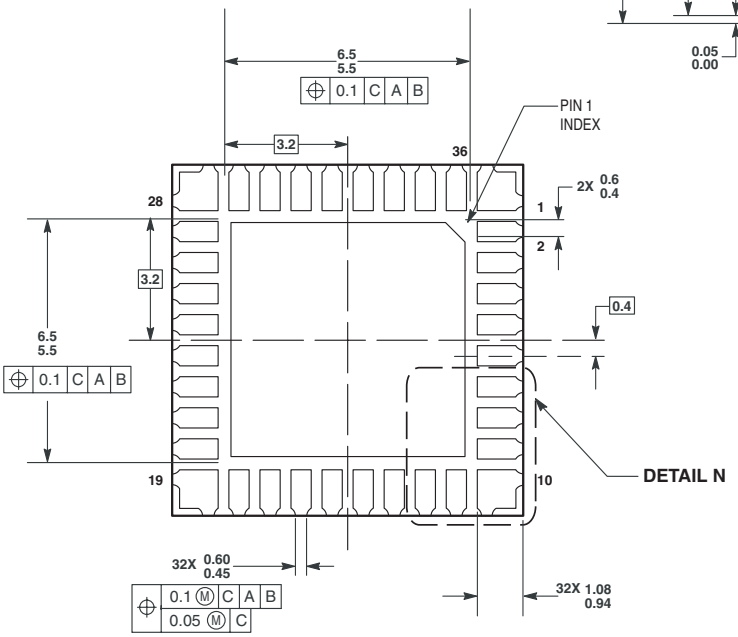




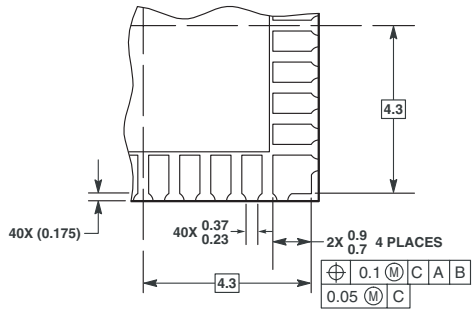
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: F-PQFP-N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.



DETAIL G
VIEW ROTATED 90° CW

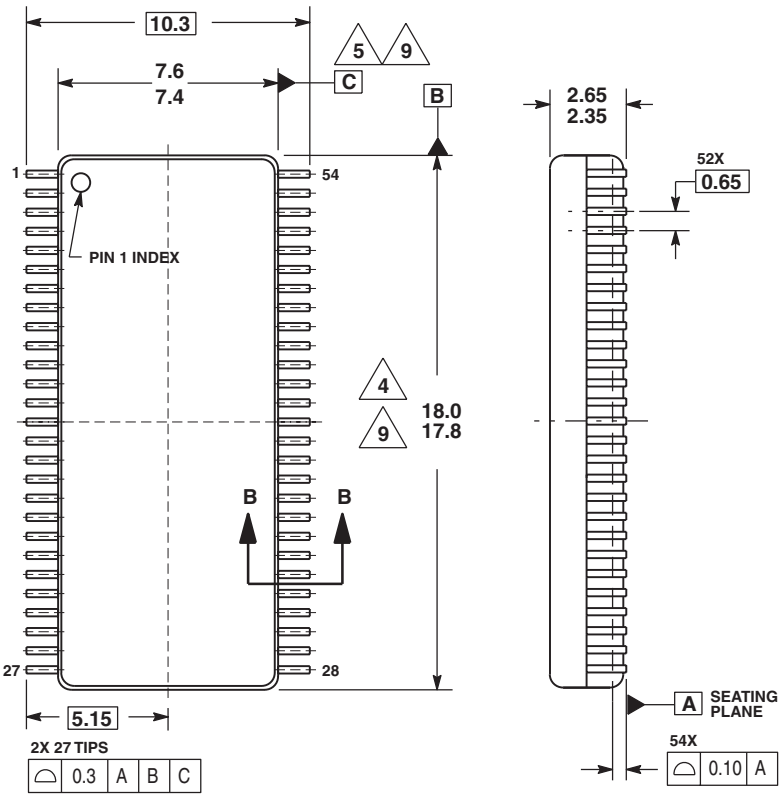


VIEW M–M

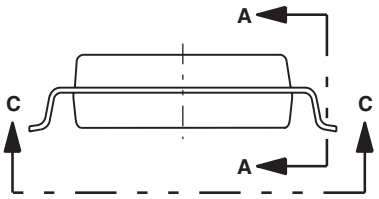


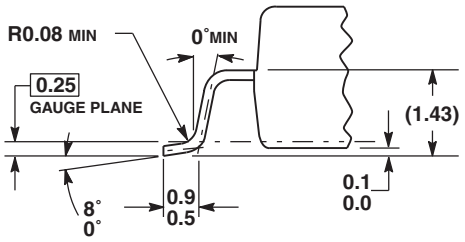
DETAIL N
CORNER CONFIGURATION

DWB SUFFIX
54-TERMINAL SOICW EXPOSED PAD
PLASTIC PACKAGE
CASE 1390-01
ISSUE B

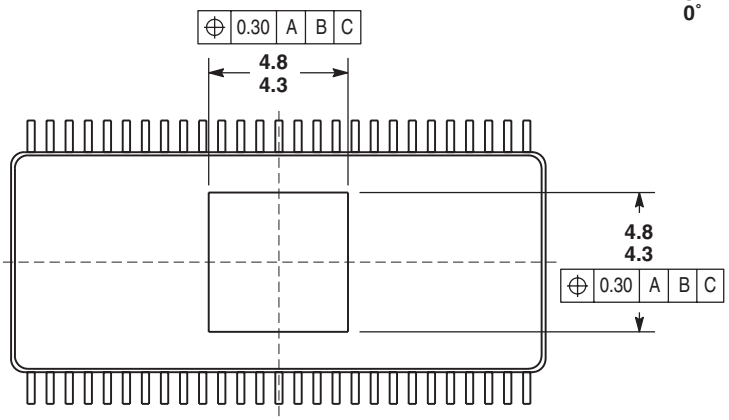


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

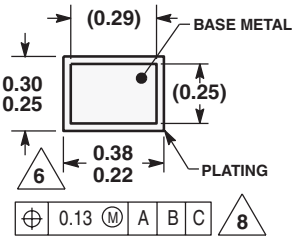




SECTION B-B



VIEW C-C



SECTION A-A
ROTATED 90° CLOCKWISE

NOTES

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NOTES

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