OKI Semiconductor

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MSM548333

240,384-Word × 8-bit + 240,384-Word × 4-bit Triple Port type Field Memory

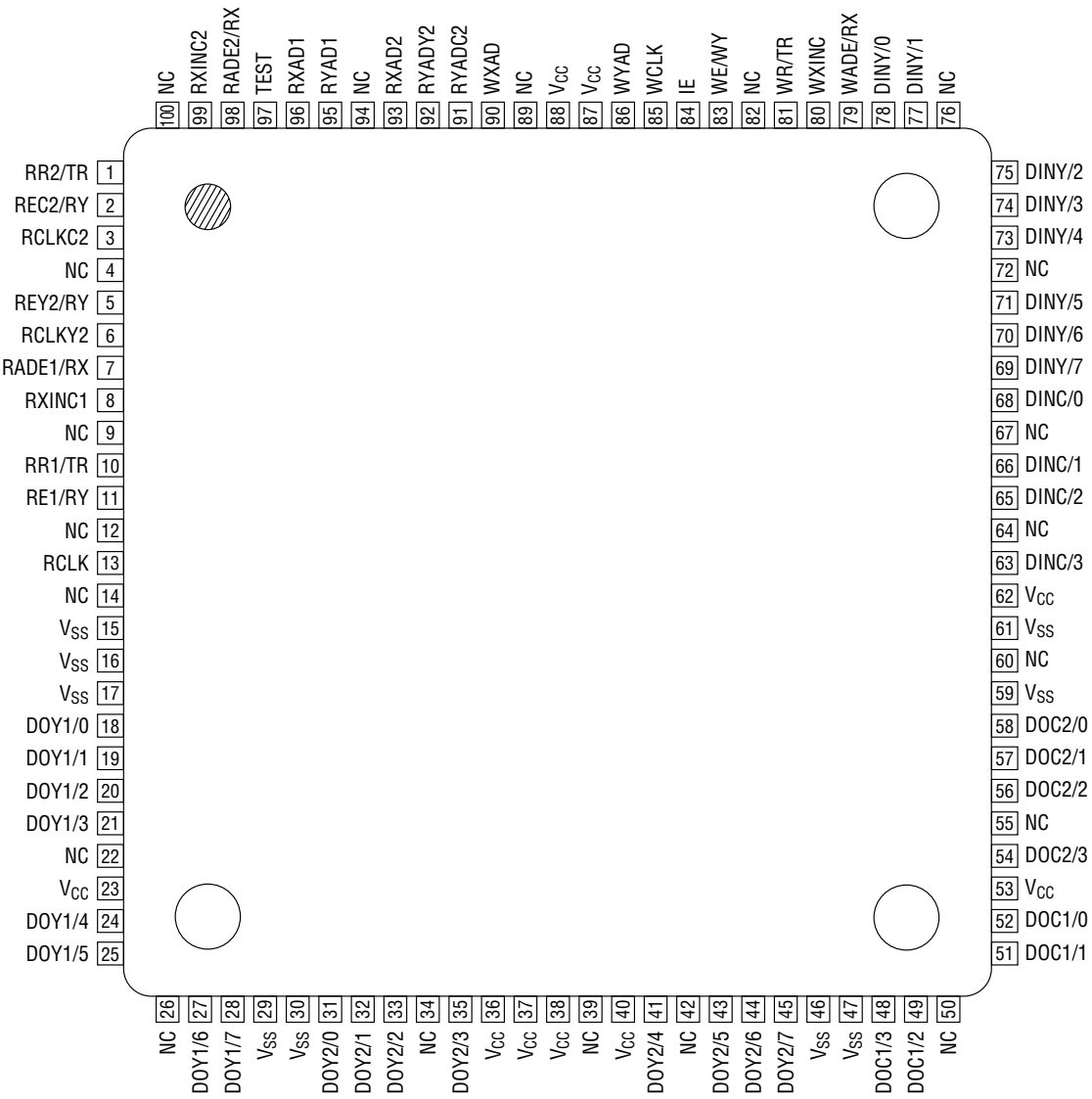
DESCRIPTION

The MSM548333 is a high performance double triple-port type 2.88-Mbit, 768 bits × 313 lines × (8 + 4), Field Memory for Y-C separation signal control. The MSM548333 has two memory plain blocks: Y area has 8 plains and C area has 4 plains. Each plain contains 768 × 313 bits. Each plain has one input port and two output ports. Access is done line by line. The line address must be set each time a line is changed.
The MSM548333 is especially designed for high performance digital cameras, TVs, VTRs and Multi-media applications which require special operations such as time-base correction, noise reduction and other digital techniques.
The MSM548333 is not designed for high end use in such applications as medical systems, professional graphics systems which require long term picture storage, data storage systems and others.
More than two MSM548333s can be cascaded directly without any delay devices between them. Cascading MSM548333s provides larger capacity and longer delay.
X and Y serial address input enables random initial address setting of serial access in a page. Other than the random address setting, MSM548333 has several types of address set modes such as line hold, address jump to initial address and line increment. For example, address jump to initial X address and line increment enable block access.
Self refresh function releases the MSM548333 from being applied external refresh control clocks even though it contains dynamic type memory cells. Input enable control or IE pin enables write mask function.

FEATURES

- Configuration
  6-port configuration
  Y area: 768 × 313 × 8-bit configuration × 1 (serial write port)
  768 × 313 × 8-bit configuration × 2 (serial read port)
  C area: 768 × 313 × 4-bit configuration × 1 (serial write port)
  768 × 313 × 4-bit configuration × 2 (serial read port)
- Line by line access.
- X and Y serial address inputs for random serial initial bit address
- Asynchronous operation
- Serial read and write cycle times
  Read cycle: 30 ns min.
  Write cycle: 50 ns min.
- Low operating supply voltage: 3.3 V ±0.3 V
- Self-refresh.
- Various address reset mode for picture processing
- Write mask by IE.
- Package:
  100-pin plastic TQFP (TQFP100-P-1414-0.50-K) (Product : MSM548333TS-K)

PIN CONFIGURATION (TOP VIEW)



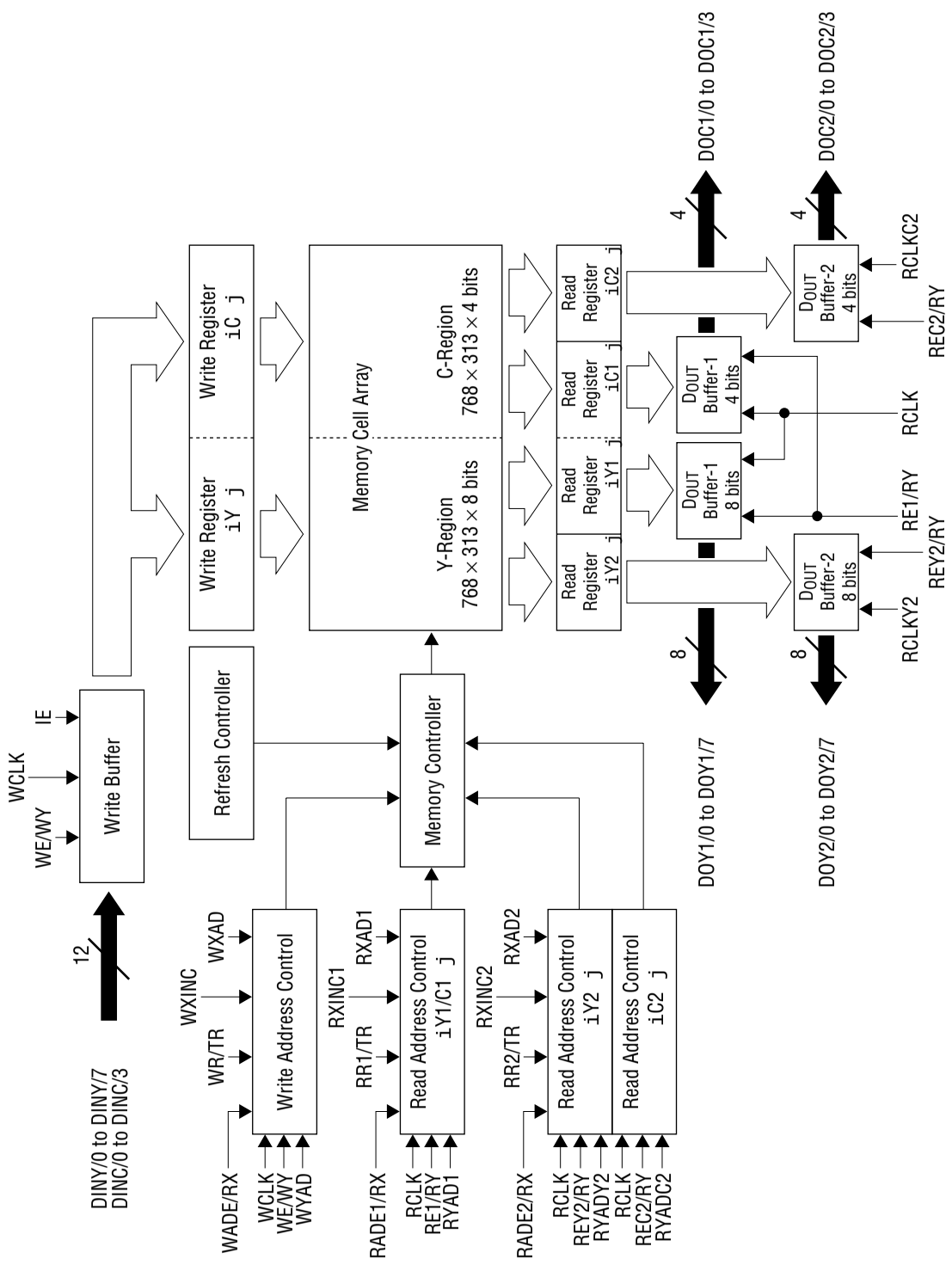
100-Pin Plastic TQFP

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	RR2/TR	26	NC	51	DOC1/1	76	NC
2	REC2/RY	27	DOY1/6	52	DOC1/0	77	DINY/1
3	RCLKC2	28	DOY1/7	53	V_{CC}	78	DINY/0
4	NC	29	V_{SS}	54	DOC2/3	79	WADE/RX
5	REY2/RY	30	V_{SS}	55	NC	80	WXINC
6	RCLKY2	31	DOY2/0	56	DOC2/2	81	WR/TR
7	RADE1/RX	32	DOY2/1	57	DOC2/1	82	NC
8	RXINC1	33	DOY2/2	58	DOC2/0	83	WE/WY
9	NC	34	NC	59	V_{SS}	84	IE
10	RR1/TR	35	DOY2/3	60	NC	85	WCLK
11	RE1/RY	36	V_{CC}	61	V_{SS}	86	WYAD
12	NC	37	V_{CC}	62	V_{CC}	87	V_{CC}
13	RCLK	38	V_{CC}	63	DINC/3	88	V_{CC}
14	NC	39	NC	64	NC	89	NC
15	V_{SS}	40	V_{CC}	65	DINC/2	90	WXAD
16	V_{SS}	41	DOY2/4	66	DINC/1	91	RYADC2
17	V_{SS}	42	NC	67	NC	92	RYADY2
18	DOY1/0	43	DOY2/5	68	DINC/0	93	RXAD2
19	DOY1/1	44	DOY2/6	69	DINY/7	94	NC
20	DOY1/2	45	DOY2/7	70	DINY/6	95	RYAD1
21	DOY1/3	46	V_{SS}	71	DINY/5	96	RXAD1
22	NC	47	V_{SS}	72	NC	97	TEST
23	V_{CC}	48	DOC1/3	73	DINY/4	98	RADE2/RX
24	DOY1/4	49	DOC1/2	74	DINY/3	99	RXINC2
25	DOY1/5	50	NC	75	DINY/2	100	NC

Pin Name	Function	
	Address Setting Cycle	Serial Read/Write Cycle
RCLK	Y1, C1, Y2 and C2 Read Ports X and Y Serial Address Strobes	Y1 and C1 Read Ports, Serial Read Clock
RE1/RY	Y1 and C1 Read Ports, Y Address Reset	Y1 and C1 Read Ports, Read Enable
DOY1/0 - 7	—	Y1 Read Port, Data Output
DOC1/0 - 3	—	C1 Read Port, Data Output
RR1/TR	Y1 and C1 Read Ports, Address Reset Mode Enable	—
RXINC1	Y1 and C1 Read Ports, X Address Increment	—
RADE1/RX	Y1 and C1 Read Ports, X and Y Address Input Enable Y1 and C1 Read Ports, X Address Reset	—
RXAD1	Y1 and C1 Read Ports, X Serial Address Data	—
RYAD1	Y1 and C1 Read Ports, Y Serial Address Data	—
RR2/TR	Y2 and C2 Read Ports, Address Reset Mode Enable	—
RXINC2	Y2 and C2 Read Ports, X Address Increment	—
RADE2/RX	Y2 and C2 Read Ports, X and Y Address Input Enable Y2 and C2 Read Ports, X Address Reset	—
RXAD2	Y2 and C2 Read Ports, X Serial Address Data	—
RYADY2	Y2 Read Port, Y Serial Address Data	—
RCLKY2	—	Y2 Read Port, Serial Read Clock
REY2/RY	Y2 Read Port, Y Address Reset	Y2 Read Port, Read Enable
DOY2/0 - 7	—	Y2 Read Port, Data Output
RYADC2	C2 Read Port, Y Serial Address Data	—
RCLKC2	—	C2 Read Port, Serial Read Clock
REC2/RY	C2 Read Port, Y Address Reset	C2 Read Port, Read Enable
DOC2/0 - 3	—	C2 Read Port, Data Output
WCLK	Y and C Write Ports, X and Y Serial Address Strobes	Y and C Write Ports, Serial Write Clock
WE/WY	Y and C Write Ports, Y Address Reset	Y and C Write Ports, Write Enable
DINY/0 - 7 DINC/0 - 3	—	Y Write Port, Input Data C Write Port, Input Data
WR/TR	Y and C Write Ports, Address Reset Mode Enable	Y and C Write Ports, Write Data Transfer
WXINC	Y and C Write Ports, X Address Increment	—
WADE/RX	Y and C Write Ports, X and Y Address Input Enable Y and C Write Ports, X Address Reset	—
WXAD	Y and C Write Ports, X Serial Address Data	—
WYAD	Y and C Write Ports, Y Serial Address Data	—
IE	—	Input Enable
V_{CC}	Power Supply Voltage (3.3 V)	
V_{SS}	Ground (0 V)	
TEST	Connect to Power Supply Voltage (3.3 V)	

Notes: 1. Same power supply voltage level must be provided to every V_{CC} pin.
Same ground voltage level must be provided to every V_{SS} pin.
2. Connect the TEST pin to the power supply.
3. NC must be opened. Don't connect to anything electrically.

BLOCK DIAGRAM



PIN FUNCTION (Note : Y1 = "port-1 of Y area", Y2 = "port-2 of Y area", C1 = "port-1 of C area", C2 = "port-2 of C area "

READ RELATED

RCLK : Read Clock for Y1 and C1, Common Read Address Strobe Clock

RCLK is the read control clock input for Y1 and C 1. Synchronized with RCLK's rising edge, serial read access from Y1 and C1 is executed when RE1/RY is high. (Note that the write port has one port, Y and C, but the read port has dual ports, Y1 and C1 plus Y2 and C2. Y1 and C1 are controlled by the common read clock RCLK. But Y2 and C2 are controlled by separated read clocks, RCLKY2 and RCLKC2, asynchronously.)

The internal counter for the serial read address is incremented automatically on the rising edge of RCLK. In a read address set cycle, all the read address bits which were input from each RXAD1, RYAD1, RXAD2, RYADY2, and RYADC2 pins are stored into internal address registers synchronized with RCLK. In this address set cycle, RADE1/RX and RADE2/RX must be held high and the RR1/TR and RR2/TR must be held low.

In the read address reset cycle, various read address reset modes can be set synchronously with RCLK. These reset cycles work to replace complicated serial address control which requires many RCLK clocks with a simple reset cycle control requiring only a single RCLK cycle. It greatly facilitates memory access.

RE1/RY : Read Enable for Y1 and C1/Read Y Address Reset Logic Function

RE1/RY is a dual function control input. RE1, one of the two functions of RE1/RY, is read enable. RE1 enables or disables both internal read address pointers and data-out buffers of Y1 and C1. When RE1/RY is high, the internal read address pointer for Y1 and C1 is incremented synchronously with RCLK. When RE1/RY is low, even if the RCLK is input, the internal read address pointer is not incremented.

RY, the second function of RE1/RY, performs a function for setting the read Y address (or bit address in a certain line) reset mode in Y1 and C1. In a read address reset mode cycle, as defined by RR1/TR being high, RY works as one of inputs which form several read reset logic as shown in the "FUNCTION TABLE for read". In the address reset cycle, when RE1/RY level is low, each Y1and C1 internal read Y address is reset to 0. When RE1/RY is high, each Y1 and C1 internal read Y address is reset to the respective address which was set in the previous read address set cycle.

DOY1/0-7 : Data-Outs for Y1

DOY1/0-7 are serial data-outs for Y1. Each corresponding data out buffer' impedance is controlled by RE1/RY.

DOC1/0-3 : Data-Outs for C1

DOC1/0-3 are serial data-outs for C1. Each corresponding data out buffer' impedance is controlled by RE1/RY.

RR1/TR : Read Reset for Y1 and C1

RR1/TR is a read reset control input for Y1 and C1. Read address reset modes are defined when RR1/TR level is high according to the "FUNCTION TABLE for read".

RXINC1 : Read X Address Increment for Y1 and C1

RXINC1 is a read X address (or line address) increment control input for Y1 and C1. In the read address reset cycle, defined by RR1/TR high, the common X address (or line address) for Y1 and C1 is incremented by RXINC1.

RADE1/RX : Read Address Enable for Y1 and C1/Read X Address Reset Logic Function
RADE1/RX is a dual function control input. RADE1, one of the two functions of RADE1/RX, is a read address enable input for Y1 and C1. In the read address set cycle, defined by RR1/TR low, X address (or line address) and Y address (or bit address in a certain line) input from the RXAD1 pin and RYAD1 pin are latched into internal read X address register and Y address register, respectively synchronously with RCLK.
RX, the second function of RADE1/RX, works as an element to set read X address (or line address) reset mode. In an address reset mode cycle, defined by RR1/TR level high, RX works as one of inputs which form several read reset logic as shown in the "FUNCTION TABLE for read".

RXAD1 : Read X Address for Y1 and C1
RXAD1 is a read X address (or line address) input for Y1 and C1. RXAD1 specifies the line address. 9 bits of read X address data are input serially from RXAD1.

RYAD1 : Read Y Address for Y1 and C1
RYAD1 is a read Y address (or bit address in a certain line) input for Y1 and C1. RYAD1 specifies the first bit address of consecutive serial read data in the line whose line address is defined by the X read address from RXAD1. 10 bits of Y address data are input serially from RYAD1.

RR2/TR : Read Reset for Y2 and C2
RR2/TR is a read reset control input for Y2 and C2. Read address reset modes for Y2 and C2 are defined when RR2/TR level is high based on the "FUNCTION TABLE for read".

RXINC2 : Read X Address Increment for Y2 and C2
RXINC2 is a read X address (or line address) increment control input for Y2 and C2. In the read address reset cycle, defined by RR2/TR high, the common read X address (or line address) for Y2 and C2 is incremented by RXINC2.

RADE2/RX : Read Address Enable for Y2 and C2/Read X Address Reset Logic Function
RADE2/RX is a dual function control input. RADE2, one of the two functions of RADE2/RX, is a read address enable input for Y2 and C2. In the read address set cycle, defined by RR2/TR high, the read X address (or line address) and the read Y address (or bit address in a certain line), which are input from the RXAD2, RYADY2 and RYADC2 pins, are latched into internal read X address register and read Y address register, respectively, synchronously with RCLK.
RX, the second function of RADE2/RX, performs a function for setting the read X address (or line address) reset mode. In a read address reset mode cycle, defined by RR2/TR level high, RX works as one of inputs which form several read reset logic as shown in the "FUNCTION TABLE for read".

RXAD2 : Read X Address for Y2 and C2
RXAD2 is a read X address (or line address) input for Y2 and C2. RXAD2 specifies the line address. 9 bits of X address data is input serially from RXAD2.

RYADY2 : Read Y Address for Y2
RYADY2 is a read Y address (or bit address in a certain line) input for Y2. RYADY2 specifies the first bit address of serial read data in the line whose line address is specified by the X address RXAD2. 10 bits of Y address data are input serially from RYADY2.

RCLKY2 : Read Clock for Y2
RCLKY2 is a read control clock input for Y2. (Note that there is RCLKC2 for C2.) Synchronized with RCLKY2's rising edge, the serial read access from Y2 is executed when REY2/RY is high.

REY2/RY : Read Enable for Y2/Read Y Address Reset Logic Function for Y2
REY2/RY is a dual function control input. REY2, one of the two functions of REY2/RY, enables or disables both internal read address pointers and data-out buffers of Y2. When REY2/RY is high, the internal read address pointer for Y2 is incremented synchronously with RCLKY2. When REY2/RY is low, even if RCLKY2 is input, the internal read address pointer is not incremented.
RY, the second function of REY2/RY, works as an element to set read Y address (or bit address in a certain line) reset mode. In a read address reset mode cycle, defined by RR2/TR high, RY works as one of inputs which form several read reset logic as shown in the "FUNCTION TABLE for read". In the read address reset cycle, when REY2/RY is low, the internal read Y address for Y2 is reset to 0. When REY2/RY is high, the internal read Y address for Y2 is reset to the address which was set in the previous address set cycle.

DOY2/0-7 : Data-Outs for Y2
DOY2/0-7 are serial data-outs for Y2. Each corresponding data-out-buffer' impedance is controlled by REY2/RY.

RYADC2 : Read Y Address for C2
RYADC2 is a read Y address (or bit address in a certain line) input only for C2. RYADC2 specifies the first bit address of serial read data in the line whose line address is specified by RXAD2. 10 bits of Y address data are input serially from RYADC2.

RCLKC2 : Read Clock for C2
RCLKC2 is a read control clock input for only C2. (Note that there is RCLKY2 for Y2.) Synchronized with RCLKC2, serial read access from C2 is executed when REC2/RY is high.

REC2/RY : Read Enable for C2/Read Y Address Reset Logic Function for C2
REC2/RY is a dual function control input. REC2, one of the two functions of REC2/RY, enables or disables both internal read address pointers and data-out buffers for C2. When REC2/RY is high, the internal read address pointer for C2 is incremented synchronously with RCLKC2. When REC2/RY is low, even if RCLKC2 is input, the internal read address pointer is not incremented.
RY, the second function of REC2/RY, performs a function for setting the read Y address (or bit address in a certain line) reset mode. In an address reset mode cycle, defined by RR2/TR high, RY works as one of inputs which form several read reset logic as shown in the "FUNCTION TABLE for read". In the read address reset cycle, when REC2/RY is low, the internal read Y address for C2 is reset to 0. When REC2/RY is high, the internal read Y address for C2 is reset to the address which was set in the previous read address set cycle.

DOC2/0-3 : Data-Outs for C2
DOC2/0-3 are serial data-outs for C2. Each corresponding data out buffer' impedance is controlled by REC2/RY.

WRITE RELATED

WCLK : Write Clock for Y and C

WCLK is a write control clock input for Y and C ports. Synchronized with WCLK's rising edge, serial write access into Y and C ports is executed when WE/WY is high and IE is high. (Note that the read port is dual port, Y1 and C1 + Y2 and C2, but write port has only one port, Y + C. X8 of Y and X4 of C inputs are controlled by a common WCLK, that is, in the write port, the MSM548333 is controlled as a X12 FRAM.)

According to WCLK clocks, the internal counter for the serial address is incremented automatically. In a write address set cycle, all the write addresses which were input from WXAD and WYAD are stored into internal address registers synchronously with WCLK. In this address set cycle, WADE/RX must be held high and WR/TR must be held low.

In the write address reset cycle, various write address reset modes can be set synchronously with WCLK. These reset cycles replace complicated serial address control with simple reset cycle control which requires only one WCLK cycle. It greatly facilitates memory access.

WE/WY : Write Enable for Y and C/Write Y Address Reset Logic Function

WE/WY is a dual function control input. WE, one of the two functions of WE/WY, is write enable. WE enables or disables both internal write address pointers and data-in buffers of Y and C. When WE/WY is high, the internal write address pointer for Y and C is incremented synchronously with WCLK. When WE/WY is low, even if WCLK is input, the internal write address pointer is not incremented.

WY, the second function of WE/WY, performs a function for setting the write Y address (or bit address in a certain line) reset mode in Y and C. In a write address reset mode cycle, defined by WR/TR high, WY works as one of inputs which form several write reset logic as shown in the "FUNCTION TABLE for write". In the address reset cycle, when WE/WY level is low, each Y and C internal write Y address is reset to 0. When WE/WY is high, each Y and C internal write Y address is reset to the respective address which was set in the previous write address set cycle.

DINY/0-7 : Data-Ins for Y

DINY/0-7 are serial data-ins for Y. Each corresponding data-in-buffer is masked by IE.

DINC/0-3 : Data-Ins for C

DINC/0-3 are serial data-ins for C. Each corresponding data-in-buffer is masked by IE.

WR/TR : Write Reset for Y and C

WR/TR is a write reset control input for Y and C. Write address reset modes are defined when WR/TR level is high according to the "FUNCTION TABLE for write".

WXINC : Write X Address Increment for Y and C

WXINC is a write X address (or line address) increment control input for Y and C. In the write address reset cycle, defined by WR/TR high, the common write X address (or line address) for Y and C is incremented by WXINC.

WADE/RX : Write Address Enable for Y and C/Write X Address Reset Logic Function

WADE/RX is a dual functional control input. WADE, one of the two functions of WADE/RX, is a write address enable input for Y and C. In the write address reset cycle, defined by WR/TR high, X address (or line address) and Y address (or bit address in a certain line) input from WXAD and WYAD are latched into internal write X address register and Y address register.

WXAD : Write X Address for Y and C

WXAD is a write X address (or line address) input for Y and C. WXAD specifies line address. 9 bits of write X address data are input serially from WXAD.

WYAD : Write Y Address for Y and C

WYAD is a read Y address (or bit address in a certain line) input for Y and C. WYAD specifies the first bit address of consecutive serial write data in the line whose line address is defined by X write address from WXAD. 10 bits of write Y address data are input serially from WYAD.

IE : Input Enable for Y and C

IE is an input enable which controls the write operation. When IE is high, the input operation is enabled. When IE is low, the write operation is masked. When WE/WY signal is high, and IE low, the internal serial write address pointer is incremented on the rising edge of WCLK without actual write operations. This function facilitates picture in picture function in a TV system.

OPERATION MODE

Write

1. Write operation
   Before the write operation begins, X address (or line address) and Y address (or bit address in the line specified by the X address) must be input to set the initial bit address for the following serial write access. When WE/WY and IE are high, a set of serial 12-bit-width write data on DINY/0-7 and DINC/0-3 is written into write registers attached to the DRAM memory arrays temporarily on the rising edge of WCLK.
   Following 12-bit-width serial input data is written into the memory locations in the write register designated by an internal write address pointer which is advanced by WCLK. This enables continuous serial write on a line. When write clock WCLK and read clock RCLK are tied together and are controlled by a common clock or CLK, more than two MSM548333s can be cascaded directly without any delay devices between the MSM548333s because the read timing is delayed by one CLK cycle to the write timing. When the write operation on a line is terminated, be sure to perform a write transfer operation by WR/TR in order to store the written data in the write registers to the corresponding memory cells in the DRAM memory arrays.

2. Write address pointer increment operation
   The write address pointer is incremented synchronously with WCLK when WE/WY is high. When the write address pointer reaches the last address of a line, it stops at the last address and no address increment occurs.

   Relationship between the WE/WY and IE input levels, Write Address pointer, and data input status

WCLK Rise		Internal Write Address Pointer	Data Input
WE/WY	IE		
H	H	Incremented	Inputted
H	L		Not Inputted
L	—	Stopped	

   When WE/WY and IE are high, the write operation is enabled.
   If IE level goes low while WCLK is active, the write operation is halted but the write address pointer will continue to advance. That is, IE enables a write mask function. When WE/WY goes low, the write address pointer stops without WCLK.

Read (Here, "port-1 of Y area" is Y1, "port-2 of Y area" is Y2, "port-1 of C area" is C1, "port-2 of C area" is C2.)

1. Read operation
   MSM548333 has dual read ports, port-1 for Y and C memory areas and port-2 for Y and C memory areas. Note that the read of Y1 and C1 are controlled by a common control clock at the same time. But the read of Y2 and C2 are controlled by separate sets of control clocks, independently.
   Before the read operation begins, the X address (or line address) and Y address (or bit address in the line specified by the X address) must be input for setting initial bit address for the following serial read access.
   When RE1/RY is high, a set of serial 12-bit-width read data on DOY1/0-7 pins and DOC1/0-3 pins is read from read registers attached to DRAM memory arrays on the rising edge of RCLK.
   When REY2/RY is high, a set of serial 8-bit-width read data on DOY2/0-7 pins is read from read registers attached to DRAM memory arrays on the rising edge of RCLKY2.

When REC2/RY is high, a set of 4-bit-width serial read data on DOC2/0-3 is read from the read registers attached to DRAM memory arrays on the rising edge of RCLKC2. Each access time is specified by the rising edges of RCLK, RCLKY2 and RCLKC2.

2. Read address pointer increment operation
   There are three separate pointers for dual port serial read operation. The first one is the read pointer for Y1 and C1 which is incremented by RCLK when RE1/RY is high. The second one is the read pointer for Y2 which is incremented by RCLKY2 when REY2/RY is high. The third one is the read pointer for C2 which incremented by RCLKC2 when REC2/RY is high. When each read address pointer reaches the last address of a line, it stops at the last address and no address increment occurs.

Initial Address Setting (Write/Read Independent)

Any read operations are prohibited in the read initial address set period. Similarly, any write operations are prohibited in the write initial address set period. Note that read initial address set and write initial address set can occur independently. Similarly, read access can be achieved independently from write initial address set period and write access can be achieved independently from read initial address set cycles.

1. Write address setting
   During a write, MSM548333 has one write address enable input, WADE/RX. Note that there are two read address enable inputs for read. WADE/RX enables Y and C initial read address inputs. When WADE/RX is high, 9 bits of serial X address (or line address) for Y and C and 10 bits of serial Y address (or bit address in the line specified by the X address) for Y and C are input in parallel from WXAD and WYAD respectively.
   The operations above enable selection of specific lines randomly and enables the start of serial write access synchronized with write clock WCLK. Address for each line must be input between each line access. In other words, MSM548333's write is achieved in a "line by line" manner. Any write operations are prohibited in the initial write address set periods.
   Y and C Serial write input enable time t_{SWE} must be kept for starting a serial write just after the initial write address set period.

2. Read address setting
   During a read, MSM548333 has two read address enable inputs, RADE1/RX and RADE2/RX. RADE1/RX enables Y1 and C1 initial read address inputs. Similarly, RADE2/RX enables Y2 and C2 initial read address inputs.
   When RADE1/RX is high, 9 bits of serial X address (or line address) for Y1 and C1 and 10 bits of serial Y address (or bit address in the line specified by the X address) for Y1 and C1 are input in parallel from RXAD1 and RYAD1, respectively. Note that the X and Y address inputs when RADE1/RX is high are for Y1 and C1.
   When RADE2/RX is high, 9 bits of serial X address (or line address) for Y2 and C2 is input from RXAD2. In the same period, 10 bits of serial Y address (or bit address in the line specified by the X address) for Y2 is input from RYADY2 pin and another 10 bits of serial Y address (or bit address in the line specified by the same X address input from RXAD2) for C2 is input from RYADC2 pin. Note that the X address input here is for both Y2 and C2 and the two sets of Y address inputs from RYADY2 and RYADC2 are for Y2 and C2, respectively. That is, MSM548333 can't set separate line addresses in Y2 and C2 but can set separate initial bit address in Y2 and C2 on the specified lines by the common line address.
   The operations above enable selection of specific lines randomly and enables the start of serial read access synchronized with read clocks, RCLK for Y1 and C1, RCLKY2 for Y2 and RCLKC2 for C2. Address for each line must be input between each line access. In other words,

MSM548333's read operation is achieved in "line by line" manner.
Any read operations are prohibited in the initial read address set periods. Serial read operations for Y1 and C1, and also Y2 and C2, are prohibited while RADE1/RX is high. Similarly, serial read operations for Y1 and C1, and also Y2 and C2, are prohibited while RADE2/RX level is high. Y1 and C1 Serial read port enable time t_{SRE1}, Y2 serial read port enable time t_{SREY2} and C2 serial read port enable time t_{SREC2} must be kept for starting a serial read just after the initial read address set period.

Initial Address Reset Modes (Write/Read Independent)

The initial address reset modes replace complicated read or write initial address settings with simple reset cycles. Initial address reset modes are selected by RR/TR high during read and WR/TR high during write. As in normal read or write address settings, any read operations are prohibited in the read address reset cycles. Similarly, any write operations are prohibited in the initial write address reset cycles. Note that read initial address reset and write initial address reset can occur independently. Similarly, read access can be achieved independently from write initial address reset cycles and write access can be achieved independently from read initial address reset cycles.
Input addresses are stored into address registers which are connected with address counter which controls address pointer operation. In the serial access operation, the input address into the address registers are kept.
Serial write data input enable time t_{SWE}, Y1 and C1 read port read enable time t_{SRE1}, Y2 serial read port read enable time t_{SREY2}, C2 serial read port read enable time t_{SREC2} must be kept for starting serial read or write just after the initial read or write address reset cycles. Note that all the read ports' initial address reset must occur with the same timing.

1. Original address reset No.1 - "X, Y address counter reset" -
   By the "Original address reset No.1" logic which is composed by a combination of control input' levels, the address counter is reset to (0,0), and then, the address pointer is initialized to (0,0). Reference the "FUNCTION TABLE" for read and write shown later. After the reset mode, serial access starts from the address (0,0) : the line address is "0" and the initial bit address on the line is (0,0).
   The address counter is reset by this reset mode but the address register, which stored input address in the previous address reset cycle or address set cycle, is not reset. The non-initialized address can be used as a preset address in "address jump reset" mode. When the address register must be reset, choose "address register reset" mode.

2. Original address reset No.2 - "X,Y address register reset" -
   By the "Original address reset No.2" logic, the address register is reset, and then, the address counter and address pointer are initialized to address (0,0) automatically. After the reset mode, serial access starts from the address (0,0) : the line address is "0" and the initial bit address on the line is (0,0)
   Both address register and address counter are reset to (0,0) and the stored initial address in the previous address reset cycle or address set cycle is cleared by this "address register reset". Once the reset mode is selected, the reset address (0,0) is stored in the address register as a preset address until next initial address set or reset operation. The address can be used as a preset address in the "address jump reset" mode.
   Note that REY2/RY and REC2/C2 must be both "L" at the same time when the "address register reset" is selected. REY2/RY = "L" and REC2/RY = "H" or REY2/RY = "H" and REC2/RY = "L" are prohibited.

3. Original address reset No.3 - Y address counter reset" -
   By the "Original address reset No.3" logic, the Y address register is reset, and then, address

pointer for the line access is initialized to Y address (0). The X address Xi which specifies a certain line address is one which was stored in the X address register in the previous address reset or address set cycle. After the reset mode, serial access starts from the address (Xi,0) : line address is "Xi" and initial bit address on the line is (0).
The Y address counter is reset by this reset mode but the Y address register, which stored the input initial Y address in the previous address reset cycle or address set cycle, is not reset. The non-initialized Y address can be used as a preset Y address in the "address jump reset" mode.

4. Line increment reset No.1 - "X address counter increment and Y address counter reset" -
   By the "Line increment reset No.1" logic, the X address counter is incremented by one from the current X address and Y address is reset to address (0). That is, by the reset mode, serial access from the Y = (0) on the next line is enabled.

5. Line increment reset No.2 - "X address counter increment reset and Y address counter initialize" -
   By the "Line increment reset No.2" logic, the X address counter is incremented by one from the current X address and Y address is initialized to the Y address set in the previous address set cycle. This enables block access on the screen.

6. Line hold reset No. 1 (1) operation
   When a predetermined input level is set during the reset setting cycle, access is executed starting from the first word on the current line.

7. Line hold (2) operation
   When a predetermined input level is set during the reset setting cycle, access is executed starting from the word address on the current line which is initialized.

8. Address jump operation
   When a predetermined input level is set during the reset setting cycle, a jump may be caused to the initialized line or word address.
   In the case of a read, set the same level in the Y2 and C2 regions for this operation.

Note : During one reset setting cycle, a plurality of resets cannot be set.

Power ON

Power must be applied to RCLK, RCLKY2, RCLKC2, RE1/RY, REY2/RY, REC2/RY and WE/WY input signals to pull them "Low" before or when the V_{CC} supply is turned on.
After power-up, the device is designed to begin proper operation in at least 200 µs after V_{CC} has reached the specified voltage. After 200 µs, a minimum of one line dummy write operation and read operation is required according to the address setting mode, because the read and write address pointers are not valid after power-up.

New Data Read Access

In order to read out "new data', the delay between the beginning of a write address setting cycle and read address setting cycle must be at least two lines.

Old Data Read Access

In order to read out "old data", the delay between the beginning of a write address setting cycle and read address setting cycle must be more than 0 but less than a half line.

FUNCTION TABLE

1. Write

Mode	No.	Description of Operation	WR/TR	WXINC	WE/WY	WADE/ RX	Internal Address Pointer
Address Reset Mode	1	Write Transfer	H	L	L	L	
	2	Reset (1)	H	L	L	H	X and Y cleared to (0, 0)
	3	Reset (2) (Note)	H	H	L	H	X and Y cleared to (0, 0)
	4	Line Increment (1)	H	H	L	L	X set and Y cleared to (Xn + 1, 0)
	5	Line Increment (2)	H	H	H	L	X and Y set to (Xn +1, Yi)
	6	Reset (3)	H	L	H	H	X cleared and Y set to (0, Yi)
	7	Line Hold (2)	H	L	H	L	X and Y set to (Xn, Yi)
	8	Address Jump	H	H	H	H	X and Y set to (Xi, Yi)
Address Setting Mode	—	First Address Setting	L	L	L	H	X and Y set

Note : When Address reset mode No. 3 is executed, the address X and Y which are set previously will be cleared. For write, Line hold (1) is not provided.

2. Read

Mode	No.	Description of Operation	RR*/TR	RXINC*	RE*/RY	RADE* /RX	Internal Address Pointer
Address Reset Mode	1	Line Hold (1)	H	L	L	L	X set and Y cleared to (Xn, 0)
	2	Reset (1)	H	L	L	H	X and Y cleared to (0, 0)
	3	Reset (2) (Note)	H	H	L *	H	X and Y cleared to (0, 0)
	4	Line Increment (1)	H	H	L	L	X set and Y cleared to (Xn + 1, 0)
	5	Line Increment (2)	H	H	H	L	X and Y set to (Xn + 1, Yi)
	6	Reset (3)	H	L	H	H	X cleared and Y set to (0, Yi)
	7	Line Hold (2)	H	L	H	L	X and Y set to (Xn, Yi)
	8	Address Jump	H	H	H *	H	X and Y set to (Xi, Yi)
Address Setting Mode	—	First Address Setting	L	L	L	H	X and Y set

RR*/TR : RR1/TR, RR2/TR
RE*/RY : RE1/RY, REY2/RY, REC2/RY
RXINC* : RXINC1, RXINC2
RADE*/RX : RADE1/RX, RADE2/RX

* Set the same level in the Y2 and C2 regions.

Note : When address reset mode No. 3 is executed, the addresses X and Y which are set previously will be cleared.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating
Pin Voltage	V_T	Ta = 25°C, with respect to V_{SS}	–0.5 to 4.6 V
Short Circuit Output Current	I_{OS}	Ta = 25°C	50 mA
Power Dissipation	P_D	Ta = 25°C	1 W
Operating Temperature	T_{opr}	—	0 to 70°C
Storage Temperature	T_{stg}	—	–55 to 150°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Power Supply Voltage	V_{SS}	0	0	0	V
"H" Input Voltage	V_{IH}	2.1	V_{CC}	V_{CC} + 0.3	V
"L" Input Voltage	V_{IL}	–0.5	0	0.8	V

DC Characteristics

(V_{CC} = 3.0 to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Output Voltage	V_{OH}	I_{OH} = –0.1 mA	2.2	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 0.1 mA	—	0.7	V
Input Leakage Current	I_{LI}	$0 < V_I < V_{CC} + 1$ Other input voltage 0 V	–10	10	µA
Output Leakage Current	I_{LO}	$0 < V_O < 3.6$	–10	10	µA
Power Supply Current (During Operation)	I_{CC1}	min. cycle	—	50	mA
Power Supply Voltage (During Standby)	I_{CC2}	Input pin = V_{IL}/V_{IH}	—	10	mA

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance	C_I	7	pF
Output Capacitance	C_O	7	pF

AC Characteristics (1/4)

Measurement Conditions: (V_{CC} = 3.3 V ±0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Min.	Max.	Unit
WCLK Cycle Time	t_{WCLK}	50	—	ns
WCLK "H" Pulse Width	t_{WWCLH}	15	—	ns
WCLK "L" Pulse Width	t_{WWCLL}	15	—	ns
Serial Write Address Input Active Setup Time	t_{WAS}	5	—	ns
Serial Write Address Input Active Hold Time	t_{WAH}	7	—	ns
Serial Write Address Input Inactive Hold Time	t_{WADH}	7	—	ns
Serial Write Address Input Inactive Setup Time	t_{WADS}	7	—	ns
Write Transfer Instruction Setup Time	t_{WTRS}	5	—	ns
Write Transfer Instruction Hold Time	t_{WTRH}	7	—	ns
Write Transfer Instruction Inactive Hold Time	t_{WTDH}	7	—	ns
Write Transfer Instruction Inactive Setup Time	t_{WTDS}	7	—	ns
Serial Write X Address Setup Time	t_{WXAS}	5	—	ns
Serial Write X Address Hold Time	t_{WXAH}	7	—	ns
Serial Write Y Address Setup Time	t_{WYAS}	5	—	ns
Serial Write Y Address Hold Time	t_{WYAH}	7	—	ns
Serial Write Data Input Enable Time	t_{SWE}	5000	—	ns
Write Instruction Setup Time	t_{WES}	5	—	ns
Write Instruction Hold Time	t_{WEH}	7	—	ns
Write Instruction Inactive Hold Time	t_{WEDH}	7	—	ns
Write Instruction Inactive Setup Time	t_{WEDS}	7	—	ns
IE Enable Setup Time	t_{IES}	5	—	ns
IE Enable Hold Time	t_{IEH}	7	—	ns
IE Disable Hold Time	t_{IEDS}	7	—	ns
IE Disable Setup Time	t_{IEDH}	7	—	ns
Input Data Setup Time	t_{DS}	5	—	ns
Input Data Hold Time	t_{DH}	15	—	ns
WR/TR-WCLK Active Setup Time	t_{WRS}	5	—	ns
WR/TR-WCLK Active Hold Time	t_{WRH}	7	—	ns
WR/TR-WCLK Inactive Hold Time	t_{WRDH}	7	—	ns
WR/TR-WCLK Inactive Setup Time	t_{WRDS}	7	—	ns
WXINC-WCLK Active Setup Time	t_{WINS}	5	—	ns
WXINC-WCLK Active Hold Time	t_{WINH}	7	—	ns
WXINC-WCLK Inactive Hold Time	t_{WINDH}	7	—	ns
WXINC-WCLK Inactive Setup Time	t_{WINDS}	7	—	ns
WADE/RX-WCLK Active Setup Time	t_{WRXS}	5	—	ns
WADE/RX-WCLK Active Hold Time	t_{WRXH}	7	—	ns
WADE/RX-WCLK Inactive Hold Time	t_{WRXDH}	7	—	ns
WADE/RX-WCLK Inactive Setup Time	t_{WRXDS}	7	—	ns
WE/WY-WCLK Active Setup Time	t_{WRYS}	5	—	ns

AC Characteristics (2/4)

Measurement Conditions: (V_{CC} = 3.3 V ±0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Min.	Max.	Unit
WE/WY-WCLK Active Hold Time	t_{WRYH}	7	—	ns
WE/WY-WCLK Inactive Hold Time	t_{WRYDH}	7	—	ns
WE/WY-WCLK Inactive Setup Time	t_{WRYDS}	7	—	ns
RCLK Cycle Time	t_{RCLK}	30	—	ns
RCLK "H" Pulse Width	t_{WRCLH}	12	—	ns
RCLK "L" Pulse Width	t_{WRCLL}	12	—	ns
RR1/TR-RCLK Active Setup Time	t_{RRS1}	5	—	ns
RR1/TR-RCLK Active Hold Time	t_{RRH1}	7	—	ns
RR1/TR-RCLK Inactive Hold Time	t_{RRDH1}	7	—	ns
RR1/TR-RCLK Inactive Setup Time	t_{RRDS1}	7	—	ns
RXINC1-RCLK Active Setup Time	t_{RINS1}	5	—	ns
RXINC1-RCLK Active Hold Time	t_{RINH1}	7	—	ns
RXINC1-RCLK Inactive Hold Time	t_{RINDH1}	7	—	ns
RXINC1-RCLK Inactive Setup Time	t_{RINDS1}	7	—	ns
RADE1/RX-RCLK Active Setup Time	t_{RRXS1}	5	—	ns
RADE1/RX-RCLK Active Hold Time	t_{RRXH1}	7	—	ns
RADE1/RX-RCLK Inactive Hold Time	t_{RRXDH1}	7	—	ns
RADE1/RX-RCLK Inactive Setup Time	t_{RRXDS1}	7	—	ns
RE1/RY-RCLK Active Setup Time	t_{RRYS1}	5	—	ns
RE1/RY-RCLK Active Hold Time	t_{RRYH1}	7	—	ns
RE1/RY-RCLK Inactive Hold Time	t_{RRYDH1}	7	—	ns
RE1/RY-RCLK Inactive Setup Time	t_{RRYDS1}	7	—	ns
Y1 and C1 Read Port Output Instruction Setup Time	t_{RES1}	5	—	ns
Y1 and C1 Read Port Output Instruction Hold Time	t_{REH1}	t_{AC1}	—	ns
Y1 and C1 Read Port Output Instruction Inactive Hold Time	t_{REDH1}	7	—	ns
Y1 and C1 Read Port Output Instruction Inactive Setup Time	t_{REDS1}	7	—	ns
Y1 and C1 Read Port Read EnableTime	t_{SRE1}	5000	—	ns
Y1 and C1 Read Port Read Data Hold Time	t_{OH1}	15	—	ns
Y1 and C1 Output Access Time	t_{AC1}	\	30	ns
Y1 and C1 Data Output Turn Off Delay Time	t_{OHZ1}	20	—	ns
RR2/TR-RCLK Active Setup Time	t_{RRS2}	5	—	ns
RR2/TR-RCLK Active Hold Time	t_{RRH2}	7	—	ns
RR2/TR-RCLK Inactive Hold Time	t_{RRDH2}	7	—	ns
RR2/TR-RCLK Inactive Setup Time	t_{RRDS2}	7	—	ns
RXINC2-RCLK Active Setup Time	t_{RINS2}	5	—	ns
RXINC2-RCLK Active Hold Time	t_{RINH2}	7	—	ns
RXINC2-RCLK Inactive Hold Time	t_{RINDH2}	7	—	ns
RXINC2-RCLK Inactive Setup Time	t_{RINDS2}	7	—	ns
RADE2/RX-RCLK Active Setup Time	t_{RRXS2}	5	—	ns

AC Characteristics (3/4)

Measurement Conditions: (V_{CC} = 3.3 V ±0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Min.	Max.	Unit
RADE2/RX-RCLK Active Hold Time	t_{RRXH2}	7	—	ns
RADE2/RX-RCLK Inactive Hold Time	t_{RRXDH2}	7	—	ns
RADE2/RX-RCLK Inactive Setup Time	t_{RRXDS2}	7	—	ns
RCLKY2 Cycle Time	t_{RCLKY}	30	—	ns
RCLKY2 "H" Pulse Width	t_{WRCLHY}	12	—	ns
RCLKY2 "L" Pulse Width	t_{WRCLLY}	12	—	ns
REY2/RY-RCLK Active Setup Time	t_{RRYSY2}	5	—	ns
REY2/RY-RCLK Active Hold Time	t_{RRYHY2}	7	—	ns
REY2/RY-RCLK Inactive Hold Time	$t_{RRYDHY2}$	7	—	ns
REY2/RY-RCLK Inactive Setup Time	$t_{RRYDSY2}$	7	—	ns
Y2 Read Port Output Instruction Setup Time	t_{RESY2}	5	—	ns
Y2 Read Port Output Instruction Hold Time	t_{REHY2}	t_{ACY2}	—	ns
Y2 Read Port Output Instruction Inactive Hold Time	t_{REDHY2}	7	—	ns
Y2 Read Port Output Instruction Inactive Setup Time	t_{REDSY2}	7	—	ns
Y2 Read Port Enable Time	t_{SREY2}	5000	—	ns
Y2 Read Port Read Data Hold Time	t_{OHY2}	15	—	ns
Y2 Output Access Time	t_{ACY2}	—	30	ns
Y2 Data Output Turn Off Delay Time	t_{OHZY2}	20	—	ns
RCLKC2 Cycle Time	t_{RCLKC}	30	—	ns
RCLKC2 "H" Pulse Width	t_{WRCLHC}	12	—	ns
RCLKC2 "L" Pulse Width	t_{WRCLLC}	12	—	ns
REC2/RY-RCLK Active Setup Time	t_{RRYSC2}	5	—	ns
REC2/RY-RCLK Active Hold Time	t_{RRYHC2}	7	—	ns
REC2/RY-RCLK Inactive Hold Time	$t_{RRYDHC2}$	7	—	ns
REC2/RY-RCLK Inactive Setup Time	$t_{RRYDSC2}$	7	—	ns
C2 Read Port Output Instruction Setup Time	t_{RESC2}	5	—	ns
C2 Read Port Output Instruction Hold Time	t_{REHC2}	t_{ACC2}	—	ns
C2 Read Port Output Instruction Inactive Hold Time	t_{REDHC2}	7	—	ns
C2 Read Port Output Instruction Inactive Setup Time	t_{REDSC2}	7	—	ns
C2 Read Port Enable Time	t_{SREC2}	5000	—	ns
C2 Read Port Read Data Hold Time	t_{OHC2}	15	—	ns
C2 Output Access Time	t_{ACC2}	—	30	ns
C2 Data Output Turn Off Delay Time	t_{OHZC2}	20	—	ns
Y1 and C1 Serial Read Address Input Active Setup Time	t_{RAS1}	5	—	ns
Y1 and C1 Serial Read Address Input Active Hold Time	t_{RAH1}	7	—	ns
Y1 and C1 Serial Read Address Input Inactive Hold Time	t_{RADH1}	7	—	ns
Y1 and C1 Serial Read Address Input Inactive Setup Time	t_{RADS1}	7	—	ns
Y1 and C1 Serial Read X Address Setup Time	t_{RXAS1}	5	—	ns
Y1 and C1 Serial Read X Address Hold Time	t_{RXAH1}	7	—	ns

AC Characteristics (4/4)

Measurement Conditions: (V_{CC} = 3.3 V ±0.3 V, Ta = 0 to 70°C)

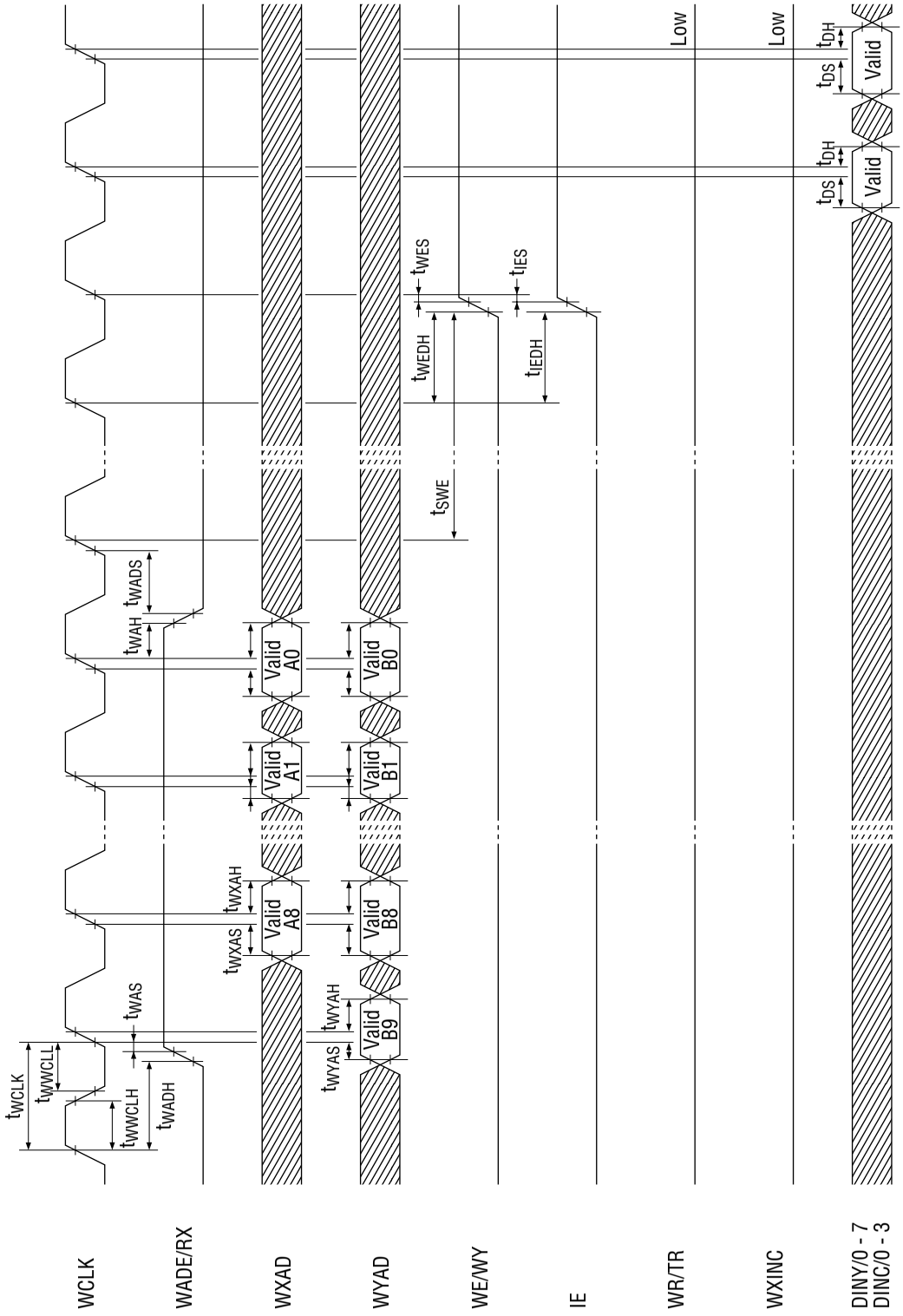
Parameter	Symbol	Min.	Max.	Unit
Y1 and C1 Serial Read Y Address Setup Time	t_{RYAS1}	5	—	ns
Y1 and C1 Serial Read Y Address Hold Time	t_{RYAH1}	7	—	ns
Y2 and C2 Serial Read Address Input Active Setup Time	t_{RAS2}	5	—	ns
Y2 and C2 Serial Read Address Input Active Hold Time	t_{RAH2}	7	—	ns
Y2 and C2 Serial Read Address Input Inactive Hold Time	t_{RADH2}	7	—	ns
Y2 and C2 Serial Read Address Input Inactive Setup Time	t_{RADS2}	7	—	ns
Y2 and C2 Serial Read X Address Setup Time	t_{RXAS2}	5	—	ns
Y2 and C2 Serial Read X Address Hold Time	t_{RXAH2}	7	—	ns
Y2 Serial Read Y Address Setup Time	t_{RYASY2}	5	—	ns
Y2 Serial Read Y Address Hold Time	t_{RYAHY2}	7	—	ns
C2 Serial Read Y Address Setup Time	t_{RYASC2}	5	—	ns
C2 Serial Read Y Address Hold Time	t_{RYAHC2}	7	—	ns
Transition Time (Rise and Fall)	t_T	3	30	ns

Note : Measurement conditions

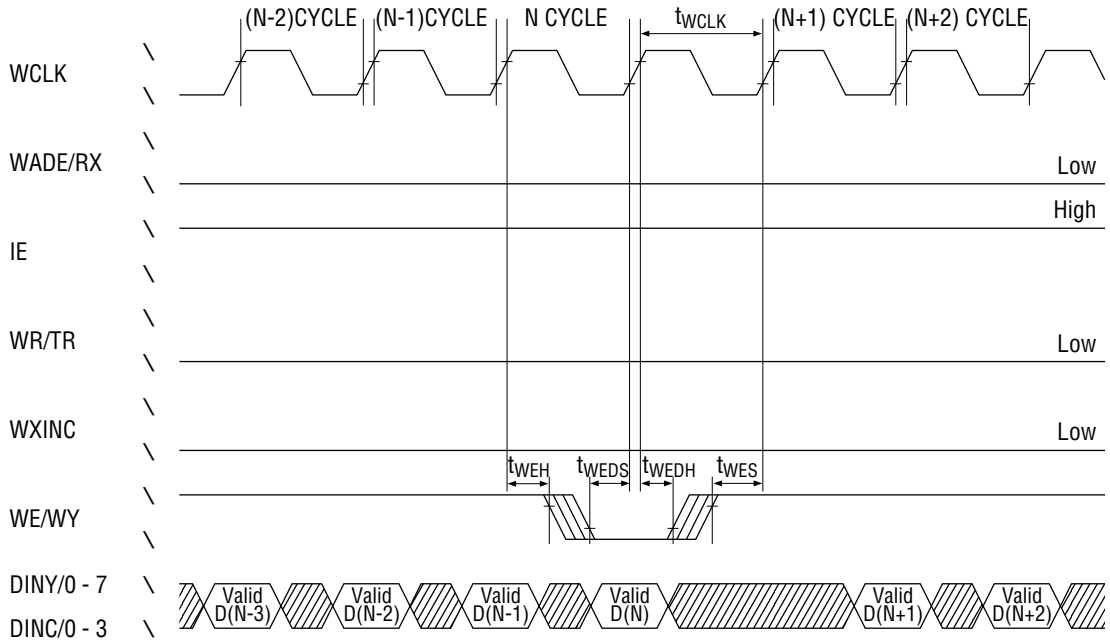
Input pulse level	: $V_{IH} = V_{CC} - 0.3$ V, $V_{IL} = 0.5$ V
Input timing reference level	: $V_{IH} = V_{CC} - 0.3$ V, $V_{IL} = 0.5$ V
Output timing reference level	: $V_{OH} = 2.2$ V, $V_{OL} = 0.7$ V
Input rise/fall time	: 3 ns
Load condition	: CL = 30 pF (Oscilloscope and tool capacity included)

TIMING WAVEFORM

Write Cycle (Address Setting Cycle)

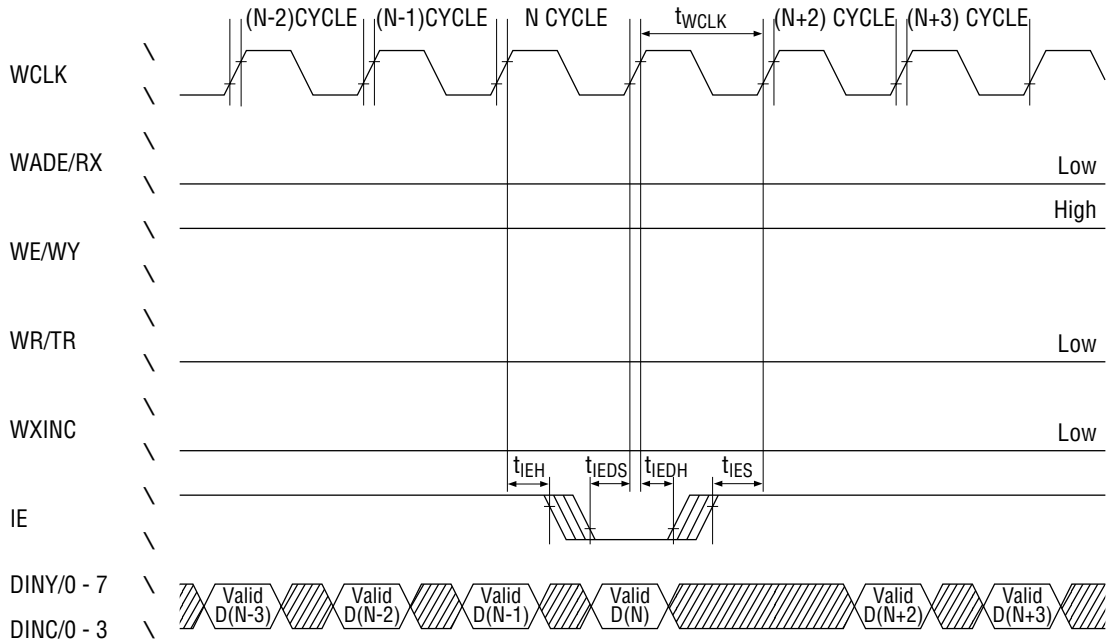


Write Cycle (WE Control)



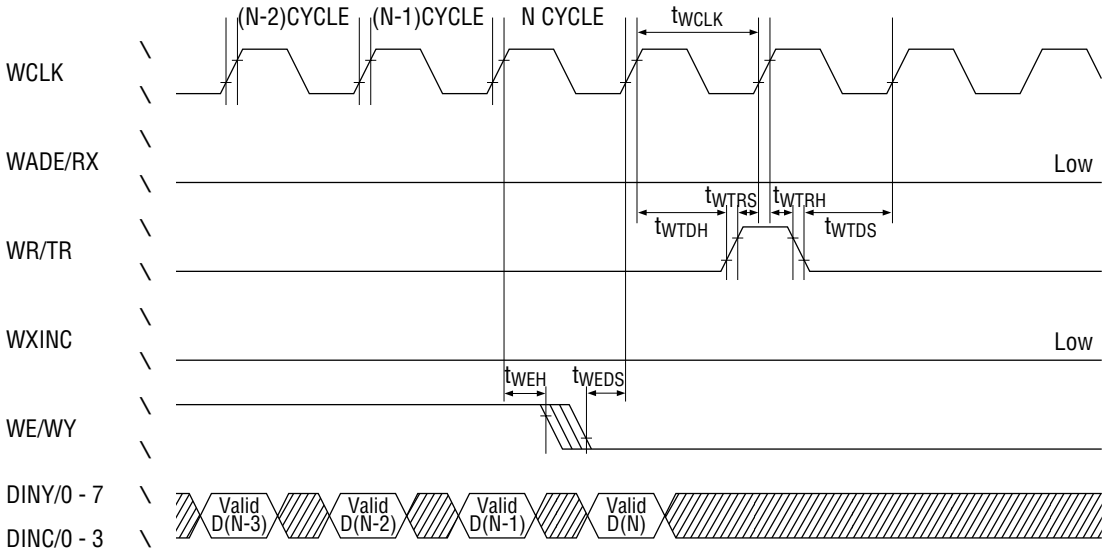
Note : In the WE/WY = "L" cycle, the write address pointer is not incremented and no DIN data is written.

Write Cycle (IE Control)



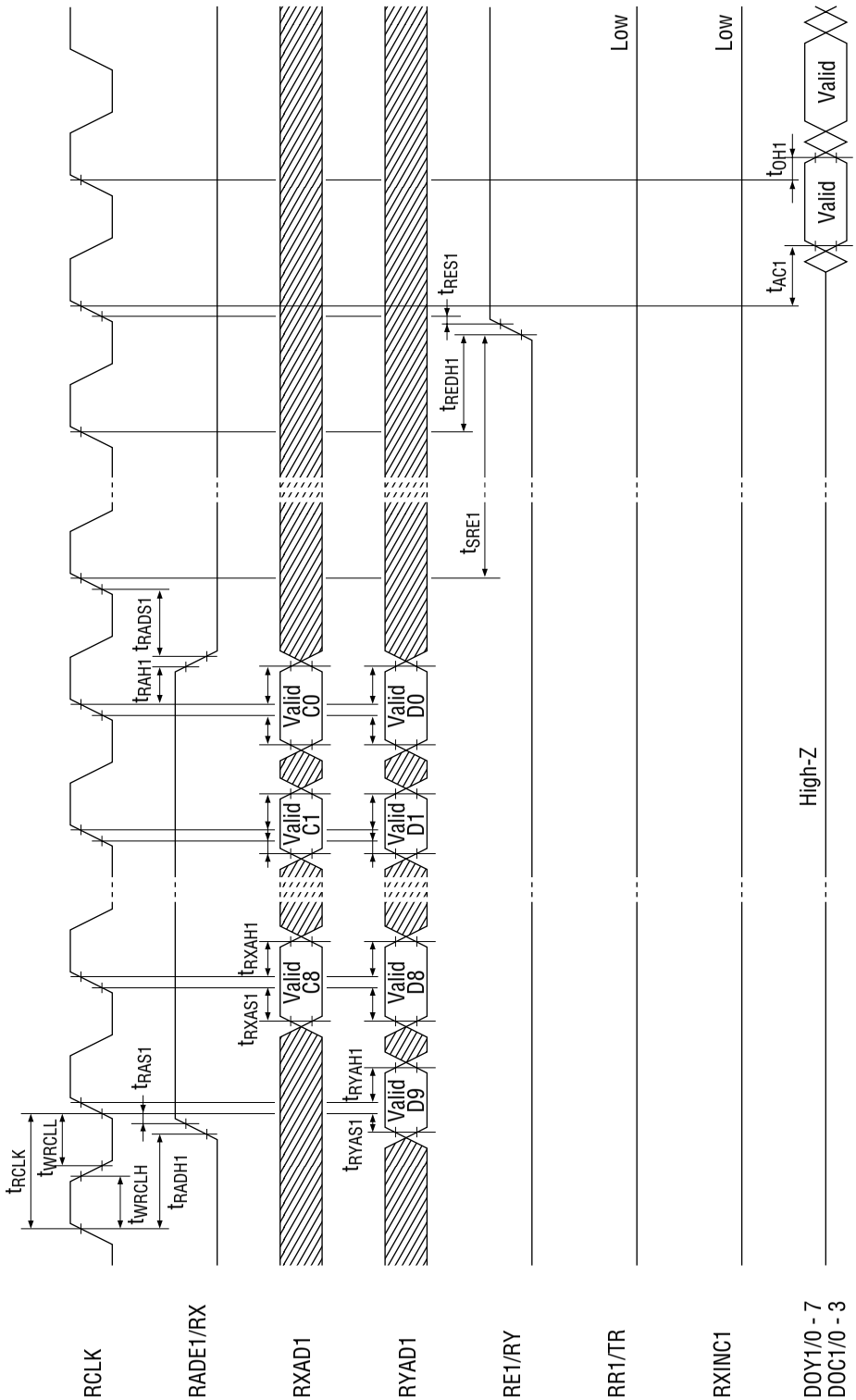
Note : In the IE = "L" cycle, the write address pointer is incremented, though no DIN data is written and the memory data is held.

Write Cycle (Write Transfer)

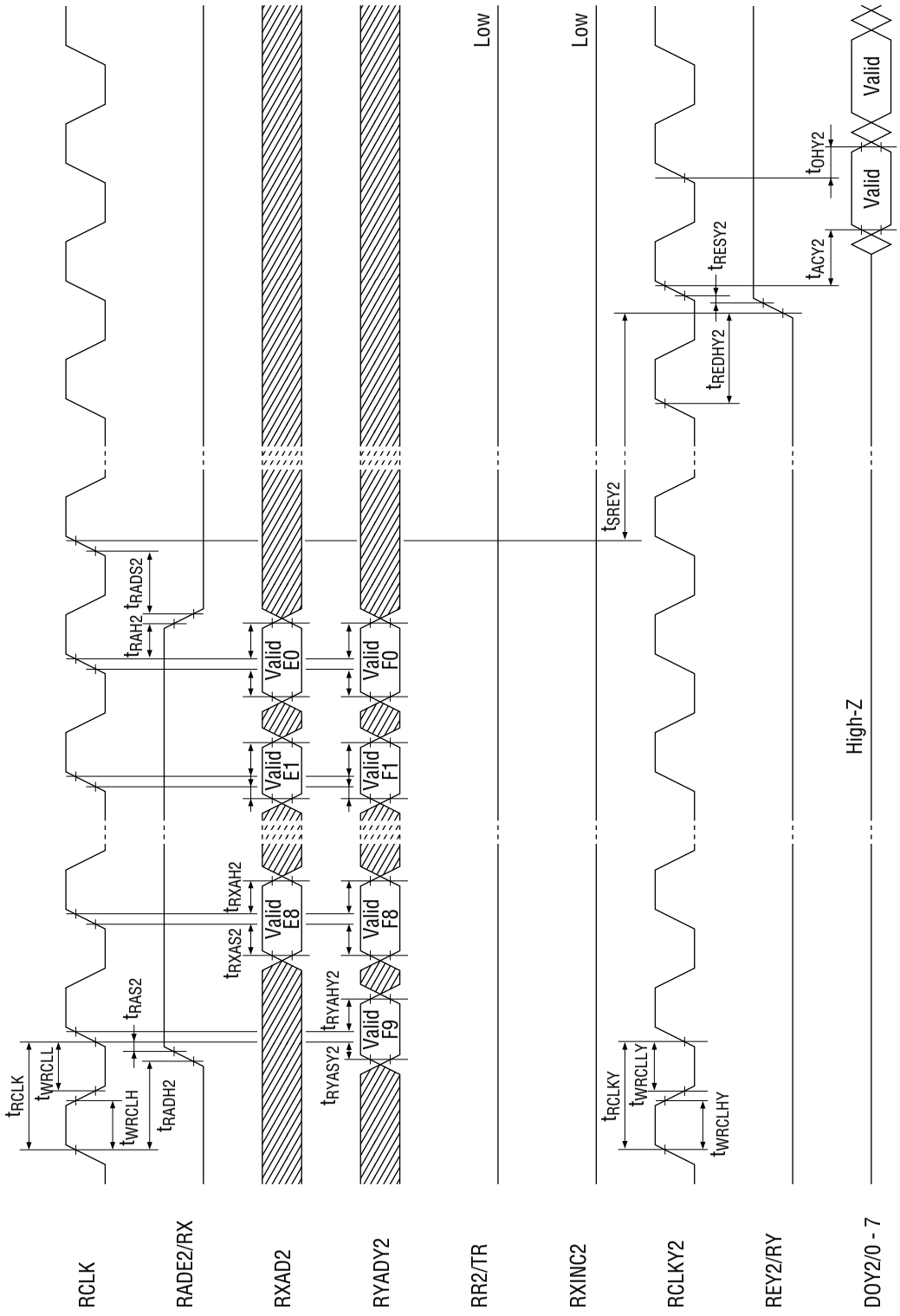


Note : When finishing the write operation on a line, be sure to perform a write transfer operation because the write data on the line is stored in the memory cell.

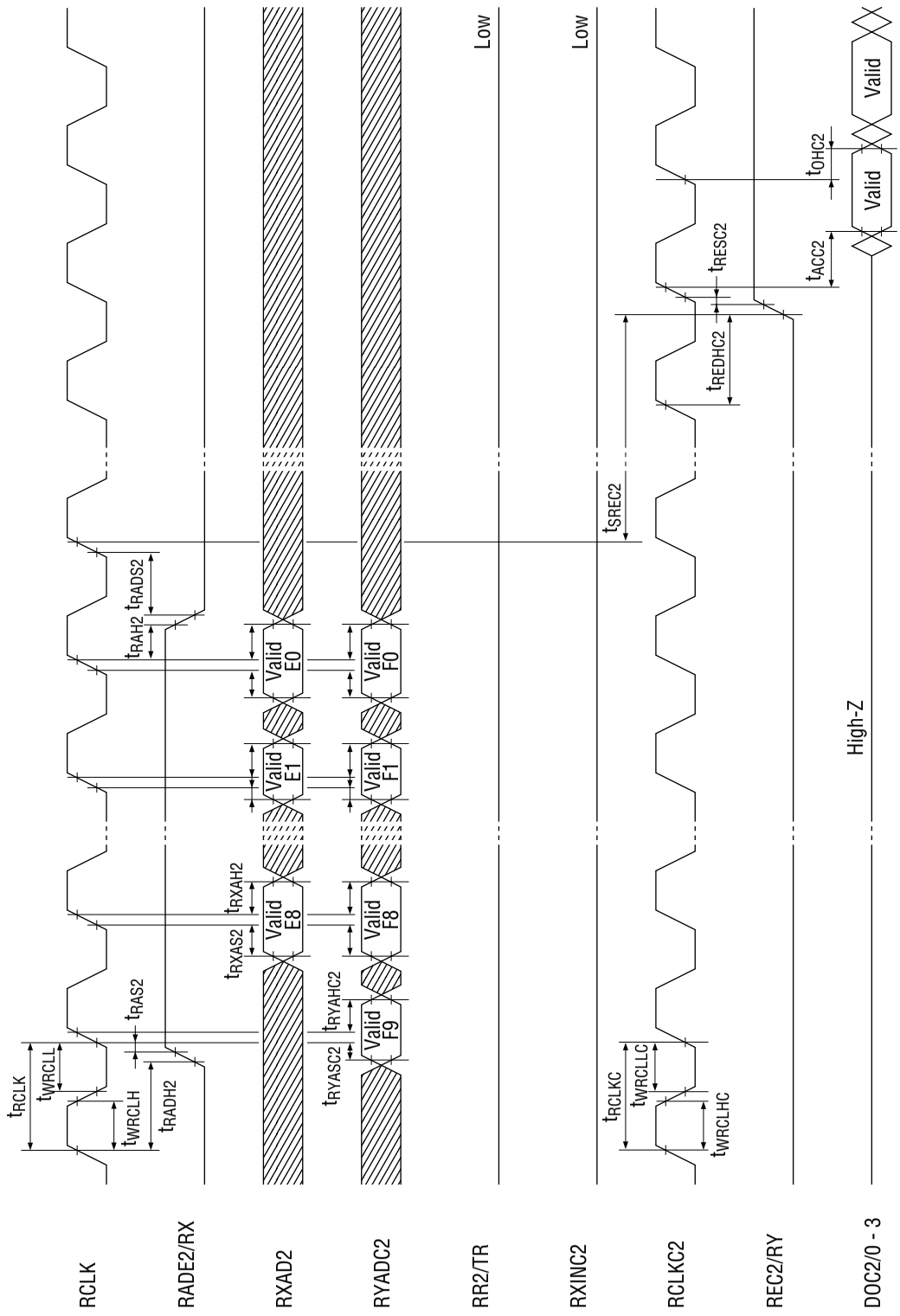
Read Cycle (Y1, C1) (Address Setting Cycle)



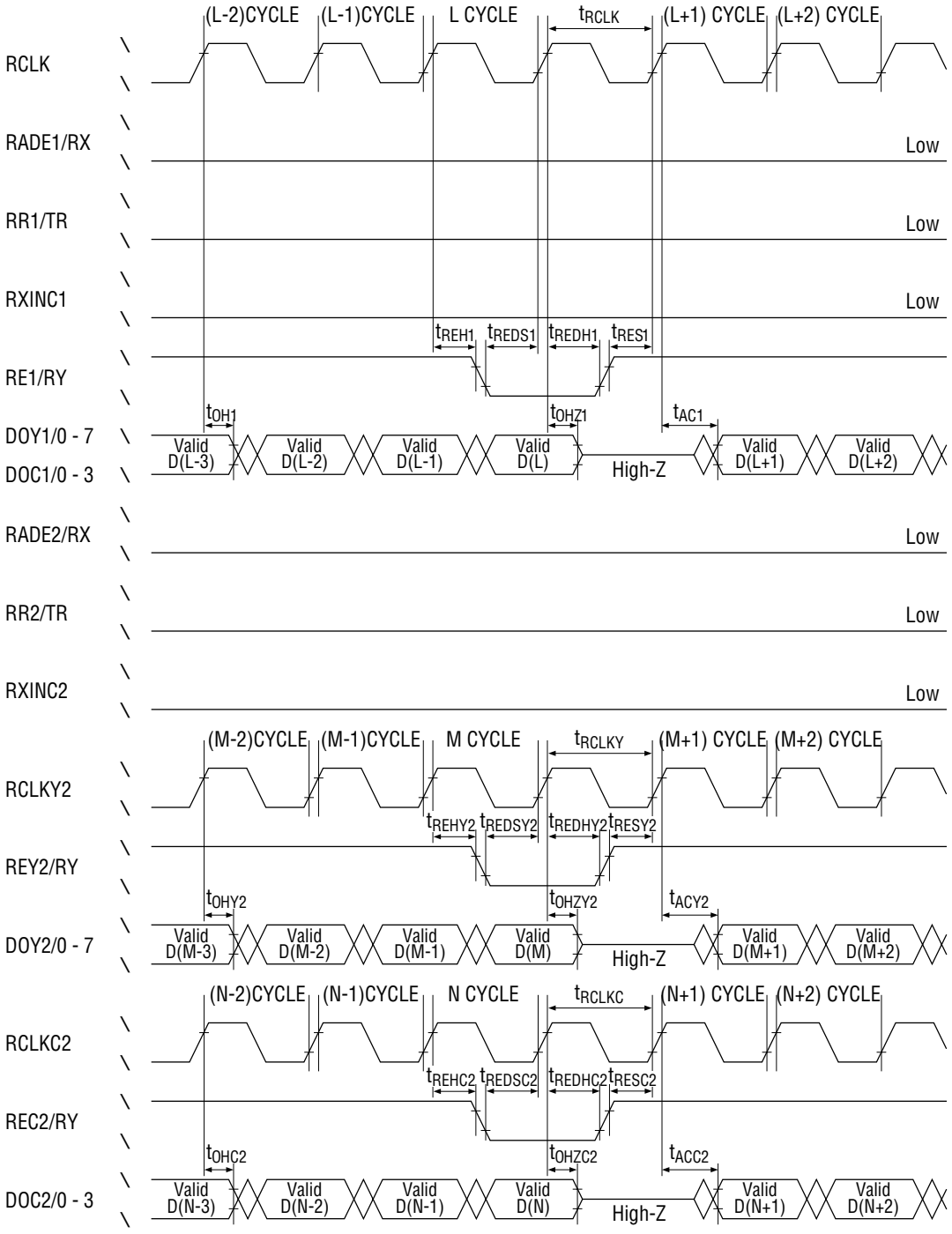
Read Cycle (Y2) (Address Setting Cycle)



Read Cycle (C2) (Address Setting Cycle)

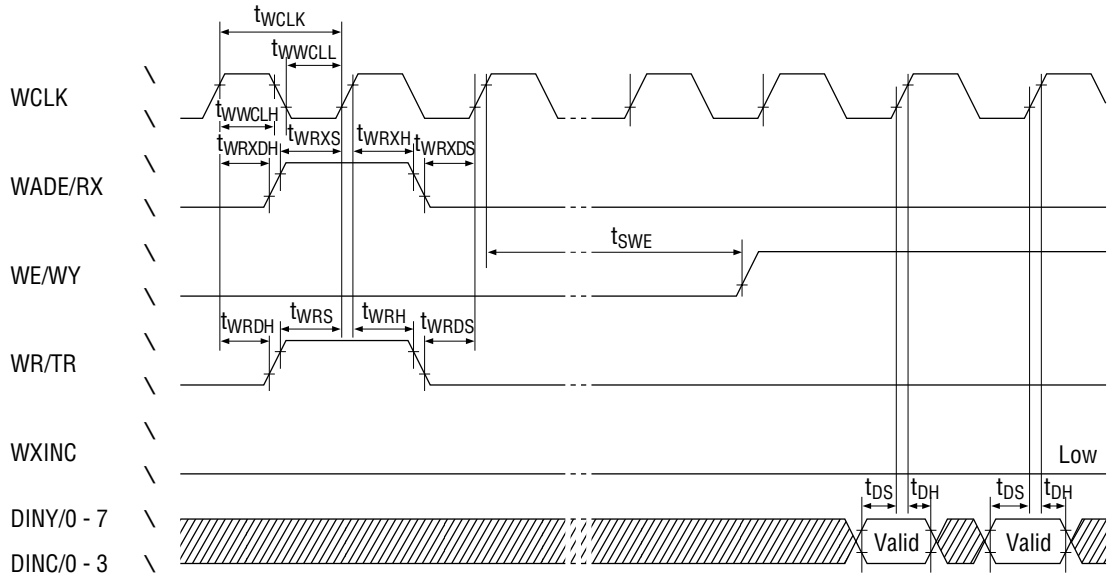


Read Cycle (RE Control)



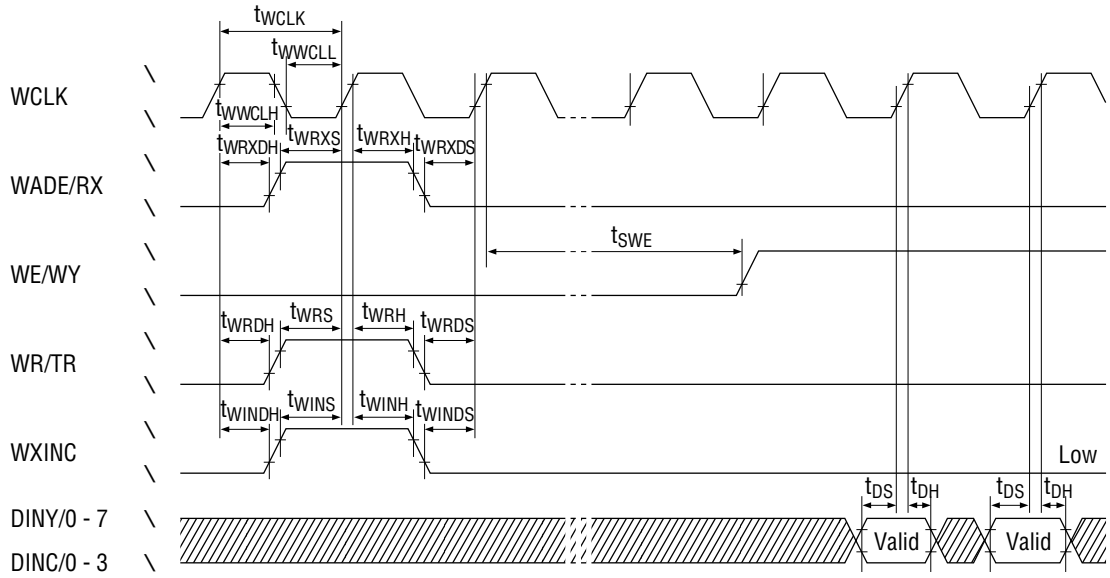
Note : In the cycle in which RE1/RY = "L", REY2/RY = "L", or REC2/RY = "L", the read address pointer is not incremented and the output enters the high impedance state.
The signals RE1/RY, REY2/RY, and REC2/RY can be operated independently.

Write Reset (1) Mode



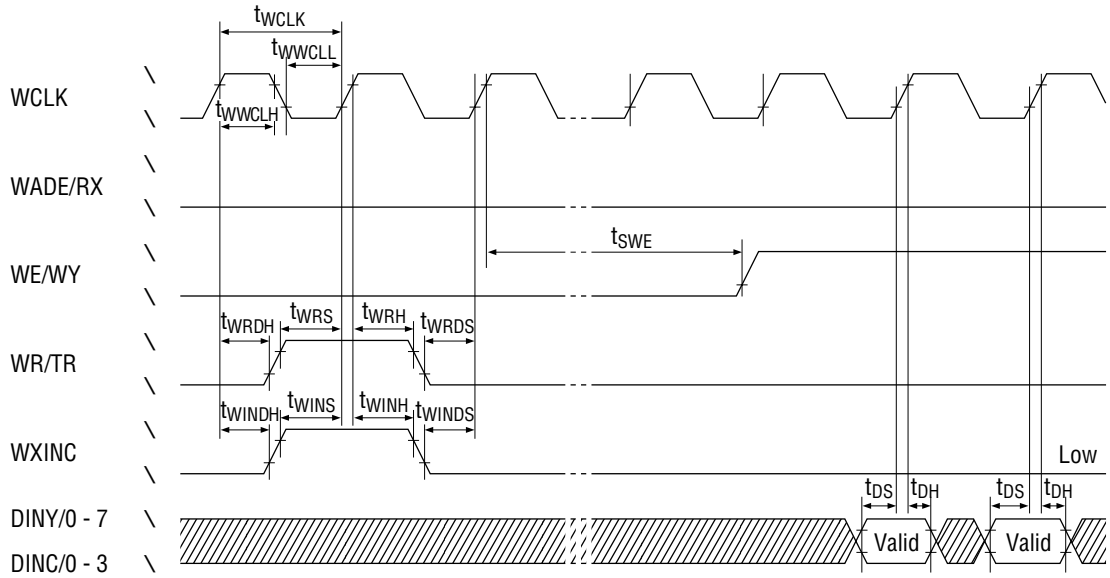
Note : Both the line address and word address are reset to 0.

Write Reset (2) Mode



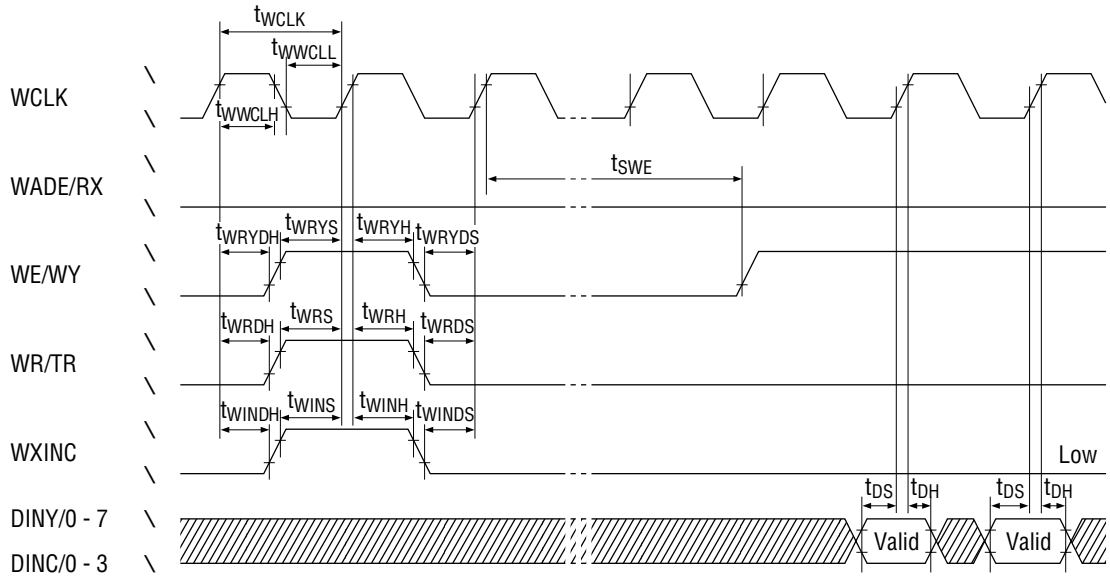
Note : Both the line address and word address are reset to 0. However, since the internal address register is also reset to 0, the initialized address data is cleared.

Write Line Increment (1) Mode



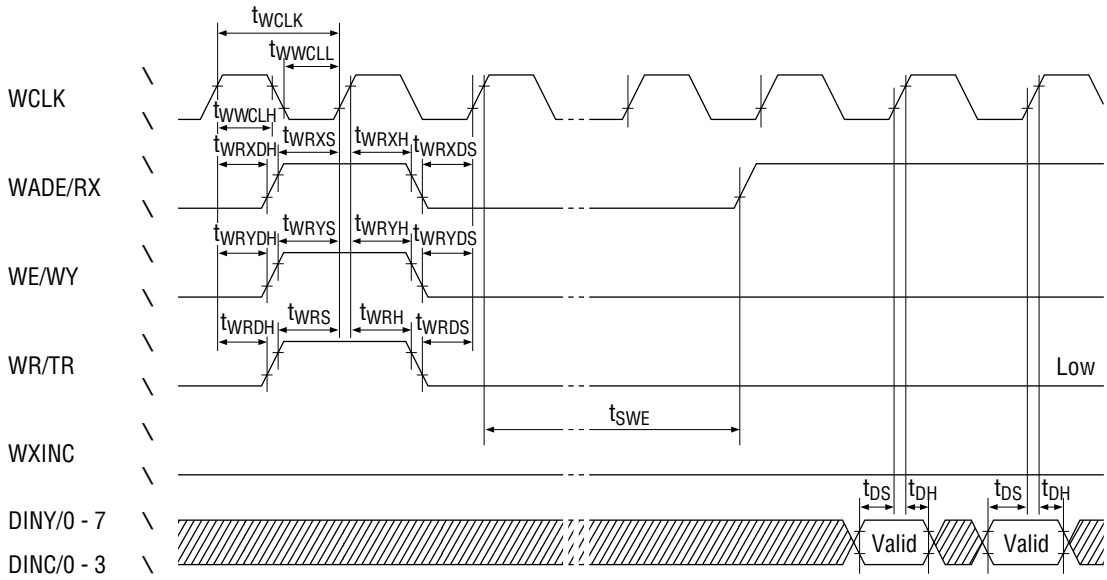
Note : The line address is incremented by 1 and the word address is reset to 0.

Write Line Increment (2) Mode



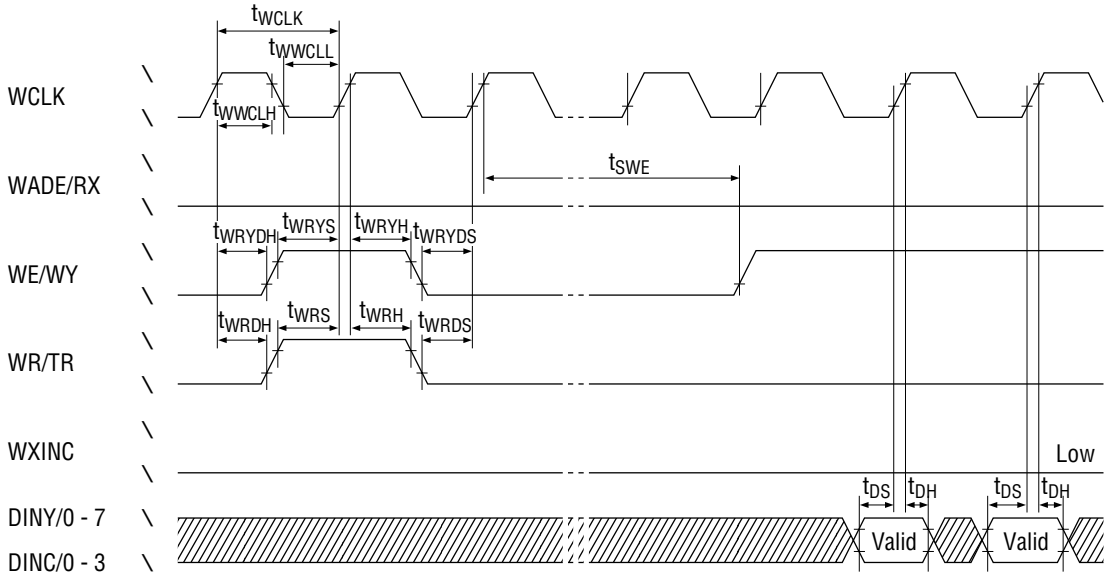
Note : The line address is incremented by 1 and the word address is reset to the initialized address.

Write Reset (3) Mode



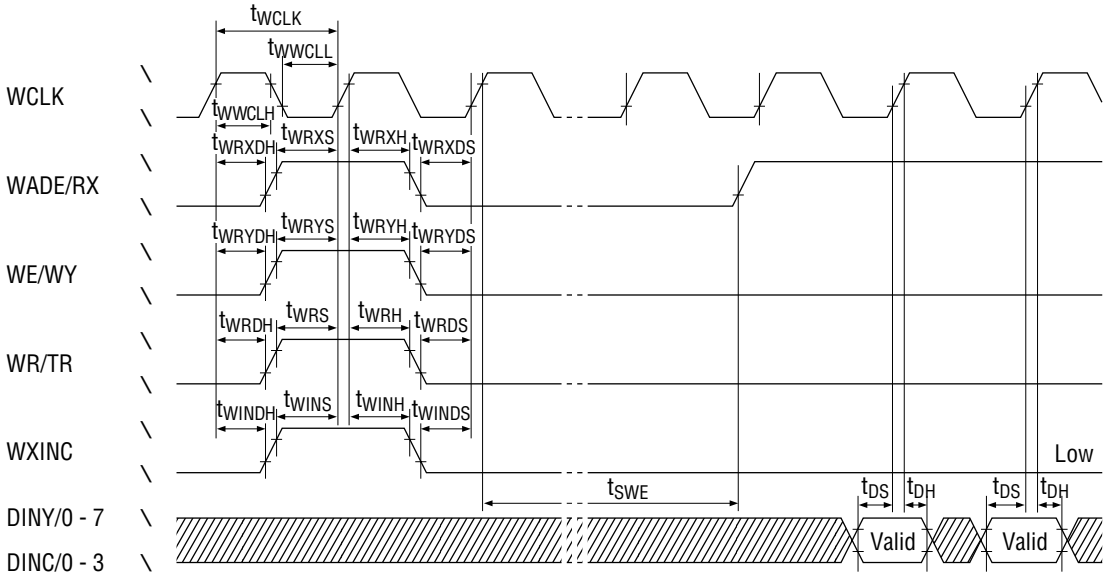
Note : The line address is reset to 0 and the word address is reset to the initialized address.

Write Line Hold (2) Mode



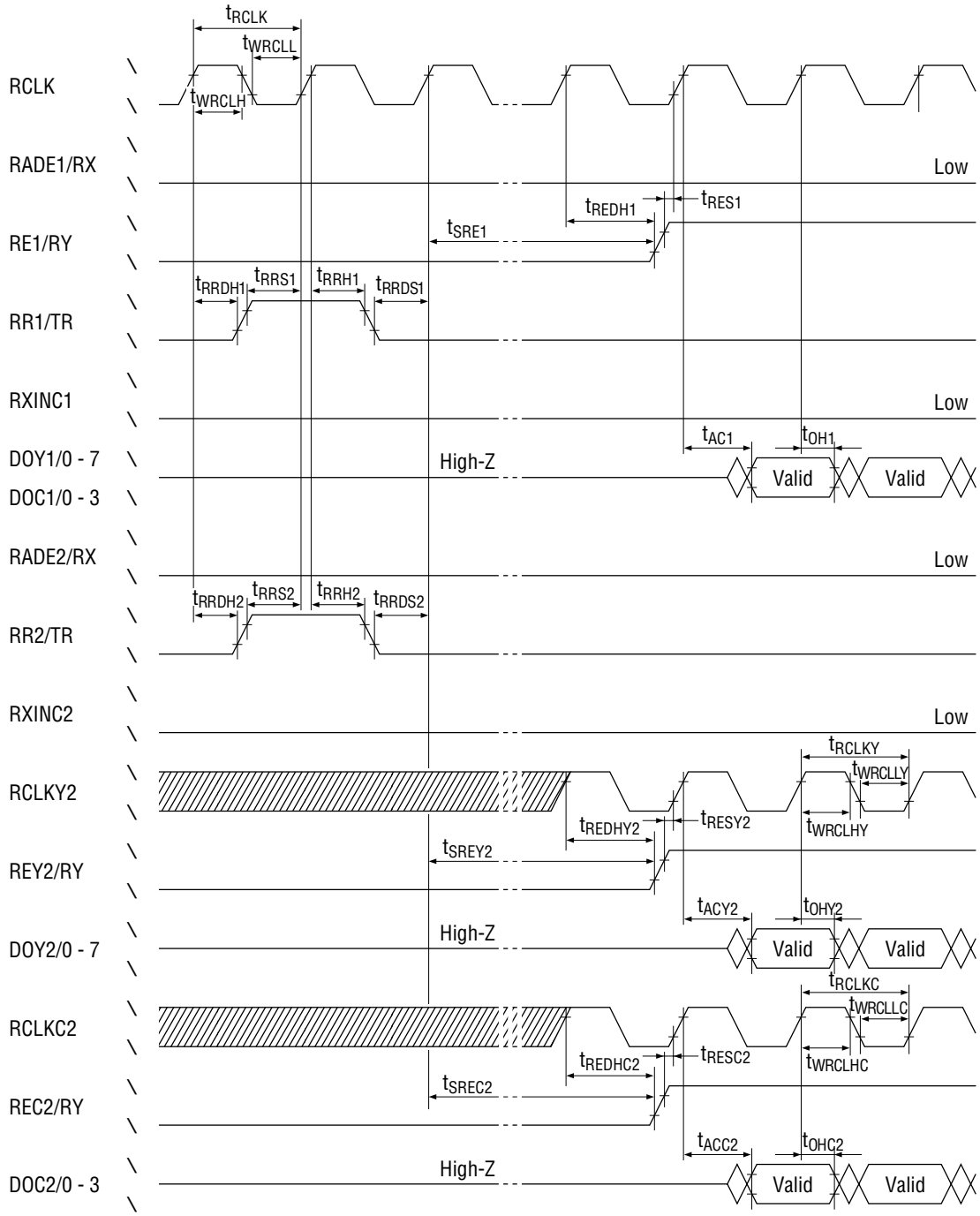
Note : The line address is held and the word address is reset to the initialized address.

Write Address Jump Mode



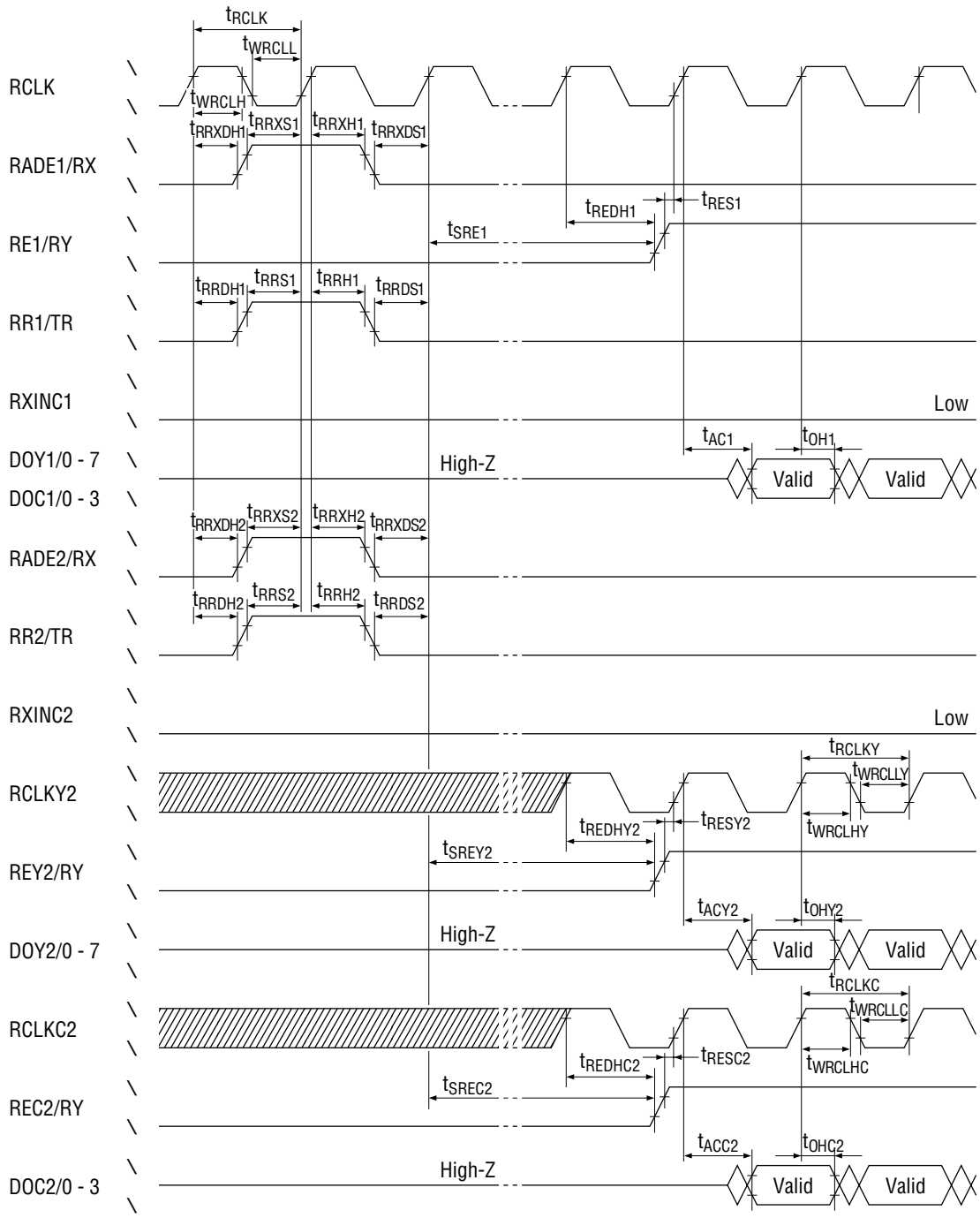
Note : Both the line address and word address are reset to the initialized addresses.

Read Line Hold (1) Mode



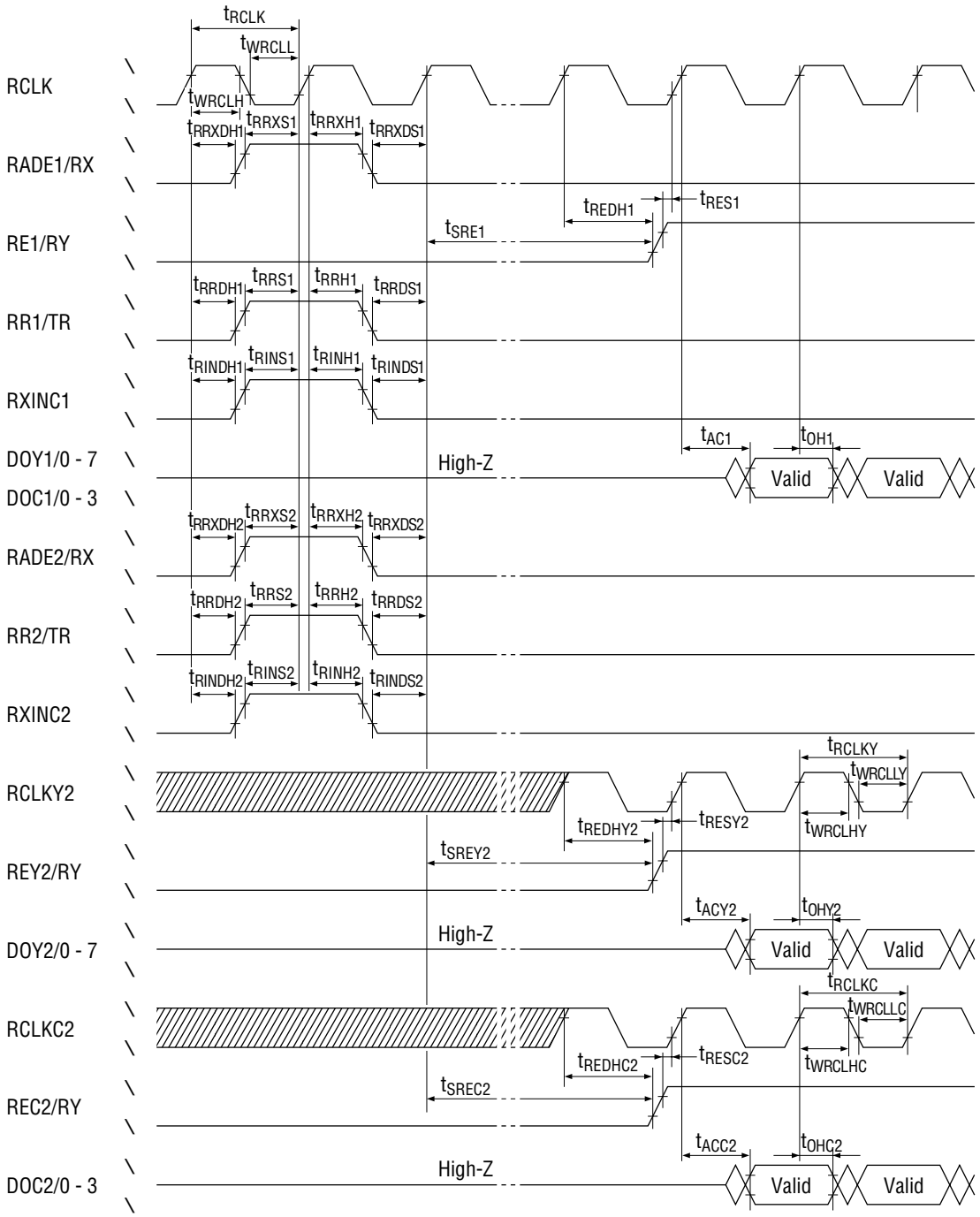
Note : The line address is held and the word address is reset to 0.

Read Reset (1) Mode



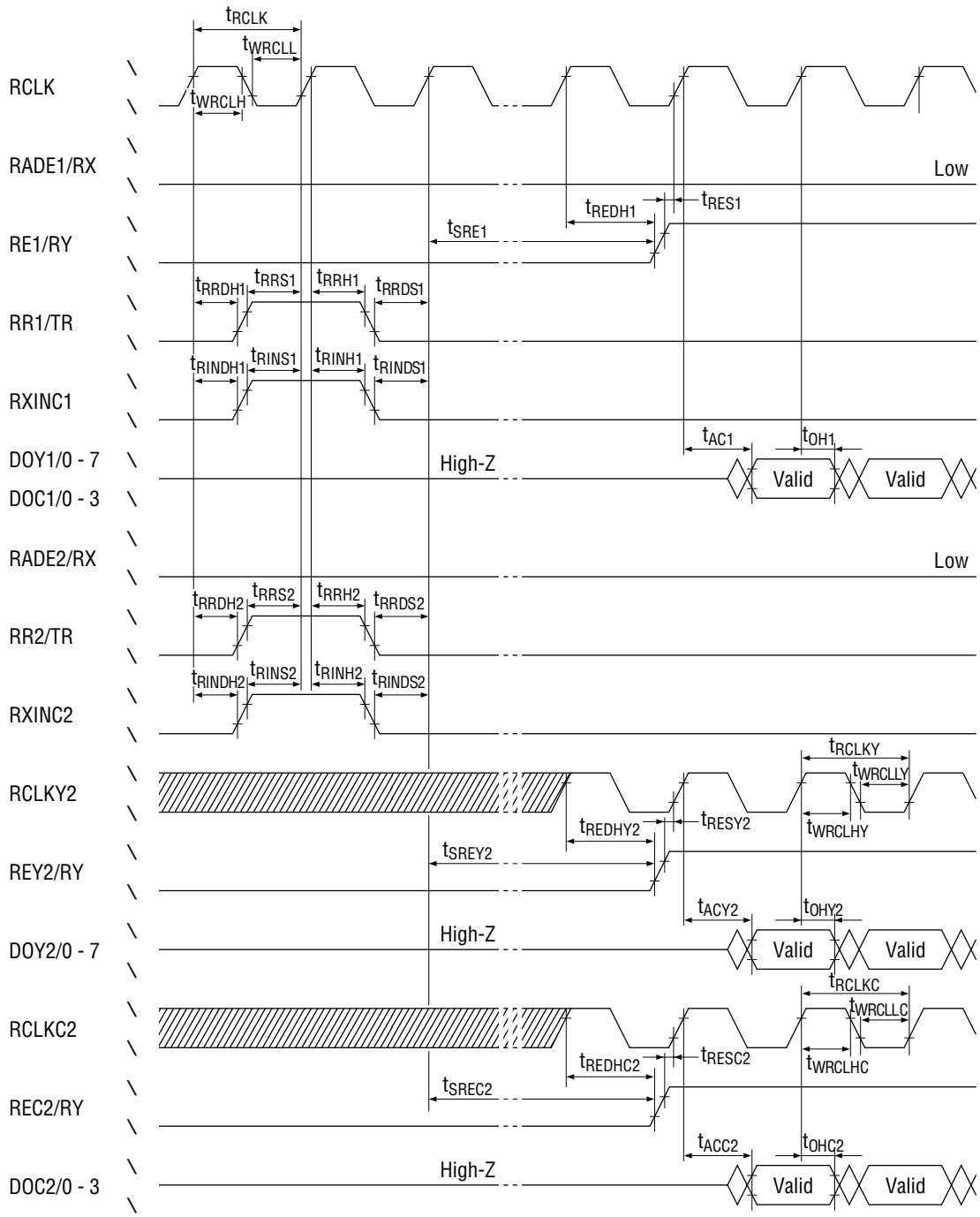
Note : Both the line address and word address are reset to 0.

Read Reset (2) Mode



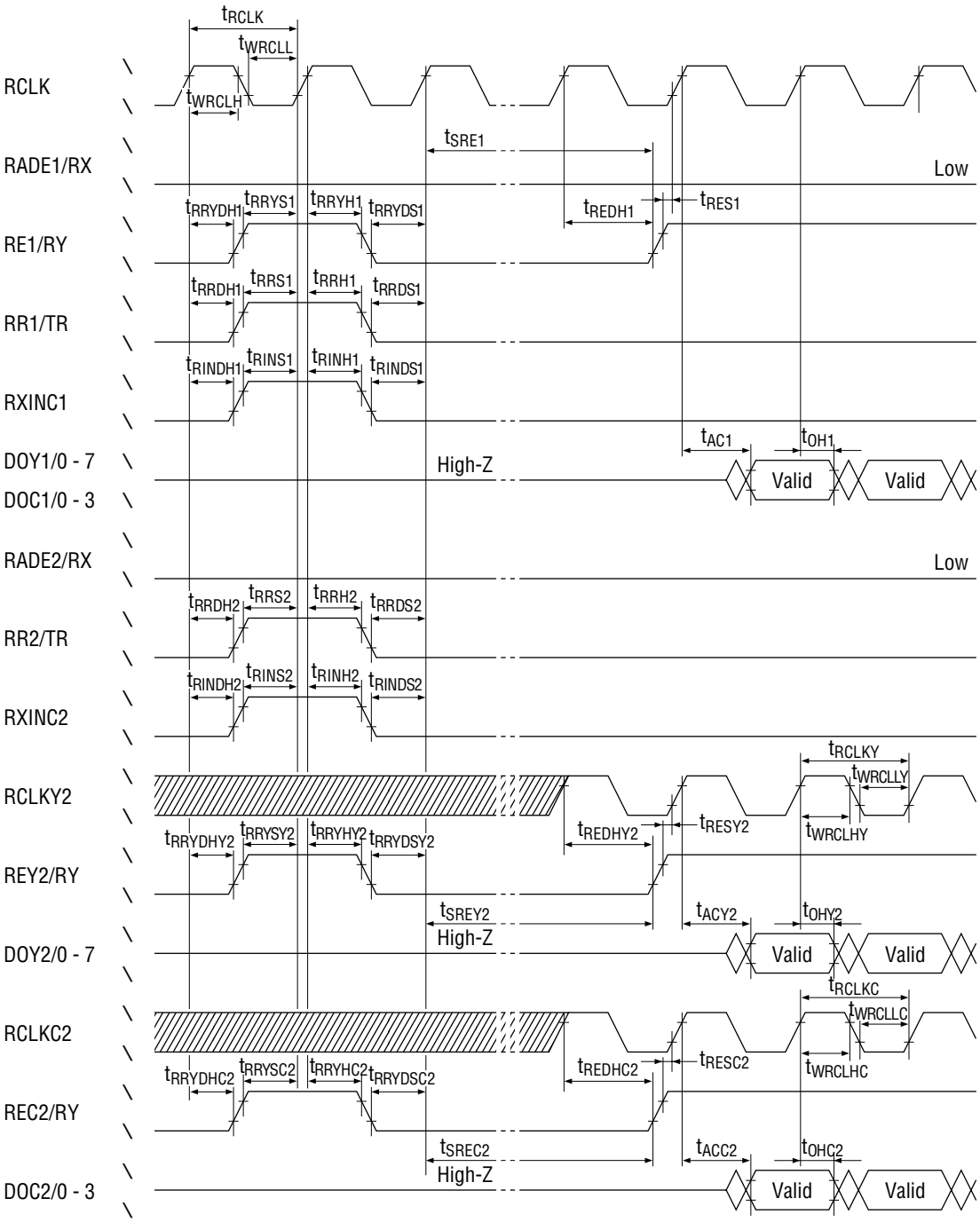
Note : Both the line address and word address are reset to 0. However, since the internal address register is also reset to 0, the initialized address data is cleared.

Read Line Increment (1) Mode



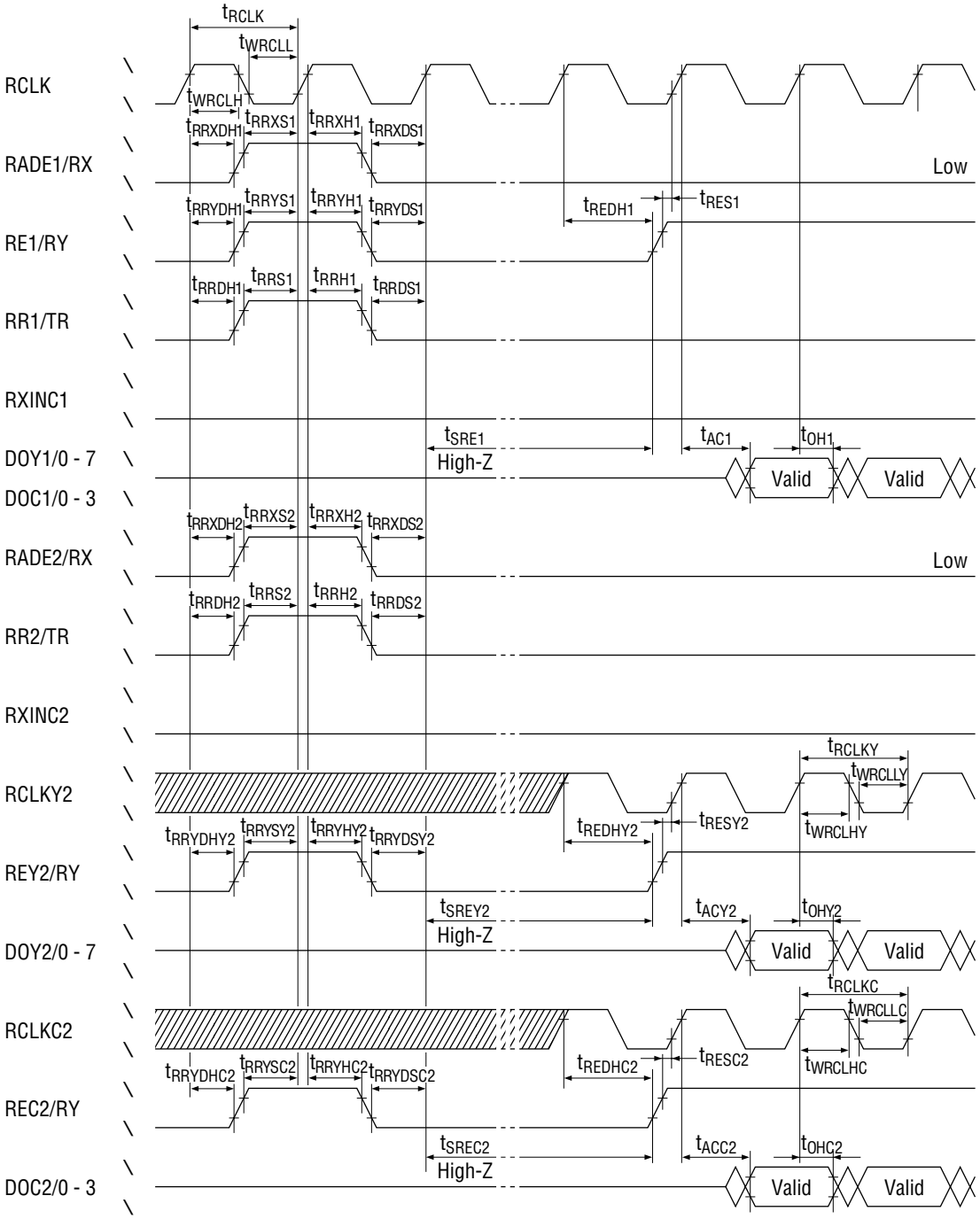
Note : The line address is incremented by 1 and the word address is reset to 0.

Read Line Increment (2) Mode



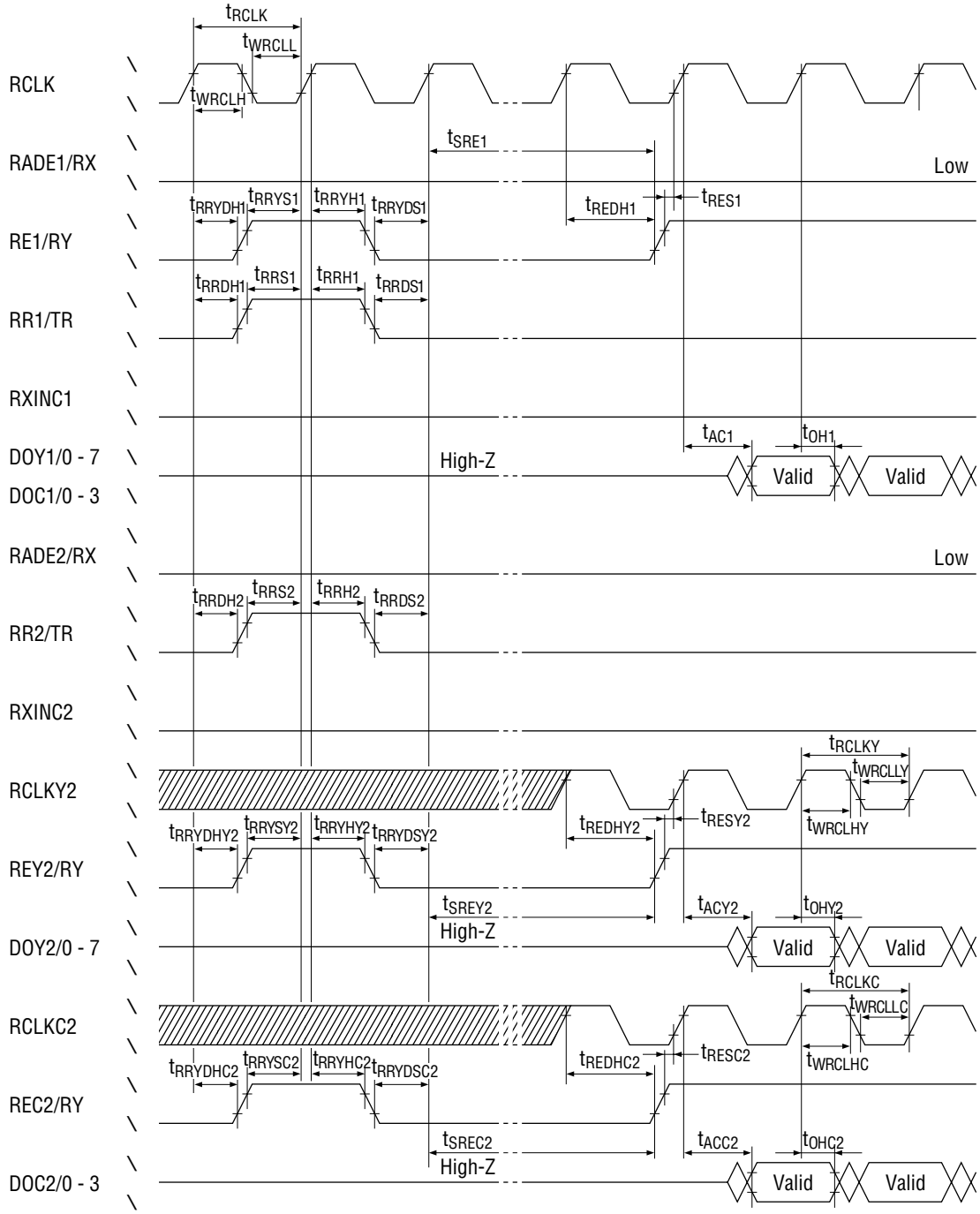
Note : The line address is incremented by 1 and the word address is reset to the initialized address.

Read Reset (3) Mode



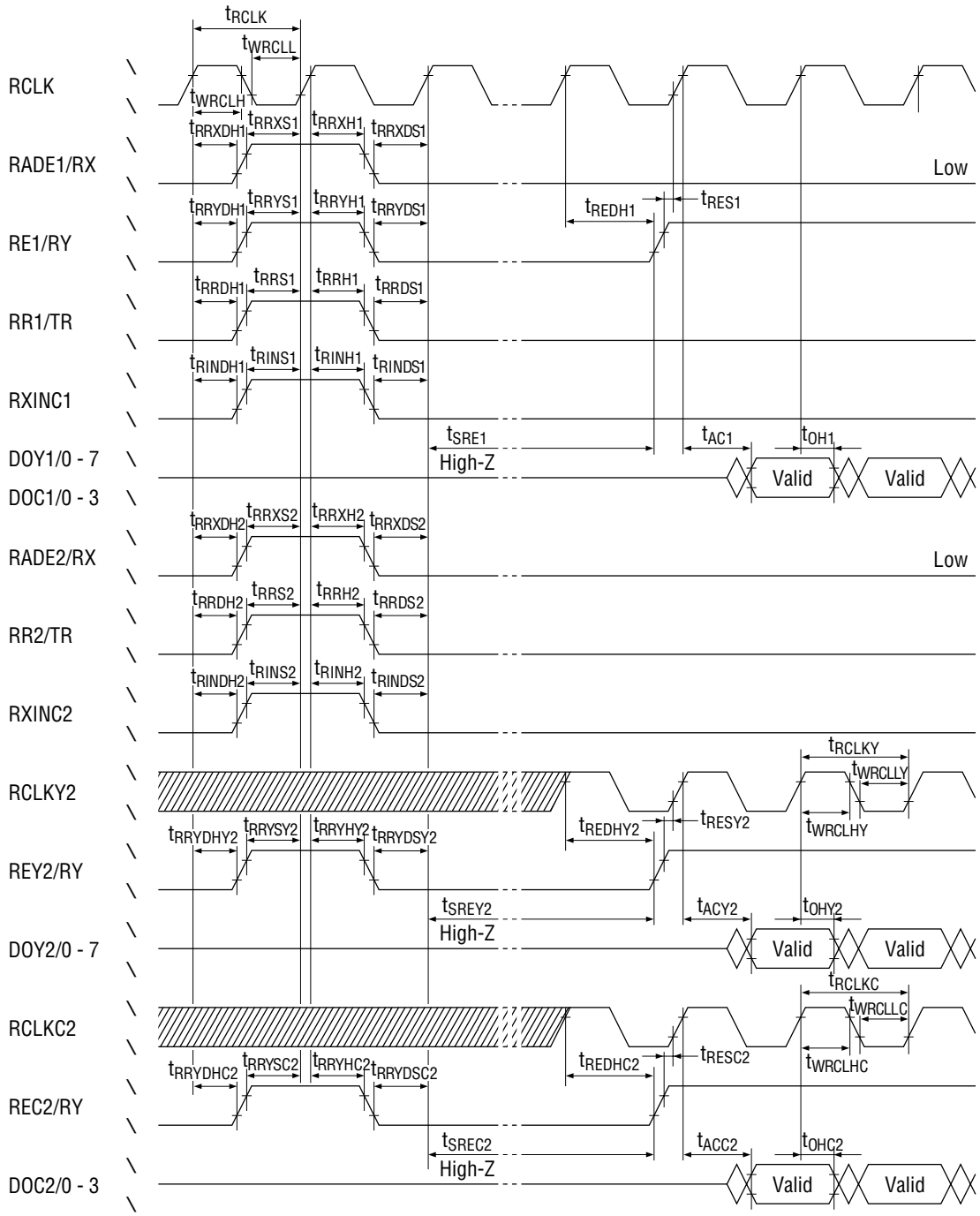
Note : The line address is reset to 0 and the word address is reset to the initialized address.

Read Line Hold (2) Mode



Note : The line address is held and the word address is reset to the initialized address.

Read Address Jump Mode

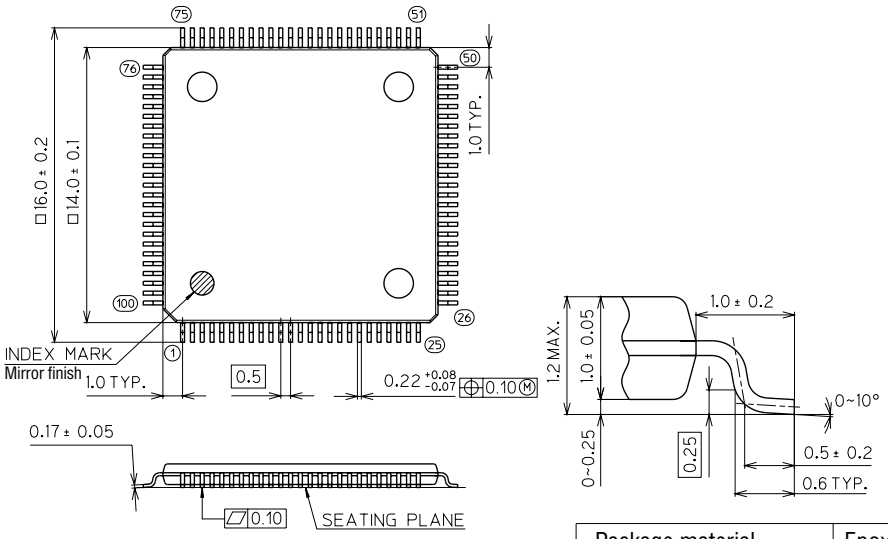


Note : Both the line address and word address are reset to the initialized addresses.

PACKAGE DIMENSIONS

(Unit : mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.55 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).