MX•COM, INC.
COMMUNICATION SEMICONDUCTORS

MX803A

DATA BULLETIN

Audio Signaling Processor

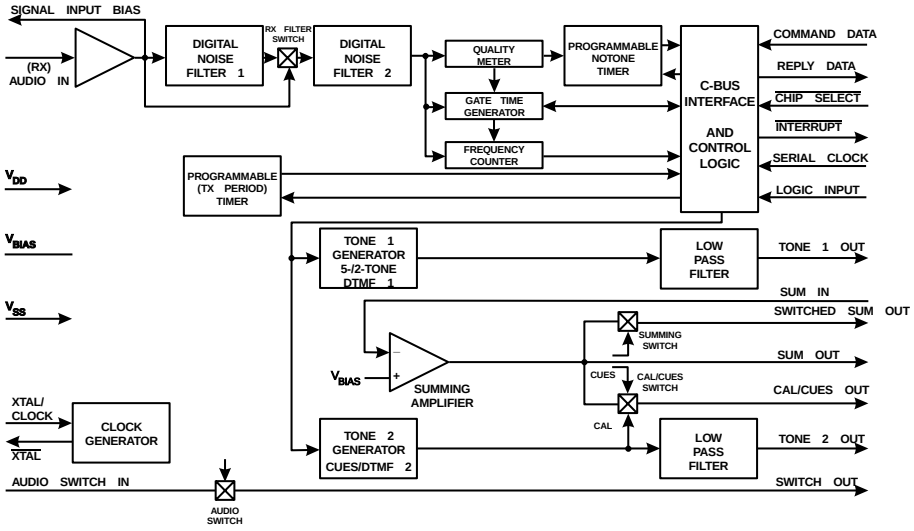
PRELIMINARY INFORMATION

Features

- **Full Duplex Audio Signaling Processor**
- **Single Tone**
- **Selective Call systems**
- **Tone Decoder with programmable NOTONE timer.**
- **Two Individual tone encoders and a programmable TX Period Timer.**
- **Low Power CMOS Device**
- **On-Chip programmable amplifier.**
- **C-BUS Compatible**

Applications

- **Signaling Systems supported**
- **SelCall (CCIR, EEA, ZVEI I / II /III)**
  2-Tone SelCall
  DTMF Encode
- **Inband Tone Signaling capability for LMR and other Radio Systems.**



The MX803A is an audio signaling processor that provides inband tone signaling capabilities for LMR and other Radio systems. A low-power CMOS device, the MX803A is a member of the DBS800 (Digitally integrated Baseband Sub-system) IC family (See section 4.2). Supported Signaling systems include SelCall (CCIR, EEA, ZVEI I, II, and III) 2-Tone SelCall and DTMF encode. The use of a non-predictive decoder and a versatile encoder, allows the MX803A to operate in any standard or non-standard tone system.

The MX803A is a full-duplex device for use with Single Tone or Selective Call systems. The MX803A consists of a tone decoder with a programmable NOTONE timer, two individual tone encoders and a programmable TX period timer, and an on-chip summing amplifier. Under the control of a µC, the MX803A will simultaneously encode and transmit 1 or 2 audio tones in the 208-3000Hz range, as well as detect, decode, and indicate the frequency of any non-predicted input tone in the frequency range of 313 to 6000Hz.

The MX803A is available in 24-pin PDIP (MX803AP), 24-pin PLCC (MX803ALH), and 24-pin SOIC (MX803ADW) packages.

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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

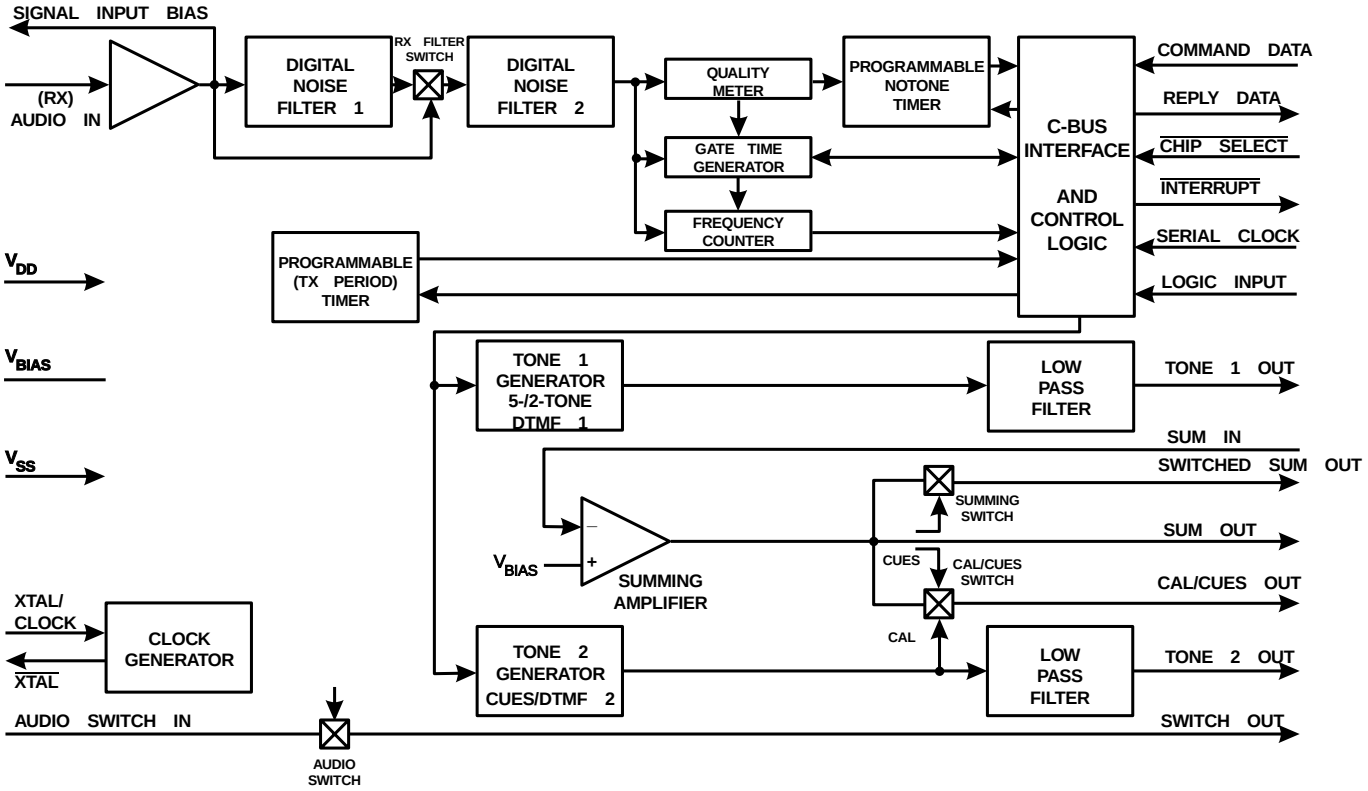


Figure 1: Block Diagram

2. Signal List

Pin No.	Name	Type	Description
1	$\overline{XTAL}$	Output	Output of the on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2.
2	Xtal/Clock	Input	Input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2.
3	Reply Data	Output	C-BUS serial data output to the µC. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the µC. See Figure 8 and Figure 9.
4	$\overline{CS}$	Input	C-BUS data loading control function. This input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the chip select signal. See Figure 8 and Figure 9.
5	Command Data	Input	C-BUS serial data input from the µC. Data is loaded to this device in 8-bit bytes, MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock. See Figure 8 and Figure 9.
6	Logic Input	Input	This "real-time" input is available as a general purpose logic input port which can be read from the Status Register. See Table 5. G/Purpose Timer Period Expired NOTONE Timer Period Expired RX Tone Measurement Complete These interrupts are inactive during relevant powersave conditions and can be disabled by bits 5 and 6 in the Control Register.
7	$\overline{IRQ}$	Output	Output of this pin indicates an interrupt condition to the µC by going to a logic "0." This is a "wire-or-able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The system IRQ line requires one pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register and are shown below:
10	Audio Switch In	Input	Input to the stand-alone on-chip Audio Switch. This function is enabled/disabled by Bit 7 of the Control Register
11	Audio Switch Out	Output	Output of the stand-alone on-chip Audio Switch..
12	V_{SS}	Power	Negative supply (GND).
13	Rx Audio In	Input	Received audio tone signaling input. This input must be ac coupled and connected, using external components, to the Signal Input Bias pin. See Figure 2.
14	Signal Input Bias	Input	External components are required between this input and the RX Audio In pin. See Figure 2.
15	V_{BIAS}	Output	Internal circuitry bias signal, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C2. See Figure 2..
16	Tone 1 Out	Output	Tone 1 Generator (2-/5-tone Selcall or DTMF 1) output. External gain and coupling components are required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to the TX Tone Generator 1 Register (Table 7). See Figure 2.
17	Tone 2 Out	Output	Tone 2 Generator (2-/5-tone Selcall, CUES or DTMF 2) output. External gain and coupling components are required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to the TX Tone Generator 2 Register (Table 7). See Figure 2.

Pin No.	Name	Type	Description
18	CAL/CUES Out	Output	An auxiliary, selectable tone frequency output, providing a square wave CALibration signal from the Tone 2 Generator or a sine wave CUES (beep) signal from the Summing Amplifier. The output mode (CAL or CUES) is selected by Bit 14 in the TX Tone Generator 2 Register (Table 7). When Tone Generator 2 is set to Notone, the CAL input is pulled to V_{BIAS}; during a powersave of Tone Generator 2 it is held at V_{SS}.
19	Sum in	Input	Input to the on-chip Summing Amplifier. This amplifier is available for combining Tone 1 and Tone 2 outputs (DTMF). Gain and coupling components should be used at this input to provide the required system gains. See Figure 2 and Figure 3
20	Sum Out	Output	Output of the on-chip summing amplifier. Combined tones (1 and 2) are available at this output. See Figure 2 and Figure 3.
21	Switched Sum Out	Output	This is the combined tone output available for transmitter modulation. The switch allows control of the MX803A output. Control of this switch is by Bit 4 of the Control Register. See Figure 2 and Figure 3.
23	Serial Clock	Input	C-BUS serial clock input. This clock, produced by the µC, is used for transfer timing of commands and data to and from the MX803A. See Figure 8 and Figure 9.
24	V_{DD}	Power	Positive supply. A single +5 volt power supply is required. Levels and voltages within this Audio Signaling Processor are dependent upon this supply..
8, 9, 22	N/C		No Internal Connection. These pins may be connected to V_{SS} to improve screening and reduce noise levels around the MX803A.

Table 1: Signal List

3. External Components

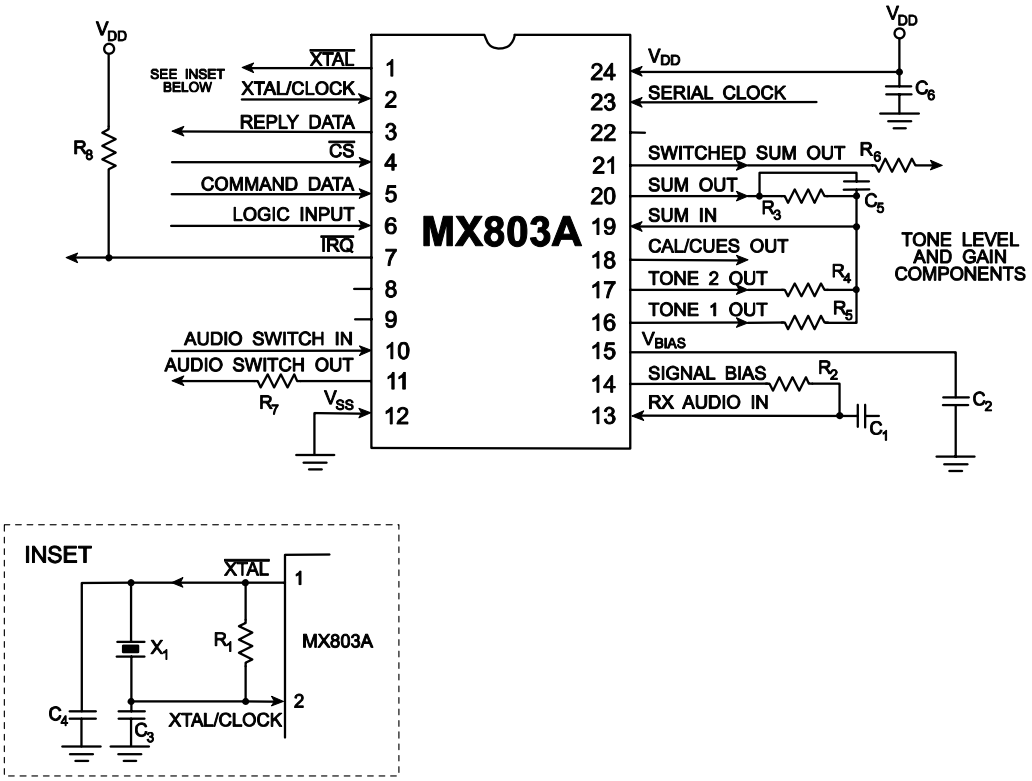


Figure 2: Recommended External Components

R1		1.0MΩ	±10%
R2		2.0MΩ	±10%
R3	Note 2, 3	100kΩ	±10%
R4	Note 2, 3	82.0kΩ	±10%
R5	Note 2, 3	122kΩ	±10%
R6	Note 2	100kΩ	±10%
R7	Note 2, 5	100kΩ	±10%
R8		22.0kΩ	

C1		0.1µF	±20%
C2		1.0µF	±20%
C3	Note 4	33.0pF	±20%
C4	Note 4	33.0pF	±20%
C5	Note 3	22.0pF	±20%
C6		1.0µF	±20%
X1	Note 1, 4	4.00MHz	

Table 2: Recommended External Components

Notes:

1. Xtal/clock components described are recommended in accordance with MX-COM's Application Note on Standard and DBS 800 Crystal Oscillator Circuits (April 1990). For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. System Components whose values are calculated to allow the MX803A to operate with other DBS 800 microcircuits. Figure 3 shows these components used in the system signal paths.
3. R3, R4, R5 and C5 are tone mixing components calculated to provide a 3dB tone differential (twist) for use in a DTMF configuration. Single tone output levels are set independently.
4. When X1 > 5.00MHz, C3 = C4 = 18pF
5. R7 provides modulation level and matching outputs for the MX803A.

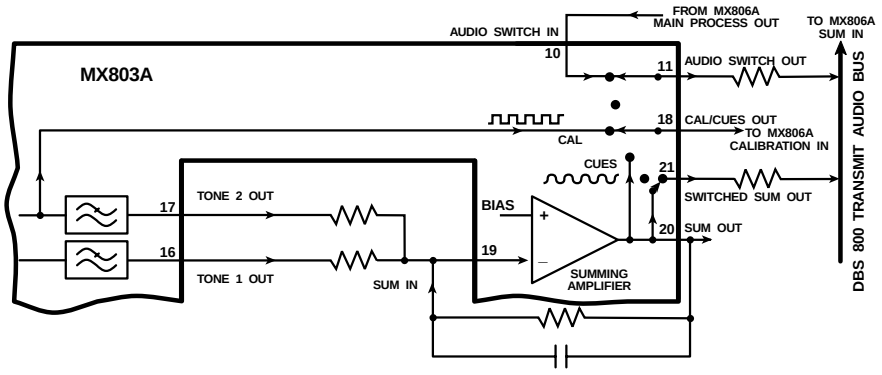


Figure 3: Example of Signal Switching in a DBS800 microcircuit

4. General Description

4.1 DESCRIPTION

The MX803A is an audio signaling processor that provides inband tone signaling capabilities for LMR and other Radio systems. A low-power CMOS device, the MX803A is a member of the DBS800 (Digitally integrated Baseband Sub-system) IC family (See section 4.2). Supported Signaling systems include SelCall (CCIR, EEA, ZVEI I, II, and III) 2-Tone SelCall and DTMF encode. The use of a non-predictive decoder and a versatile encoder, allows the MX803A to operate in any standard or non-standard tone system.

The MX803A is a full-duplex device for use with Single Tone or Selective Call systems. The MX803A consists of a tone decoder with a programmable NOTONE timer, two individual tone encoders and a programmable TX period timer, and an on-chip summing amplifier. Under the control of a µC, the MX803A will simultaneously encode and transmit 1 or 2 audio tones in the 208-3000Hz range, as well as detect, decode, and indicate the frequency of any non-predicted input tone in the frequency range of 313 to 6000Hz.

A general purpose logic input, interfacing directly with the Status Register, is provided. This may be used as an auxiliary method of routing digital information to the µC via C-BUS. Output frequencies are produced from data loaded to the MX803A. A programmable, general purpose, on-chip timer sets the tone transmit periods. A Dual-Tone Multi-Frequency (DTMF) output is obtained by combining the 2 independent output frequencies in the integral summing amplifier. This process can also be used for level correction.

Tones produced by the MX803A can be used in the system as modulation calibration inputs and as “CUE” audio indications to the operator. Received tones are measured and their frequency indicated to the µC in the form of a received data word. A poor quality or incoherent tone will indicate Notone.

4.2 DBS800 Systems

The Digitally-Integrated Baseband Subsystem (DBS800) is a family of low power ICs which provide a comprehensive range of audio processing and signaling functions for use within LMR and other Radio Systems. Each DBS800 IC may be used as part of a complete audio system, or each IC may operate as a stand alone. The system and ICs are partitioned in such a way that radio designers can easily select the device or devices appropriate to their needs.

The DBS800 family consists of the following ICs:

4.2.1 MX802 DVSR Codec

This is a full-duplex CVSD speech encoder/decoder with the ability to store and retrieve data within attached DRAM (Dynamic Random Access Memory) using an on-chip DRAM controller. The MX802 also provides on-chip input and output audio filtering.

4.2.2 MX803A Audio Signaling Processor

This provides an inband tone signaling ability to LMR and other Radio Systems.

4.2.3 MX805A Sub-Audio Signaling Processor

This provides a sub-audio and digital signaling (NRZ) ability to LMR and other Radio Systems.

4.2.4 MX806A Audio Processor

This is a half duplex audio processor providing all DBS800 system audio signal conditioning and filtering capabilities for the system transmit and receive paths.

4.2.5 MX809 MSK Modem

This is an intelligent, half-duplex 1200bps MSK/FFSK Modem with software programmable byte-synchronization system and checksum generation and checking.

4.2.6 MX812 VSR Codec

This is a half-duplex CVSD speech encoder/decoder with the ability to store and retrieve data within attached DRAM (Dynamic Random Access Memory) using an on-chip DRAM controller

4.3 C-BUS Control

C-BUS is the controlling hardware and software interface for all members of the DBS800 family. It enables the serial, bi-directional transfer of commands and data throughout the system, allowing total flexibility of operational control and data handling. System upgrades can be achieved by a simple software or firmware change.

The C-BUS physically consist of 5 lines. These lines are Serial Clock, Command Data, Reply Data, Chip Select ($\overline{CS}$), and Interrupt Request ($\overline{IRQ}$). A description of each may be found in section 2.

5. Application

Control of the MX803A Audio Signaling Processor's operation is by communication between the µC and the MX803A internal registers on the C-BUS using Address/Commands (A/Cs) and appended instructions or data. See Figure 8. The use and content of these instructions is detailed in the following sections.

For additional application information contact MX•COM, Inc.

5.1 MX803A Internal Registers

Control Register	30_H	Write only, control and configuration of the MX803A.
Status Register	31_H	Read only, reporting of device functions.
RX Tone Frequency Register	32_H	Read only, indicates frequency of the last received input.
RX Notone Timer	33_H	Write only, setting of the RX Notone period.
TX Tone Generator 1 Register	34_H	Write only, setting the required output frequency from TX Tone Generator 1.
TX Tone Generator 2 Register	35_H	Write only, setting the required output frequency from TX Tone Generator 2.
General Purpose Timer Register	36_H	Write only, setting of a general purpose sequential time period.

5.2 Address/Commands

The first byte of a loaded data sequence is always recognized by the C-BUS as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an A/C byte followed by further instruction/data or a status/data reply.
Instructions and data are loaded and transferred via C-BUS in accordance with the timing information given in Figure 8 and Figure 9. Table 3 shows the list of A/C bytes relevant to the MX803A.

Command Assignment	**Address/Command (A/C) Byte**		**Data Bytes**
	Hex	Binary	
		msb lsb	
General Reset	01	00000001	
Write to Control Register	30	00110000	+ 1 byte instruction to Control Register
Read Status Register	31	00110001	+ 1 byte reply from Status Register
Read RX Tone Frequency	32	00110010	+ 2 bytes reply from RX Tone Register
Write to Notone Timer	33	00110011	+ 1 byte instruction to Notone Register
Write to TX Tone Gen. 1	34	00110100	+ 2 bytes instruction to TX Tone Gen. 1
Write to TX Tone Gen. 2	35	00110101	+ 2 bytes instruction to TX Tone Gen. 2
Write to G/Purpose Timer	36	00110110	+ 1 byte instruction to G/Purpose Timer

Table 3: C-BUS Address/Commands

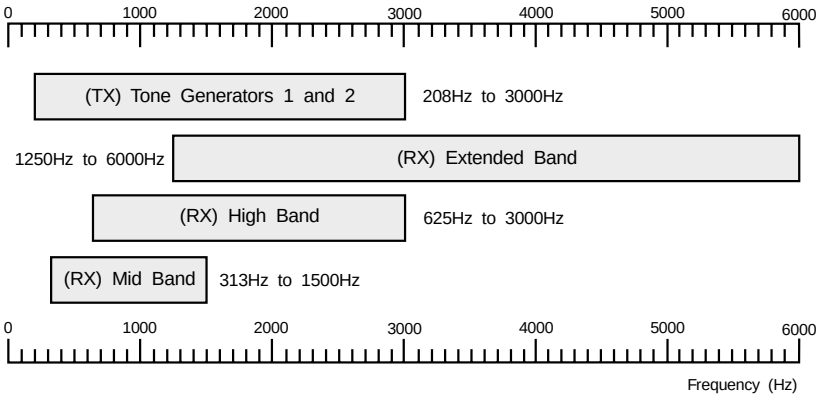


Figure 4: MX803A Frequencies

5.2.1 Write to Control Register

A/C 30_H, followed by 1 byte of Command Data

Audio Switch: Enables or Disables the stand-alone on-chip Audio Switch.

General Purpose Timer: This should be set up before interrupts are enabled since a General Reset command will set the timer period to 00_H - 0ms (permanent interrupt).

Interrupt Enable Instructions: Status bits 0, 1 and 2 are produced regardless of the state of these settings.

Band Selection: Bits 2 and 3 set the required frequency range. See Figure 4.

Summing Switch: Used to Enable or Disable the switch that controls the MX803A output.

Interrupt Designation: Decoder Interrupts

Notone Timer and RX Tone Measurement

Transmitter Interrupt

G/Purpose Timer Interrupt

Setting		Control Bits
MSB		**Transmitted First**
Bit 7		**Audio switch**
1		Enable
0		Disable
Bit 6		**G/Purpose Timer Interrupt**
1		Enable
0		Disable
Bit 5		**Decoder Interrupts**
1		Enable
0		Disable
Bit 4		**Summing Switch**
1		Enable
0		Disable
Bit 3	**Bit 2**	**Band Selection**
0	0	High Band
0	1	Mid Band
1	0	Extended Band
1	1	Do not use this setting
Bit 1		**Set to**
0		0
Bit 0		**Set to**
0		0

Table 4: Control Register

5.2.2 Read Status Register

A/C 31_H, followed by 1 byte of Reply Data

Interrupt Requests (IRQ): Interrupts on this device are available to draw the attention of the μC to a change in the condition of the bit in the status register. However, bits are set in the status register irrespective of the setting of interrupt enable bits (Table 4) and these changes may be recognized by polling the register.

General Purpose Timer Period: Set to a logic "1" when the timer period has expired. Cleared to a logic "0" by:

1. Reading the Status Register
2. New G/Purpose Timer information
3. General Reset command

Notone Timer Period: Set to a logic "1" when the timer period has expired. Cleared to a logic "0" by:

1. Reading the Status Register
2. New Notone Timer information
3. General Reset command

RX Tone Measurement: Set to a logic "1" when the RX Tone Measurement is complete. Cleared to a logic "0" by:

1. Reading the Status Register
2. General Reset command

Setting	Status Bits
MSB	**Received First**
Bit 7	**Set to**
0	0
Bit 6	**Set to**
0	0
Bit 5	**Set to**
0	0
Bit 4	**Set to**
0	0
Bit 3	**Logic Input Status**
1	1
0	0
Bit 2	**G/Purpose Timer Period**
1	Expired
	(Interrupt Generated)
Bit 1	**Notone Timer Period**
1	Expired
	(Interrupt Generated)
Bit 0	**RX Tone Measurement**
1	Complete
	(Interrupt Generated)

Table 5: Status Register

5.2.3 TX Tone Generator Registers 1 and 2

Each TX Tone Generator is controlled individually by writing a two-byte command to the relevant TX Tone Generator Register. The format of this command word, which is different for each tone generator, is shown below with the calculations required for tone frequency (f_{TONE}) generation described in the following text.

5.2.3.1 Write to TX Tone Generator 1 Register

A/C 34_H, followed by 2 bytes of Command Data

MSB (loaded first)			**Bit Numbers**												**LSB (loaded last)**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Notone/Enable	These 13 bits (0 to 12) are used to produce a binary number, designated 'A'. 'A' is used in the formulas below to set the TX Tone 1 frequency ($f_{TONE}1$).												

Table 6: Tx Tone Generator 1

5.2.3.1.1 SETTING TX TONE GENERATOR 1

The binary number produced by Bits 0 to 12 (MSB) is designated "A." If "A" = all logic "0" TX Tone Generator 1 is Powersaved.

Bit 13 at logic 1 = Tone 1 Output at V_{BIAS} (NOTONE)
0 = Tone 1 Output Enabled

Bits14 and15(MSB) must be logic 0

5.2.3.2 Write to TX Tone Generator 2 Register

A/C 35_H, followed by 2 bytes of Command Data

MSB (loaded first)			**Bit Numbers**												**LSB (loaded last**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CAL/CUES	Notone/Enable	These 13 bits (0 to 12) are used to produce a binary number, designated 'B'. 'B' is used in the formulas below to set the TX Tone 2 frequency ($f_{TONE}2$).												

Table 7: Tx Tone Generator 2

Write to TX Tone Generator 2 Register Notes:

Programming Tone Generator 2 to Notone will place the CAL/CUES output at V_{BIAS} via a 40kΩ internal resistor.

Programming Tone Generator 2 to Powersave will place the CAL/CUES output at V_{SS}.

If both Tone Generators are Powersaved, the Input Amplifier is also Powersaved

5.2.3.2.1 SETTING TX TONE GENERATOR 2

The binary number produced by bits 0 to 12 (MSB) is designated "B." If "B" = all logic "0" then TX Tone Generator 2 is Powersaved.

Bit 13 at logic 1 = Tone 1 Output at V_{BIAS} (NOTONE)
0 = Tone 1 Output Enabled
Bit 14 at logic 1 = Squarewave CAL Output
0 = Sinewave CUES Output

Bit 15 (MSB) must be a logic "0."

5.2.3.3 Calculations

As seen in Table 6 and Table 7, a binary number ("A" or "B" - bits 0 to 12) is loaded to the respective TX Tone Generator. The formulas described below are used to produce the required output frequency.

Required TX Tone output frequency	=	f_{TONE} 1 or 2
Xtal/clock frequency	=	f_{XTAL}
Input Data Word (bits 0 to 12)	=	"A" or "B"

$$f_{TONE} = \frac{f_{XTAL}}{4 \times \text{'A' or 'B'}} \text{ Hz} \quad \text{or} \quad \text{Input 'A' or 'B'} = \frac{f_{XTAL}}{4 \times f_{TONE}} \text{ Hz}$$

5.2.3.4 Tx Tone Frequencies

With reference to Table 6 and Table 7, while Input Data Words "A" or "B" can be programmed for frequencies outside the stated limits of 208Hz and 3000Hz, any output frequencies obtained may not be within specified parameters. See section 6.

5.2.4 Read RX Tone Frequency Register

A/C 32_H, followed by 2 bytes of Reply Data

5.2.4.1 Measurement of RX Signal Frequency S_{IN}

The input audio signal, S_{IN}, is measured in the Frequency Counter over a specified measurement period (9.125ms or 18.250ms).

The measuring function counts the number of complete input cycles occurring within the count period and then the number of measuring clock cycles necessary to make up the period.

When the count period of a successful decode is complete, the RX Tone Measurement bit in the Status Register and the Interrupt bit are set.

The RX Tone Frequency Register will now indicate the signal frequency S_{IN} in the form of 2 bytes (1 and 0) as illustrated in Figure 6.

Note: The following measurements are based on a clock frequency of 4.032 MHz. See section 5.2.4.4 for a scaling formula for other crystal values).

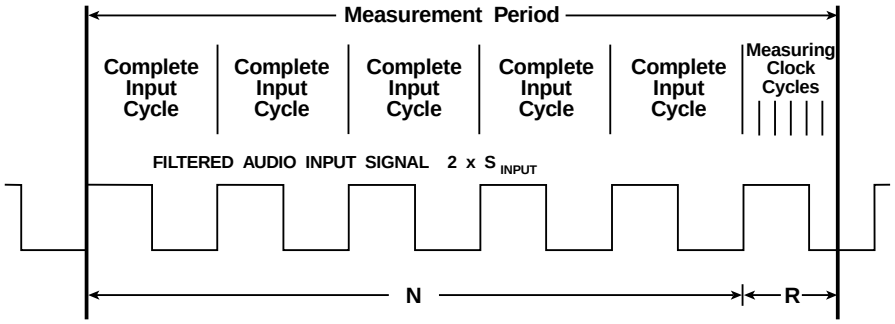


Figure 5: Measurement of an Rx Frequency

5.2.4.2 The Integer (N) - Byte 1

This is a binary number representing twice the number of complete input audio cycle periods. It is counted during the specified measurement period (t), when (t) is:

High Band Decode	=	9.125ms
Mid Band Decode	=	18.250ms
Extended Band Decode	=	9.125ms

Note: See section 5.2.4.4 for calculation of measurement period (t) using a Xtal other than 4.032MHz.

5.2.4.3 The Remainder (R) - Byte 0

This is a binary number representing the remainder part, R, of twice the Input Signal Frequency. R = "the number of specified measuring-clock cycles" required to complete the specified measurement period (See 5.2.4.2). The clock cycle frequency (f) is:

High Band Decode	=	56.00kHz
Mid Band Decode	=	28.00kHz
Extended Band Decode	=	56.00kHz

Note: See section 5.2.4.4 for calculation of clock cycle frequency (f) using a Xtal other than 4.032MHz.

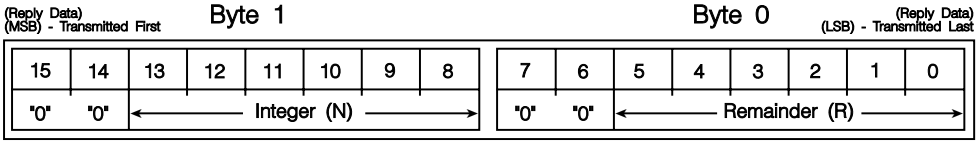


Figure 6: Format of the Rx Tone Frequency Register

5.2.4.4 f_{XTAL} Scaling Factors

The following formulas allow the calculation of the Integer N (see section 5.2.4.2) and the Remainder R (see section 0) using any Xtal value.

$$t\ scaled = t \times \left(\frac{4.032}{f_{XTAL}}\right) \qquad f\ scaled = f \times \left(\frac{f_{XTAL}}{4.032}\right)$$

5.2.5 Frequency Measurement

The following formulas show the derivation of the Rx frequency S_{IN} from the measured data bytes (N and R)

Note: The following measurements are based on a clock frequency of 4.032 MHz. See section 5.2.4.4 for a scaling formula for other Xtal values.

5.2.5.1 High Band Measurement

S_{IN} - High Band

In the measurement period of 9.125ms, there are N cycles at $2S_{IN}$ and R clock cycles at 56.000kHz.

$$\frac{N}{2S_{IN}} + \frac{R}{56000} = 9.125ms$$

$$\text{from which } S_{IN} = \frac{28000 \times N}{(511 - R)}$$

N and R - High Band

The measurement period = 9.125ms.
Clock Frequency = 56.000kHz
The measured frequency = $2S_{IN}$Hz
In the measurement period there are:

$9.125 \times 10^{-3} \times 2S_{IN}$ cycles

N_{HIGH} is the lower integer value of the number of $2S_{IN}$ cycles:

$N = INT(9.125 \times 10^{-3} \times 2S_{IN})$

R_{HIGH} is the number of remaining measuring clock cycles to complete the measurement period, rounded to the nearest integer:

$$R = ROUND\left(\left(9.125 \times 10^{-3} - \frac{N}{2S_{IN}}\right) \times 56000\right)$$

5.2.5.2 Mid Band Measurement

S_{IN} - MID Band

In the measurement period of 18.250ms, there are N cycles at $2S_{IN}$ and R clock cycles at 28.000kHz.

$$\frac{N}{2S_{IN}} + \frac{R}{28000} = 18.250\text{ms}$$

$$\text{from which } S_{IN} = \frac{14000 \times N}{(511 - R)}$$

N and R - Mid Band

The measurement period = 18.250ms.
Clock Frequency = 28.000kHz
The measured frequency = $2S_{IN}$Hz
In the measurement period there are:

$18.250 \times 10^{-3} \times 2S_{IN}$ cycles

N_{MID} is the lower integer value of the number of $2S_{IN}$ cycles:

$$N = \text{INT}(18.250 \times 10^{-3} \times 2S_{IN})$$

R_{MID} is the number of remaining measuring clock cycles to complete the measurement period, rounded to the nearest integer:

$$R = \text{ROUND}\left(\left(18.250 \times 10^{-3} - \frac{N}{2S_{IN}}\right) \times 28000\right)$$

5.2.5.3 Extended Band Measurement

S_{IN} - Extended Band

In the measurement period of 9.125ms, there are N cycles at S_{IN} and R clock cycles at 56.000kHz.

$$\frac{N}{S_{IN}} + \frac{R}{56000} = 9.125\text{ms}$$

$$\text{from which } S_{IN} = \frac{56000 \times N}{(511 - R)}$$

N and R - Extended Band

The measurement period = 9.125ms.
Clock Frequency = 56.000kHz
The measured frequency = S_{IN}Hz
In the measurement period there are:

$9.125 \times 10^{-3} \times S_{IN}$ cycles

$N_{EXTENDED}$ is the lower integer value of the number of S_{IN} cycles:

$$N = \text{INT}(9.125 \times 10^{-3} \times S_{IN})$$

$R_{EXTENDED}$ is the number of remaining measuring clock cycles to complete the measurement period, rounded to the nearest integer:

$$R = \text{ROUND}\left(\left(9.125 \times 10^{-3} - \frac{N}{S_{IN}}\right) \times 56000\right)$$

5.2.6 Write to RX Notone Timer Register

A/C 33_H, followed by 1 byte of Command Data

5.2.6.1 Operation of the RX Notone Timer

A NOTONE period is that period when no signal or a consistently bad quality signal is received. The NOTONE Timer is employed to indicate to the μC that a NOTONE situation has existed for a predetermined period.

The NOTONE Timer period is "primed" by writing to the NOTONE Timer Register (33_H) using the instructions and information (1 data byte) given in Table 8. This timer register can be written-to and set in any mode of the MX803A except "Notone Timer Powersave." Priming the timer sets the timing period; this period will not be allowed to start until at least one frequency (tone) measurement has been successfully completed.

The NOTONE Timer is a one-shot timer that is reset only by successful tone measurements.

If the quality of the received signal drops to an unusable level the NOTONE Timer will start its run-down. On completion of this timer period, the NOTONE Timer Period Expired bit in the Status Register and an Interrupt are set.

Upon detection of the Interrupt, the Status Register should be read by the μC to ascertain the source of the Interrupt.

The NOTONE Timer Period Expired bit is cleared:

1. By a read of the Status Register.
2. New NOTONE Timer Information
3. General Reset Command

The timer is set to 00_H by a General Reset command.

Setting				**Function / Period**			
MSB							
7	**6**	**5**	**4**	**Transmitted Bit 7 first**			
0	0	0	0	these 4 bits must be 0			
				period (ms)			
3	**2**	**1**	**0**	**High Band**	**%**	**Mid Band**	**%**
0	0	0	0	0		0	
0	0	0	1	20	±1	40	±1
0	0	1	0	40	±1	80	±1
0	0	1	1	60	±1	120	±1
0	1	0	0	80	±1	160	±1
0	1	0	1	100	±1	200	±1
0	1	1	0	120	±1	240	±1
0	1	1	1	140	±1	280	±1
1	0	0	0	160	±1	320	±1
1	0	0	1	280	±1	360	±1
1	0	1	0	200	±1	400	±1
1	0	1	1	220	±1	440	±1
1	1	0	0	240	±1	480	±1
1	1	0	1	260	±1	520	±1
1	1	1	0	280	±1	560	±1
1	1	1	1	300	±1	600	±1

Table 8: RX Notone Timer Settings

5.2.6.2 NOTONE TIMER CIRCUITRY

The following situations may be encountered by the Notone Timer Circuitry

5.2.6.2.1 No Signal

The Notone timer can only start its run down on completion of a valid frequency measurement.

5.2.6.2.2 No signal after a valid Tone measurement

The timer will start to run down when the last RX Tone Measurement complete bit is set. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

5.2.6.2.3 Signal fades after a valid Tone measurement

The timer will start to run down when the signal becomes unreadable to the device. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

5.2.6.2.4 Signal appears after the Timer has started

If the frequency measurement is more than 75% complete when the timer period expires, neither the NOTONE bit nor the Interrupt will be set unless that frequency measurement is subsequently aborted.

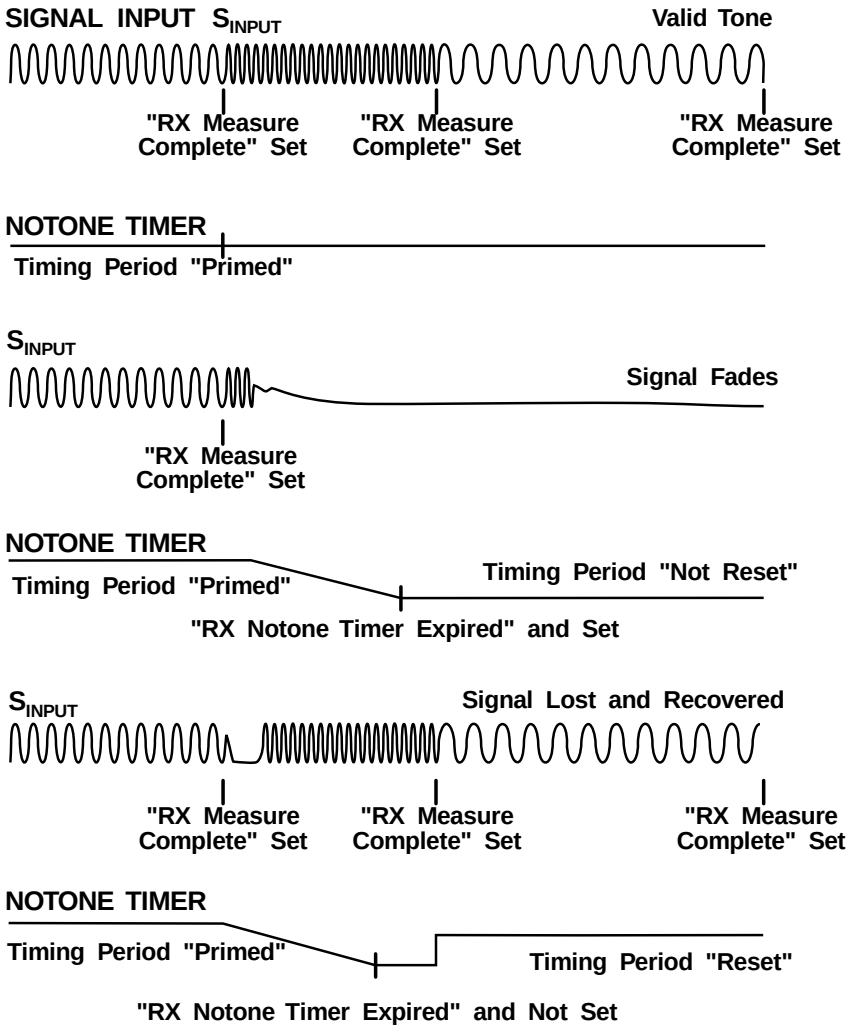


Figure 7: Notone Timing

5.2.7 Write to General Purpose Timer Register

A/C 36_H, followed by 1 byte of Command Data

5.2.7.1 Operation of the General Purpose Timer

This timer, which is not dedicated to any specific function within the MX803A, can be used within the DBS 800 system to indicate time-elapsed periods of between 10-150ms in the High Band or 20-300ms in the Mid Band to the μC. Setting of the timer is by loading a single byte data word via the C-BUS (See Table 9) to the MX803A through the Command Data line.

The timer will be reset and the run-down started on completion of Timer Data Word loading.

When the programmed time period has expired, the General Purpose Timer Expired bit (bit 2) in the Status Register and the Interrupt are set.

The General Purpose Timer Expired bit is cleared:

1. By a read of the Status Register
2. New G/P Timer information
3. General Reset Command.

When the programmed time period has expired, this timer will reset, restart itself and continue sequencing until:

1. New G/P Timer information is written
2. A General Reset Command is received.

The General Purpose Timer Expired bit and the interrupt will remain set until cleared.

The timer is set to 00_H (0ms) by a General Reset command.

Setting				Function / Period			
MSB							
7	**6**	**5**	**4**	**Transmitted Bit 7 first**			
0	0	0	0	these 4 bits must be 0			
				Reset Timer and Start Timing period (ms)			
3	**2**	**1**	**0**	**High Band**	**%**	**Mid Band**	**%**
0	0	0	0	0		0	
0	0	0	1	10	±1	20	±1
0	0	1	0	20	±1	40	±1
0	0	1	1	30	±1	60	±1
0	1	0	0	40	±1	80	±1
0	1	0	1	50	±1	100	±1
0	1	1	0	60	±1	120	±1
0	1	1	1	70	±1	140	±1
1	0	0	0	80	±1	160	±1
1	0	0	1	90	±1	180	±1
1	0	1	0	100	±1	200	±1
1	0	1	1	110	±1	220	±1
1	1	0	0	120	±1	240	±1
1	1	0	1	130	±1	260	±1
1	1	1	0	140	±1	280	±1
1	1	1	1	150	±1	300	±1

Table 9: General Purpose Timer Settings

5.3 Powersave

Various sections of the MX803A can be placed independently into a power-economical condition. Table 10 gives a summary of these states available to the MX803A.

Powersaved Section	Instruction Source		Table
Tone Encoder 1	TX Tone Gen. 1 Reg. (34_H)	All bits = "0"	Table 6
Tone Encoder 2	TX Tone Gen. 2 Reg. (35_H)	All bits = "0"	Table 7
Input Amplifier	This action is automatic when both Tone Encoders are in the Powersave condition		

Table 10: MX803A Powersave Functions

5.3.1 Powersave Conditions

Xtal/Clock and C-BUS: This circuitry is always active, on all DBS 800 ICs, under any depowered/powersaved conditions

5.4 Interrupt Request $\overline{\text{IRQ}}$

An Interrupt (IRQ), when enabled, is provided by the MX803A to indicate the following conditions to the µC.

	Notone Timer Period Expired	G/Purpose Timer Period Expired	Rx Tone Measurement Complete
Enabled	By control Resister bit 5	By control Resister bit 6	By control Resister bit 5
Set	When the preset Notone Flag is set	When the General Purpose Timer has timed out.	When an RX Frequency Measurement has been successfully completed
Identified	By Status Register bit 1	By Status Register bit 2	By Status Register bit 0
Cleared	By reading the Status Register	By reading the Status Register	By reading the Status Register

Table 11: Interrupt Request

On recognition of the "Read Status" Command byte, the interrupt output is cleared, the Status bits are transferred to the µC via the C-BUS Reply Data line and the internal Status bits are cleared.

5.5 Operational Recommendations

Following initial system power-up, a General Reset command should be sent.

5.5.1 Receive Sequence

1. Send Control Command for RX: Select Midband/Highband and Digital Filter length.
2. Disable transmitters if desired by writing to Tone Frequency registers.
3. Prime the Notone timer by sending the required period byte.
4. Enable/disable interrupts as desired.
5. When a valid tone has been detected by a successfully completed measurement the Status Register is set to "Tone Measurement Complete" and an interrupt is set to the µC.
6. The µC examines the Status Register. If tone measurement is complete, it reads in the RX Tone Frequency in the form N + R (Figure 6).
7. RX Tone Measurement Complete interrupts are periodically sent to the µC unless Notone is detected, in which case a Notone Interrupt is sent.

5.5.2 Transmit Sequence

1. Set Tone Frequency Generators to Notone during the transmitter initialization period.
2. Send Control Command for TX: Select Sum/Switched Sum Out and Audio Switch states.
3. Send General Purpose (GP) Timer information for the Notone transmitter initialization period. This will initiate the timer.
4. Enable/disable interrupts as desired.
5. µC waits for "GP Timer Expired," reads the Status Register to check interrupts due to timer, and resets the Status Bit. If required, the µC sends the next timer period followed by the next tone(s) frequency information. A new timer period sent will reset the timer, otherwise the timer is self-resetting.
6. The µC monitors the interrupts and repeats steps 5 and 6 as required.
7. After last loaded tone, µC turns off Tone Generator(s).

5.6 General Reset

Upon power-up the bits in the MX803A registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to reset all microcircuits on the C-BUS. It has the following effect on the MX803A:

Control Register	Set as 00_H
Status Register (bits 0, 1, 2)	Set as 00_H
Notone Timer	Set as 00_H
Tone Gen. 1 Reg. (2 bytes)	Set as 0000_H
Tone Gen. 2 Reg. (2 bytes)	Set as 0000_H
Gen. Purpose Reg.	Set as 00_H

Table 12: General Reset effect on MX803A

This sets the MX803A to Encoder High Band (625Hz to 3000Hz) with interrupts disabled and both timers set to 00_H.
Both timers should be set up before interrupts are enabled to prevent initial, undesired interrupts.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Operation of the device outside of the operating limits is not suggested.

General	Min.	Max.	Units
Supply Voltage (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / P / LH Packages			
Operating Temperature	-40	85	°C
Storage Temperature	-55	125	°C
Total allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C

6.1.2 Operating Limits

All devices were measured under the following conditions unless otherwise noted.

	Notes	Min.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.5	V
Temperature		-40	85	°C
Xtal/Clock Frequency			4.0	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 5.0 @ T_{AMB} = 25°C Xtal = 4MHz (refer to section 5.2.4.4 for Xtal Scaling factor)
Audio level 0dB ref. = 308mV_{RMS} @ 1kHz (60% deviation, FM)
Noise Bandwidth = 5.0kHz Band-Limited Gaussian

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Decoder + Both Timers			2.0		mA
Decoder, Both Timers + One TX only			4.0		mA
All Functions Enabled			5.0		mA
Analog Impedance					
RX Audio Input			20.0		MΩ
Summing Amp Input			20.0		MΩ
Switch			1.0		kΩ
Tones 1 and 2 Outputs			10.0		kΩ
CAL/CUES Output			5.0		kΩ
Summing Outputs			10.0		kΩ
Dynamic Values					
Digital Interface					
Input Logic “1”	1	3.5			V
Input Logic “0”	1			1.5	V
Output Logic “1” (I_{OH} = -120μA)	2	4.6			V
Output Logic “0” (I_{OL} = 360μA)	3			0.4	V
I_{OUT} Tristate (Logic “1” or “0”)	3			4.0	μA
Input Capacitance	1			7.5	pF
I_{OX} (V_{OUT} = 5V)	4			4.0	μA
Overall Performances					
RX - Decoding					
High Band					
Sensitivity			-20.0		dB
Tone Response Time					
Good Signal	5,10			30.0	ms
Tone-to-Noise Ratio = 0dB	5,6,10			40.0	ms
Frequency					
Band		625		3000	Hz
Measurement Resolution			0.2		%
Measurement Accuracy	9		0.5		%
Mid-Band					
Sensitivity			-20.0		dB
Tone Response Time					
Good Signal	7,10			60.0	ms
Tone-to-Noise Ratio = 0dB	6,7,10			80.0	ms

	Notes	Min.	Typ.	Max.	Units
Frequency					
Band		313		1500	Hz
Measurement Resolution			0.2		%
Measurement Accuracy	9		0.5		%
Extended Band					
Sensitivity			-20.0		dB
Tone Response Time					
Good Signal	5,10			20.0	ms
Frequency					
Band		1250		6000	Hz
Measurement Resolution			0.2		%
Measurement Accuracy	9		0.5		%
TX - Encoders 1 and 2					
Tone Frequency		208		3000	Hz
Period ($1/f_{TONE}$) Error				1.0	µs
Tone Amplitude		-1.5		1.5	dB
Total Harmonic Distortion				5.0	%
Rise Time to 90%			$3/f_{TONE}$		ms
Fall Time to 10%	8			5.0	ms
Frequency Change Time			$3/f_{TONE}$		ms
Timers					
General Purpose					
Timing Period Range					
High-Band		10.0		150	ms
Mid-Band		20.0		300	ms
RX Notone					
Timing Period Range					
Hi-Band		20.0		300	ms
Mid-Band		40.0		600	ms
Xtal/Clock Frequency (f_{XTAL})			4.0	6.0	MHz

6.1.3.1 Operating Characteristics Notes:

6. Device control pins: Serial Clock, Command Data, and $\overline{CS}$.
7. Reply Data output.
8. Reply Data and $\overline{IRQ}$ outputs.
9. Leakage current into the “Off” $\overline{IRQ}$ output.
10. Measurement period = 9.198ms.
11. Decode Probability = 0.993.
12. Measurement period = 18.396ms.
13. When set to Powersave.
14. For a good input signal.
15. Inversely proportional to Xtal frequency, i.e. Spec. x $\frac{4MHz}{f_{XTAL}}$. So, for a 6MHz clock a 30ms tone response time becomes 20ms.

6.2 Timing Information

Figure 8 shows timing parameters for two-way communication between the µC and the MX803A on the C-BUS.

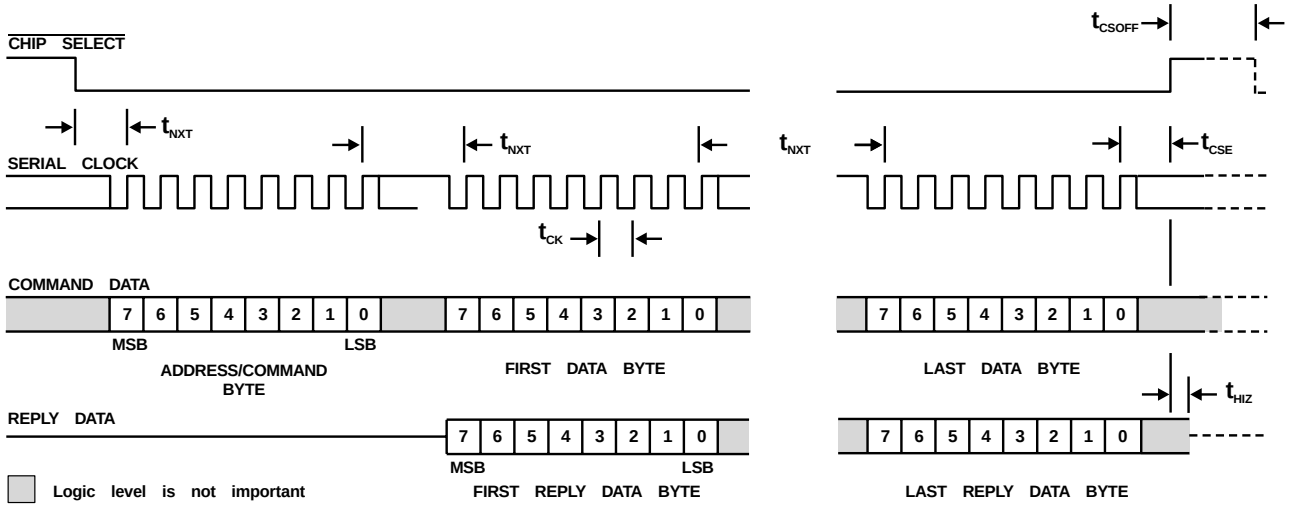


Figure 8: C-BUS Timing

Parameter		Min	Typ	Max	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0			µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0			µs
t_{CSOFF}	Chip Select High	2.0			µs
t_{NXT}	Command Data Inter-Byte Time	4.0			µs
t_{CK}	Serial Clock Period	2.0			µs
t_{CH}	Decoder or Encoder Clock High	500			ns
t_{CL}	Decoder or Encoder Clock Low	500			ns
t_{CDS}	Command Data Set-Up Time	250			ns
t_{CDH}	Command Data Hold Time	0			ns
t_{RDS}	Reply Data Set-Up Time	250			ns
t_{RDH}	Reply Data Hold Time	50.0			ns
t_{HIZ}	Chip Select High to Reply Data High - Z			2.0	µs

Table 13: Timing Information

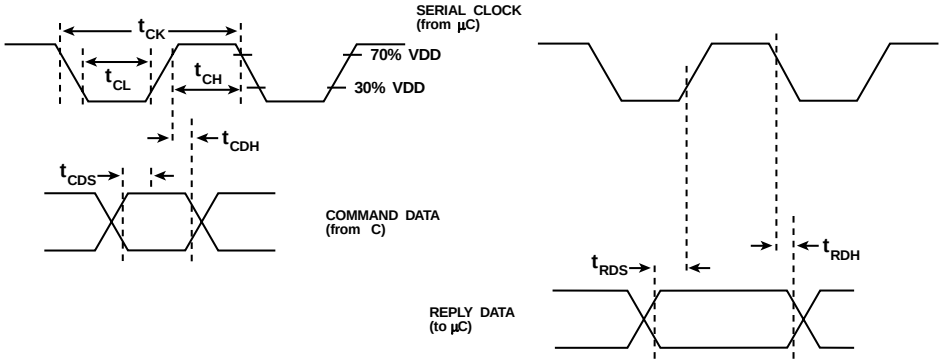
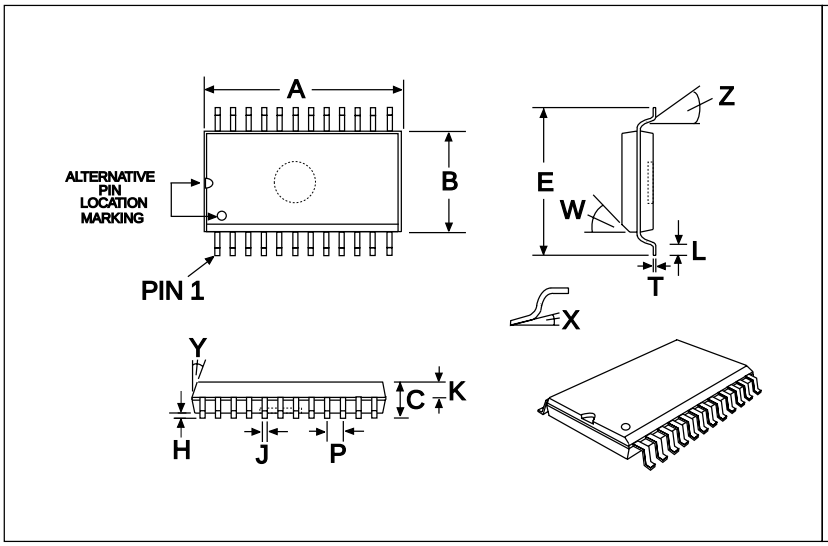


Figure 9: Timing Relationship for C-BUS Information Transfer

6.2.1 Timing Information Notes

1. Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the MX803A MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into the MX803A and into the µC on the rising Serial Clock edge.
3. Loaded data instructions are acted upon at the end of each individual, loaded byte.
4. To allow for differing µC serial interface formats, the MX803A will work with either polarity Serial Clock pulses.

6.3 Packaging

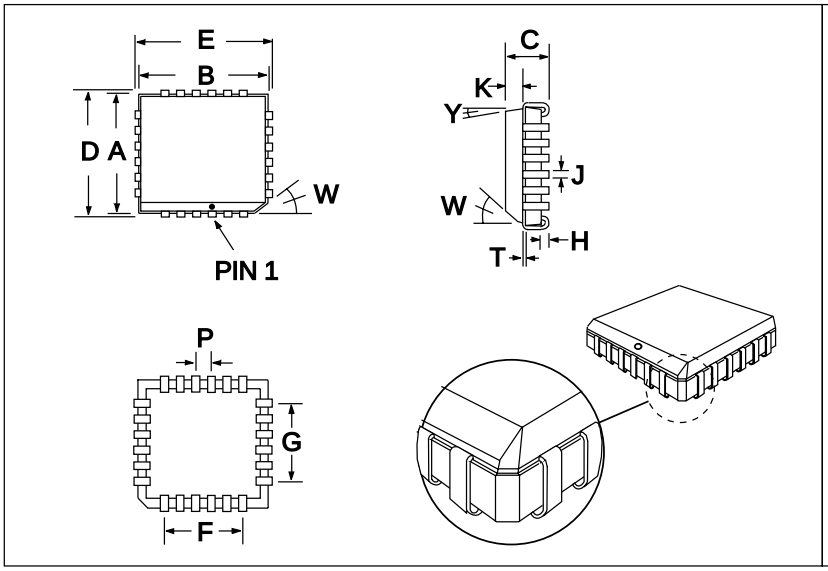


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin SOIC Mechanical Outline: order as part no. MX803ADW

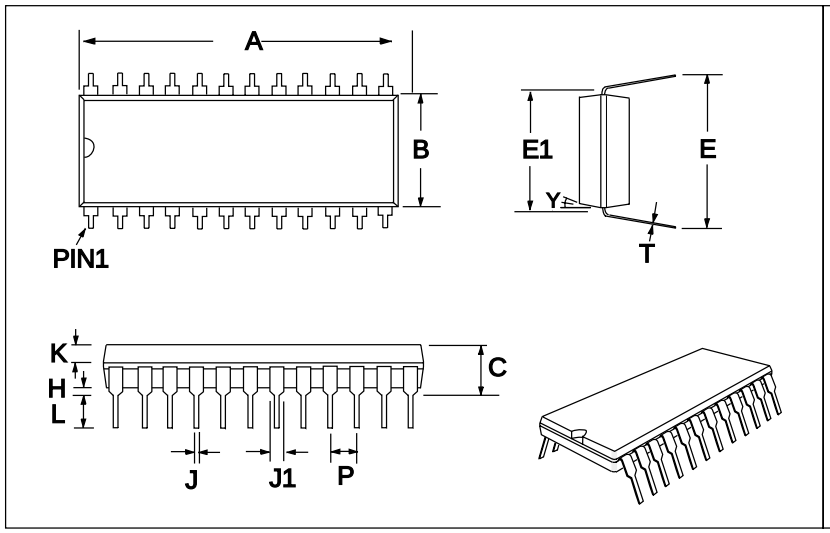


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PLCC Mechanical Outline: order as part no. MX803ALH



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 24-pin PDIP Mechanical Outline: order as part no. MX803AP

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the **'MX-COM'** textual logo is being replaced by a **'CML'** textual logo.

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D/CML (D)/2 May 2002