64-Bit MIPS RISC Microprocessor with Integrated L2 Cache

FEATURES

- Dual-Issue symmetric superscalar microprocessor
  - 600MHz max CPU frequency
  - Capable of issuing two instructions per clock cycle
- Integrated primary and secondary caches
  - 16KB Instruction, 16KB Data, and 256KB on-chip secondary
  - All are 4-way set associative with 32-byte line size
  - Per-line locking in primary and secondary caches
  - Fast Packet Cache™ increases system efficiency in networking applications
- Integrated external cache controller
  - Allows up to 64Mbyte of external cache for applications with large data sets
  - Enhanced protocol eliminates requirement for TAG RAMS
- High-performance system interface
  - 1600 Mbyte per-second peak throughput
  - 200 MHz max. freq., HSTL multiplexed address/data bus (SysAD200)
  - Supports two outstanding reads with out-of-order return
- High-performance floating-point unit
  - 1200 MFLOPS maximum
  - IEEE754 compliant single and double precision floating-point operations
- 64-bit MIPS instruction set architecture
  - Data PREFETCH instruction allows the processor to overlap cache miss latency and instruction execution
  - Single-cycle floating-point multiply-add
- Integrated memory management unit
  - Fully associative TLB
  - 64/48 dual entries map 128/96 pages
  - Variable page size
- Embedded application enhancements
  - Fourteen fully prioritized vectored interrupts-10 external, 2 internal, 2 software
  - Specialized DSP integer Multiply-Accumulate instructions (MAD/MADU), and three-operand Multiply instruction (MUL)
  - I and D Test/Break-point (Watch) registers for emulation and debug
  - Performance counter for system and software tuning and debug

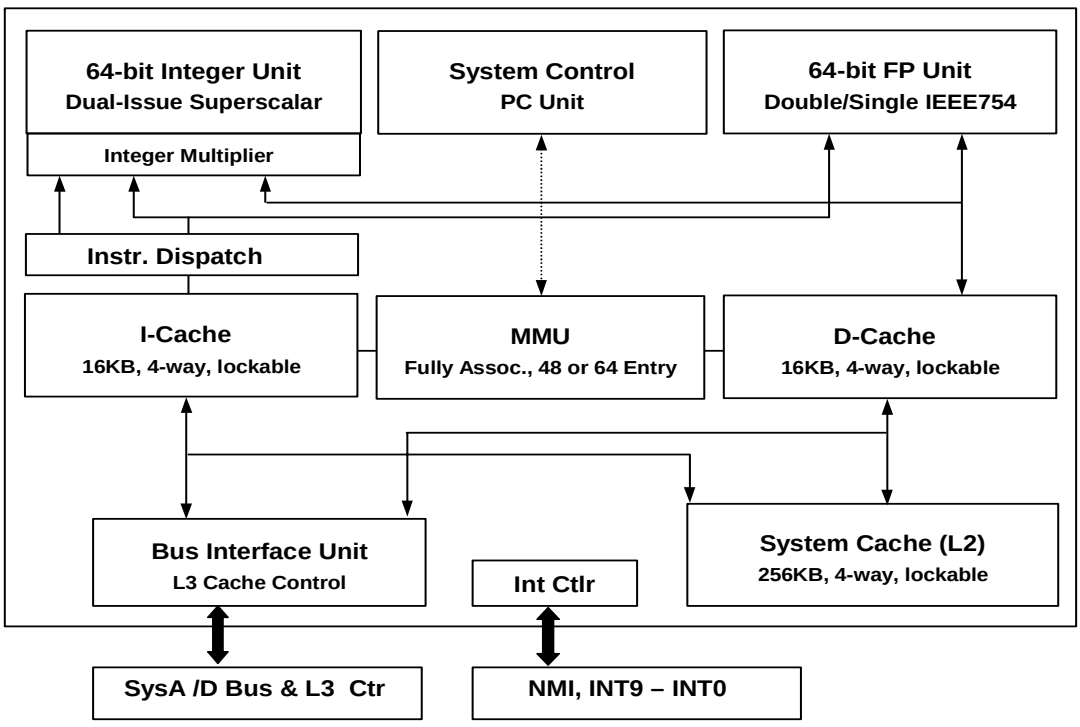
PACKAGING

- Fully Static 0.13µ CMOS design with dynamic power down logic
- 304 pin TBGA package, 31x31 mm

DEVELOPMENT TOOLS

- Operating Systems:
  - Linux by MontaVista and Red Hat
  - VxWorks by Wind River Systems
  - Nucleus by Accelerated Technology
  - Neutrino by QNX Software Systems
- Compiler Suites

BLOCK DIAGRAM



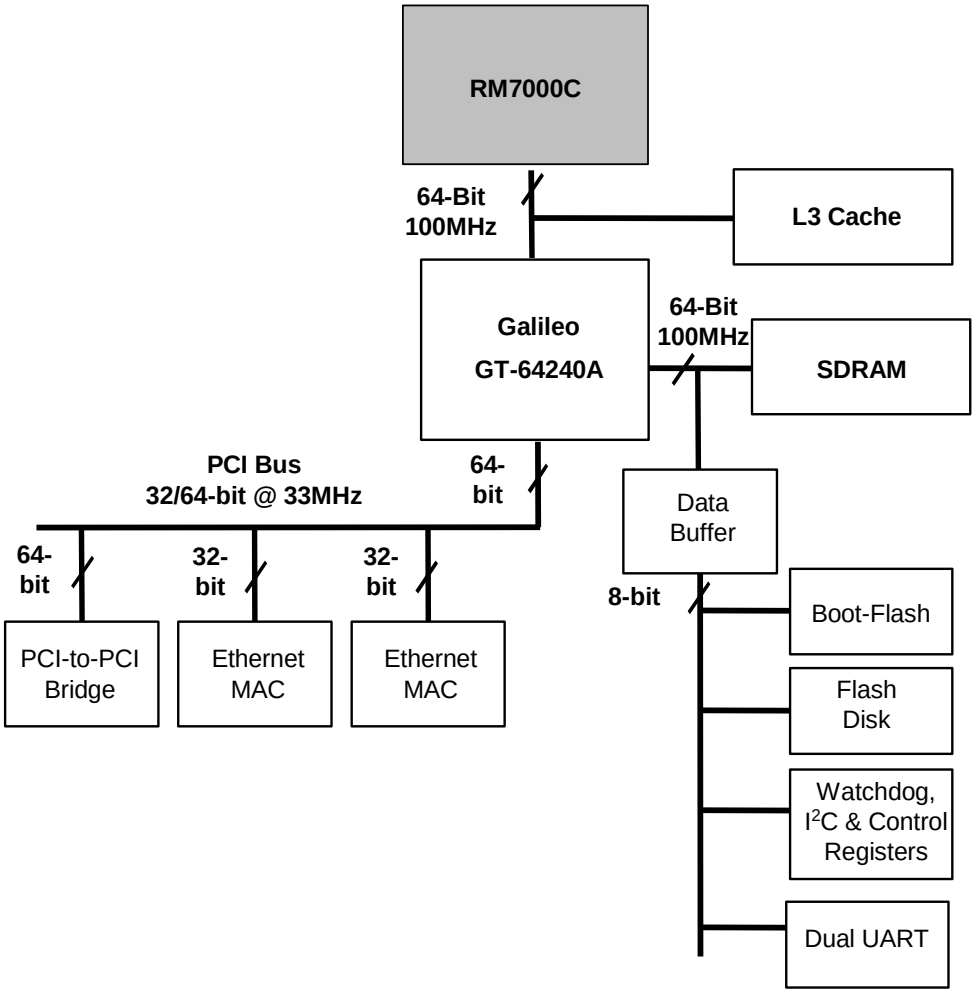
64-Bit MIPS RISC Microprocessor with Integrated L2 Cache

- Algorithmics
- Green Hills Software
- Red Hat
- Evaluation Boards and Companion Chips
  - Galileo Technology
    - EV-64120A-7000: 32/64-bit, 33/66MHz PCI
    - EV-64240-7000: 32/64-bit, 33/66MHz PCI
  - Momentum Computer
  - Ocelot: 6U RM7000 Compact PCI Single Board Computer
- Logic Analyzers and Emulation
  - HP
  - Tektronix
  - Corelis
  - Crescent Heart Software

APPLICATIONS

- Voice Gateways
- Multi-Service Access Platforms
- DSLAMs/Access Concentrators
- Remote Access Switches
- Web Switches
- Layer 3 Switches
- Backbone Switches/Routers
- RAIDs
- Set Top Boxes
- Networked Printers
- Cellular Base Stations

TYPICAL APPLICATION



Head Office:
PMC-Sierra, Inc.
#105 - 8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 604.415.6000
Fax: 604.415.6200

To order documentation, send email to: document@pmc-sierra.com or contact the head office, Attn: Document Coordinator

All product documentation is available on our web site at: http://www.pmc-sierra.com For corporate information, send email to: info@pmc-sierra.com

PMC- 2011604(P1)