DATA SHEET

SAA7356HL
1394 SBP-2 link layer controller

Preliminary specification
File under Integrated Circuits, IC01

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PHILIPS

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1 FEATURES

- Institute of Electrical and Electronics Engineers (IEEE) 1394-1995 standard link layer controller
- Compatible with the P1394a standard
- Fully automated Serial Bus Protocol 2 (SBP-2) transaction layer for data storage applications
- Interface to many of the industry standard Direct Memory Access (DMA) protocols
- Interface to any IEEE1394-1995 or P1394a PHY layer interface
- Very low power comma mode
- Small package
- Single 3.3 V supply voltage with 5 V tolerance.

2 GENERAL DESCRIPTION

The SAA7356HL is an IEEE1394-1995 and P1394a compliant link layer controller featuring an embedded SBP-2 transaction layer for data storage applications. The SAA7356HL provides full automation of the SBP-2 transaction layer to an extent that the user need not have knowledge of SBP-2 or 1394.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	3.3	3.6	V
I_{DD}	supply current	V_{DD} = 3.3 V	–	29	–	mA
SCLK	system clock		49.147	49.152	49.157	MHz

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7356HL	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

5 BLOCK DIAGRAM

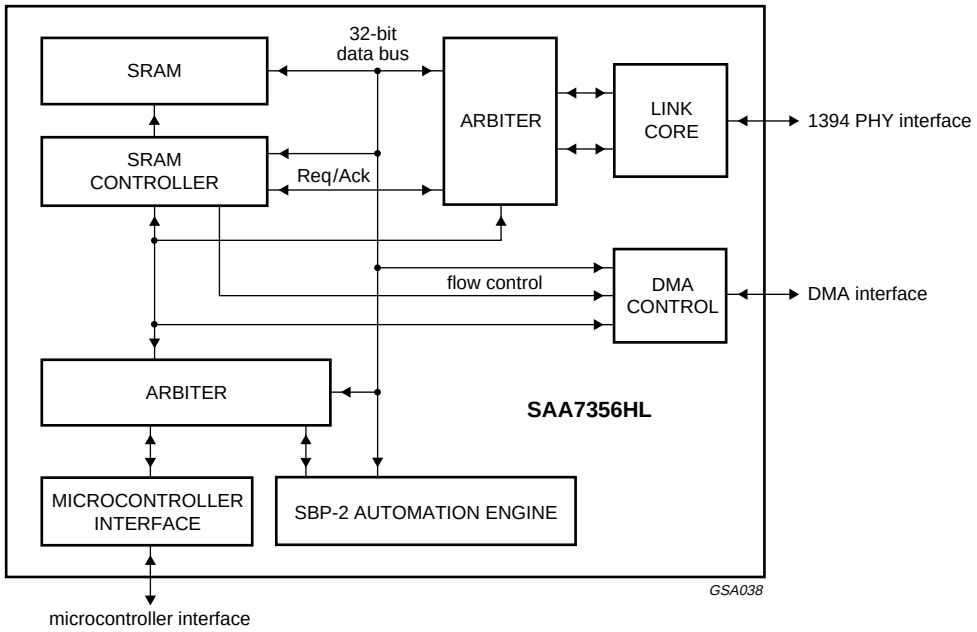


Fig.1 Block diagram.

6 PIN CONFIGURATION

SYMBOL	PIN	TYPE[1]	DESCRIPTION
MICRO_ADDR[0]	1	I	microcontroller address input (bit 0); note 2
MICRO_ADDR[1]	2	I	microcontroller address input (bit 1); note 2
MICRO_ADDR[2]	3	I	microcontroller address input (bit 2); note 2
MICRO_ADDR[3]	4	I	microcontroller address input (bit 3); note 2
$V_{DD1(P)}$	5	S	supply voltage 1 for periphery
$V_{SS1(P)}$	6	S	ground 1 for periphery
MICRO_ADDR[4]	7	I	microcontroller address input (bit 4); note 2
MICRO_ADDR[5]	8	I	microcontroller address input (bit 5); note 2
MICRO_ADDR[6]	9	I	microcontroller address input (bit 6); note 2
MICRO_ADDR[7]	10	I	microcontroller address input (bit 7); note 2
$V_{DD2(P)}$	11	S	supply voltage 2 for periphery
$V_{SS2(P)}$	12	S	ground 2 for periphery
DMA_DATA[15]	13	I /O	DMA data input/output (bit 15); note 3
DMA_DATA[14]	14	I /O	DMA data input/output (bit 14); note 3
DMA_DATA[13]	15	I /O	DMA data input/output (bit 13); note 3
DMA_DATA[12]	16	I /O	DMA data input/output (bit 12); note 3
DMA_DATA[11]	17	I /O	DMA data input/output (bit 11); note 3
DMA_DATA[10]	18	I /O	DMA data input/output (bit 10); note 3
$V_{DD1(C)}$	19	S	supply voltage 1 for core
$V_{SS1(C)}$	20	S	ground 1 for core
DMA_DATA[9]	21	I /O	DMA data input/output (bit 9); note 3
DMA_DATA[8]	22	I /O	DMA data input/output (bit 8); note 3
DMA_DATA[7]	23	I /O	DMA data input/output (bit 7); note 3
DMA_DATA[6]	24	I /O	DMA data input/output (bit 6); note 3
DMA_DATA[5]	25	I /O	DMA data input/output (bit 5); note 3
DMA_DATA[4]	26	I /O	DMA data input/output (bit 4); note 3
DMA_DATA[3]	27	I /O	DMA data input/output (bit 3); note 3
DMA_DATA[2]	28	I /O	DMA data input/output (bit 2); note 3
$V_{SS3(P)}$	29	S	ground 3 for periphery
$V_{DD3(P)}$	30	S	supply voltage 3 for periphery
DMA_DATA[1]	31	I /O	DMA data input/output (bit 1); note 3
DMA_DATA[0]	32	I /O	DMA data input/output (bit 0); note 3
DMA_REQ	33	O	DMA request signal output in slave mode (acknowledge in master/ATA mode) (may be configured for active HIGH or active LOW)
DMA_ACK	34	I	DMA acknowledge signal input in slave mode (request in master/ATA mode) (may be configured for active HIGH or active LOW)
$V_{SS2(C)}$	35	S	ground 2 for core
$V_{DD2(C)}$	36	S	supply voltage 2 for core
DMA_READ	37	I /O	DMA read strobe input/output (may be configured for active HIGH or active LOW)

SYMBOL	PIN	TYPE(1)	DESCRIPTION
DMA_WRITE	38	I /O	DMA write strobe input/output (may be configured for active HIGH or active LOW)
PHY_CTRL[1]	39	I /O	PHY control line input/output (1); note 4
PHY_CTRL[0]	40	I /O	PHY control line input/output (0); note 4
PHY_DATA[0]	41	I /O	PHY data input/output (bit 0); notes 4, 5 and 6
PHY_DATA[1]	42	I /O	PHY data input/output (bit 1); notes 4 and 5
PHY_DATA[2]	43	I /O	PHY data input/output (bit 2); notes 4 and 5
PHY_DATA[3]	44	I /O	PHY data input/output (bit 3); notes 4 and 5
$V_{SS4(P)}$	45	S	ground 4 for periphery
$V_{DD4(P)}$	46	S	supply voltage 4 for periphery
PHY_DATA[4]	47	I /O	PHY data input/output (bit 4); notes 4 and 5
PHY_DATA[5]	48	I /O	PHY data input/output (bit 5); notes 4 and 5
PHY_DATA[6]	49	I /O	PHY data input/output (bit 6); notes 4 and 5
PHY_DATA[7]	50	I /O	PHY data input/output (bit 7); notes 4 and 5
$V_{DD5(P)}$	51	S	supply voltage 5 for periphery
$V_{SS5(P)}$	52	S	ground 5 for periphery
PHY_SCLK	53	I	PHY system clock input (49.152 MHz)
MICRO_SEL[0]	54	I	microcontroller select (0) input; selects microcontroller interface; note 10
PHY_LREQ	55	O	PHY-Link request output (used to request arbitration or read/write PHY registers); note 4
$\overline{\text{PHY\_ISO}}$	56	I	PHY isolation barrier input (active LOW). Negated HIGH when the Link and PHY are directly connected or when bus-holder isolation is used; note 4
MICRO_SEL[1]	57	I	microcontroller select (1) input; selects microcontroller interface; note 10
1394_MODE	58	I /O	note 7
$\overline{\text{RESET}}$	59	I	asynchronous master reset input to the SAA7356HL (active LOW)
TC	60	–	reserved for factory testing; for normal operation should be connected to ground
BT	61	–	reserved for factory testing; for normal operation should be connected to ground
$\overline{\text{MICRO\_CS}}$	62	I	microcontroller chip select input (active LOW)
$V_{DD3(C)}$	63	S	supply voltage 3 for core
$V_{SS3(C)}$	64	S	ground 3 for core
$\overline{\text{MICRO\_INT}}$	65	O	microcontroller interrupt open-drain output (active LOW)
$\overline{\text{MICRO\_WRITE}}$	66	I	microcontroller write strobe input (active LOW)
$\overline{\text{MICRO\_READ}}$	67	I	microcontroller read strobe input (active LOW)
MICRO_ALE	68	I	microcontroller address latch enable input; note 8
$V_{SS6(P)}$	69	S	ground 6 for periphery
$V_{DD6(P)}$	70	S	supply voltage 6 for periphery
MICRO_DATA[0]	71	I /O	microcontroller data input/output [bit 0); note 9
MICRO_DATA[1]	72	I /O	microcontroller data input/output (bit 1); note 9
MICRO_DATA[2]	73	I /O	microcontroller data input/output (bit 2); note 9
MICRO_DATA[3]	74	I /O	microcontroller data input/output (bit 3); note 9

SYMBOL	PIN	TYPE[1]	DESCRIPTION
MICRO_DATA[4]	75	I /O	microcontroller data input/output (bit 4); note 9
MICRO_DATA[5]	76	I /O	microcontroller data input/output (bit 5); note 9
$V_{SS4(C)}$	77	S	ground 4 for core
$V_{DD4(C)}$	78	S	supply voltage 4 for core
MICRO_DATA[6]	79	I /O	microcontroller data input/output (bit 6); note 9
MICRO_DATA[7]	80	I /O	microcontroller data input/output (bit 7); note 9

Notes

1. Pin type abbreviations: I = Input, O = Output and S = Supply.
2. Used in NEC V851 and 16-bit Intel 8031 microcontroller interface configurations.
3. DMA data to the external buffer manager may be configured for 16 or 8 bits wide. For 16-bit operation pins DMA_DATA[15:0] are used, and for 8-bit operation, pins DMA_DATA[7:0] are used.
4. For more information see IEEE1394-1995 standard, Annex J.
5. Data is expected on PHY_DATA[0:1] for 100 Mbits/s, PHY_DATA[0:3] for 200 Mbits/s and PHY_DATA[0:7] for 400 Mbits/s.
6. To preserve compatibility to the specified Link-PHY interface of the IEEE1394-1995 standard, Annex J, bit 0 is the most significant bit.
7. During Power-on reset, this line is sampled to select between IEEE1394-1995 mode (HIGH) and P1394a mode (LOW). A 22 kΩ pull-up or pull-down resistor should be connected accordingly. This line acts as the $\overline{\text{MICRO\_WAIT}}$ line when the V851 microcontroller interface mode is selected.
8. Used in NEC V851 and Intel 8031 (8-bit and 16-bit) microcontroller interface configurations.
9. This is the data bus for all microcontroller interface configurations. This forms the lower address bus for the NEC V851 and Intel 8031 microcontroller configurations.
10. MICRO_SEL [1:0] = ‘00’ selects 8-bit 8031 mode; MICRO_SEL [1:0] = ‘01’ selects H8 mode; MICRO_SEL [1:0] = ‘10’ selects 16-bit 8031 mode; MICRO_SEL [1:0] = ‘11’ V851 mode.

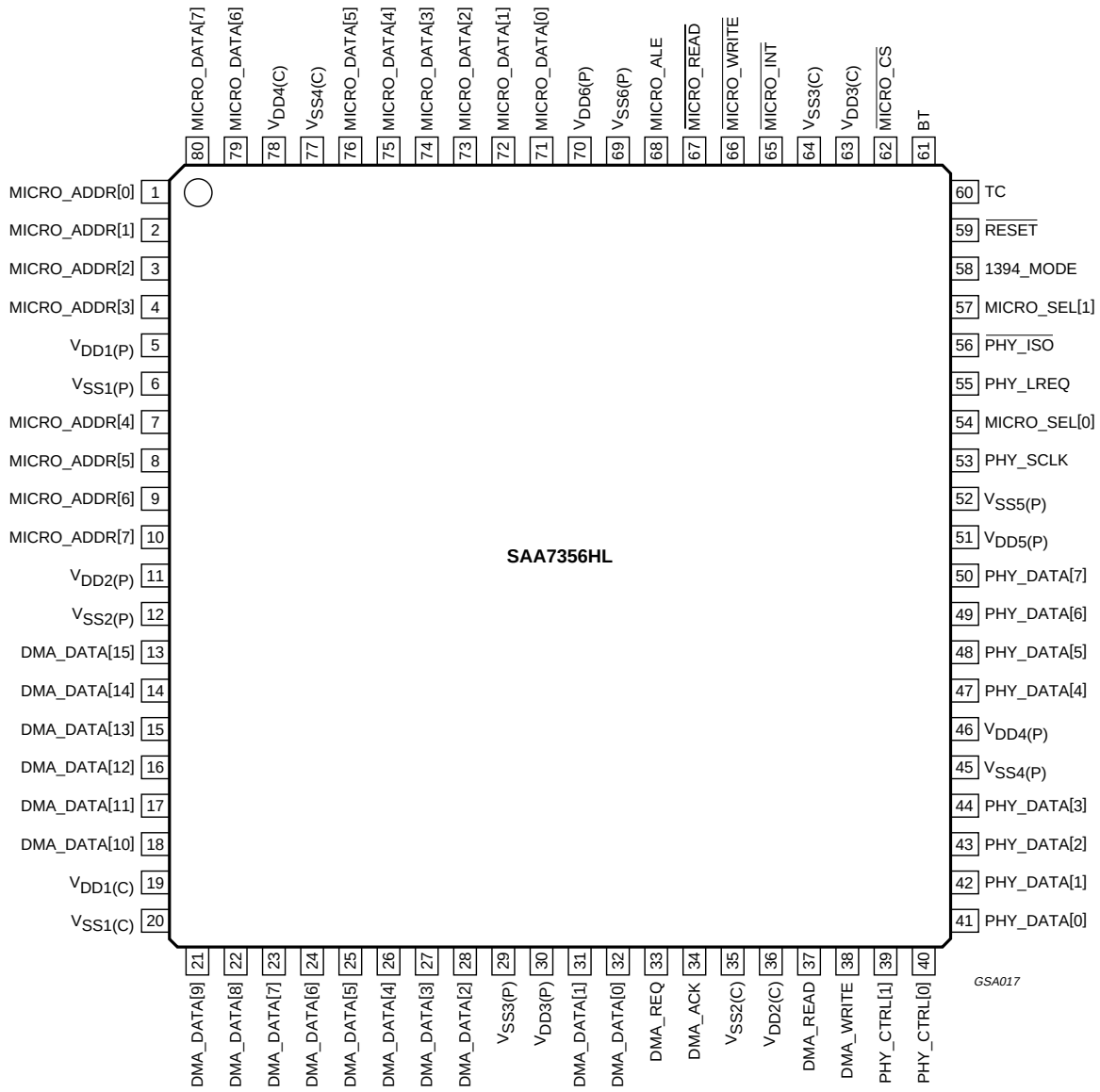


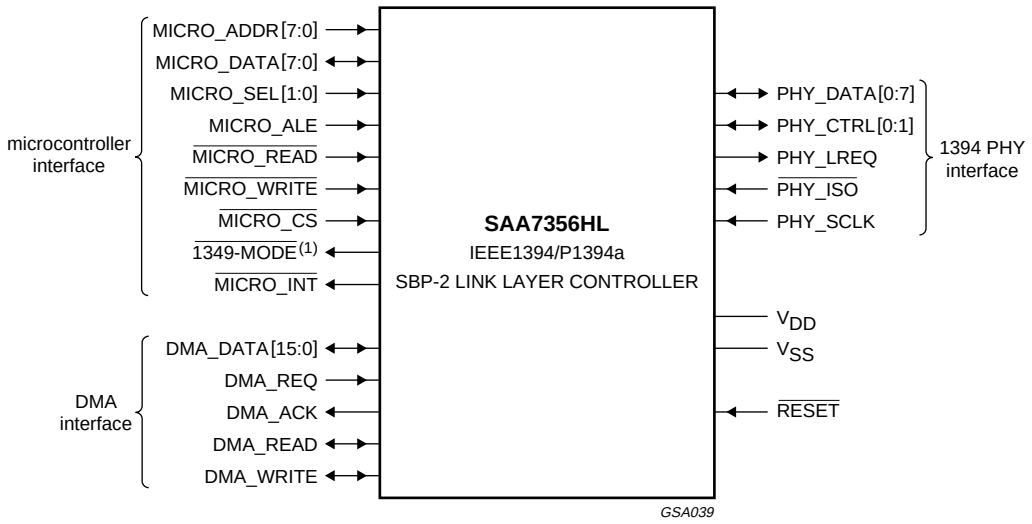
Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Overview

The SAA7356HL is an IEEE1394-1995 and P1394a compliant link layer controller. It provides a direct interface between a 1394 bus and a DMA interface found on many buffer managers (see Fig.3). Through this interface, the SBP-2 automation engine performs all transaction layer specific operations; these include the management agent, fetch agent, and page table handling features.

The SBP-2 link also provides an interface to an external microcontroller. The microcontrollers supported include 8/16-bit addressing from the Intel 8031 derivatives, the Hitachi H8 and the NEC V851. Through this interface, the microcontroller retrieves the 12-byte Command Descriptor Blocks (CDBs) and provides the command status indication; unsolicited status information is also supported.



(1) Acts as the MICRO_WAIT line when the V851 microcontroller interface mode is selected.

Fig.3 Functional diagram.

7.2 SBP-2 automation engine

The complete SBP-2 transaction layer is supported by the SAA7356HL. This includes the log-in, log-out and reconnect functions in the management agent plus the fetch engine for retrieving linked lists of Operation Request Blocks (ORBs) from the logged-in node. The data transfers plus the required flow control and target node page-table management are also supported. The transaction layer parses the ORBs to extract the CDBs and presents them to the microcontroller. The microcontroller returns status indication to the transaction layer: the SBP-2 engine then returns this information plus the transaction status information to the logged-in node.

The SAA7356HL will present all Configuration-ROM reads to the microcontroller. The microcontroller will return the requested information. The SAA7356HL will then add the required header for the 1394 transaction to service these requests.

7.3 DMA interface

The SAA7356HL supports many formats of DMA interface. The DMA bus width may be 8 or 16 bits wide. The polarity of the request, acknowledge, read and write strobes can be configured for active HIGH or active LOW. The DMA controller may also be configured as a master or a slave. In the slave mode, the burst length can also be configured. All configuration details are loaded into the SAA7356HL via a shared page in the Static Random Access Memory (SRAM).

In slave mode a buffer data transfer begins when the DMA interface asserts the DMA_REQ pin. The buffer manager responds with the DMA_ACK signal. The burst configuration defines the number of bytes/words to keep DMA_REQ asserted. The settings include:

- DMA_REQ is asserted until the last byte/word is transferred or until there is no space/data available in the FIFO
- DMA_REQ is asserted and negated for each byte/word transferred
- DMA_REQ is not asserted unless there is space/data available in the FIFO
- the DMA interface waits until there are at least two bytes/words of data/space in the FIFO before asserting DMA_REQ (in this case, DMA_REQ remains asserted for the two bus transfers and then de-asserts); and
- the DMA interface waits until there are at least four bytes/words of data/space in the FIFO before asserting DMA_REQ (in this case, DMA_REQ remains asserted for the four bus transfers and then de-asserts).

This process repeats until all of the data is transferred. In slave mode, there are three modes of operation for moving data between the SAA7356HL and the DMA interface:

- Mode 0: DMA_WRITE strobes the data from the buffer memory data bus into the FIFO; DMA_READ gates the data from the FIFO onto the buffer memory data bus
- Mode 1: DMA_WRITE strobes the data from the buffer memory into the FIFO. DMA_ACK gates data from the FIFO onto the buffer memory data bus
- Mode 2: DMA_ACK strobes the data from the buffer memory bus into the FIFO and also gates the data from the FIFO onto the buffer memory data bus.

In slave mode the DMA interface drives the DMA_REQ pin and waits for the buffer manager to acknowledge the request via DMA_ACK as described above. In master mode, the buffer manager drives the DMA_REQ pin and the DMA interface acknowledges the availability of data/space with the DMA_ACK pin.

The read or write strobes are driven by the buffer manager in slave mode, and by the DMA interface in master mode. All mode selections listed above are also valid in master mode, however it should be noted that the burst configuration is not applicable in master mode.

Burst size in master mode is determined by the buffer manager request signal, and DMA interface flow control by the time duration between successive acknowledge assertions or read/write assertions.

In master mode the SAA7356HL appears to be an Advanced Technology Attachment (ATA) host and can be connected to an ATA or Advanced Technology Attachment Packet Interface (ATAPI) peripheral. The SAA7356HL output signal (DMA_REQ) behaves like the acknowledge on the Integrated Drive Electronics (IDE) bus; the input signal (DMA_ACK) behaves like the request line on the IDE bus.

The configuration information is provided via a communication page which is shared between the microcontroller and the SAA7356HL. The connections for the various modes are shown in Figs 4 and 5.

7.4 Microcontroller interface

Because of the high-level protocol support, only ten addresses are required. The user should note that all of the internal SAA7356HL registers are still accessible and so the chip-select line should be used to ensure that the SAA7356HL is not accessed accidentally. The behaviour on accessing these other addresses is not specified.

When used in V851 and H8 modes, the $\overline{\text{MICRO\_WAIT}}$ line is asserted within 4 ns of the $\overline{\text{MICRO\_READ}}$ falling edge.

For all modes of operation, the data bus is the MICRO_DATA bus. The microcontroller interface can be configured for four modes of operation, namely:

- Mode 0: 8-bit addressed Intel 8031 peripheral (multiplexed address/data bus)
- Mode 1: 8-bit addressed Hitachi H8 peripheral (non-multiplexed address and data buses)
- Mode 2: 16-bit addressed Intel 8031 peripheral (lower address from multiplexed address/data bus)
- Mode 3: 16-bit addressed NEC V851 peripheral (acting as an 8-bit peripheral).

7.4.1 INTEL 8031 INTERFACE SUPPORT

The microcontroller interface logic supports the industry standard 8031 style interface.

On reading, the MICRO_DATA output is enabled as soon as the $\overline{\text{MICRO\_READ}}$ is asserted. Before this happens, the address will have already been decoded and the internal Data Out signal asserted. On writing, the data is loaded from the rising edge of $\overline{\text{MICRO\_WRITE}}$.

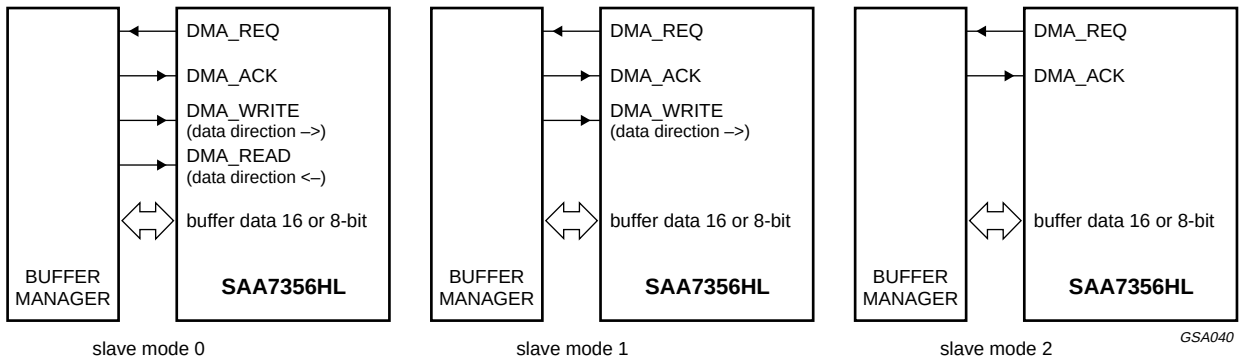


Fig.4 Slave Mode 0, 1 and 2

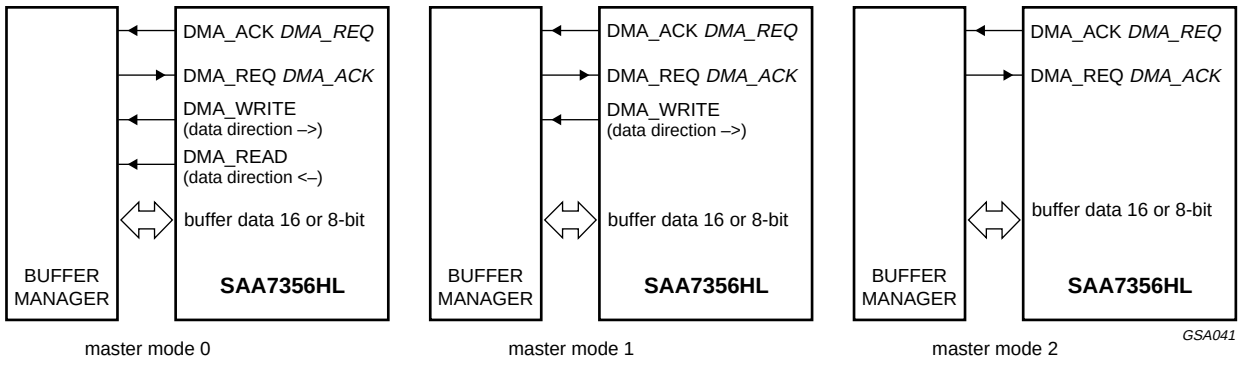


Fig.5 Master Mode 0, 1 and 2.

7.4.2 HITACHI H8 INTERFACE

In this mode, the address and data buses are non-multiplexed. The address bus is connected directly to the MICRO_ADDR pins and the data bus is connected directly onto the MICRO_DATA pins.

The $\overline{\text{MICRO\_CS}}$ pin must be asserted before the assertion of the $\overline{\text{MICRO\_READ}}$ pin. The SAA7356HL will stop driving the microcontroller data bus when either the $\overline{\text{MICRO\_CS}}$ pin or the $\overline{\text{MICRO\_READ}}$ pin are negated.

The H8 microcontroller supports wait states. The timing is shown in Fig.6. Note that the $\overline{\text{MICRO\_WAIT}}$ pin must be low during the falling edge of the (H8) CLK during state T2. Since the relationship between the SAA7356HL and the H8 clock is unknown the $\overline{\text{MICRO\_WAIT}}$ pin is asserted low when the $\overline{\text{MICRO\_READ}}$ and the $\overline{\text{MICRO\_CS}}$ are asserted. The SAA7356HL will de-assert the $\overline{\text{MICRO\_WAIT}}$ line once the data is ready for transfer.

7.4.3 NEC V851 INTERFACE SUPPORT

The most important timing information for this microcontroller is given in Fig.7.

The $\overline{\text{MICRO\_WAIT}}$ line must be low during the falling edge of the (V851) CLK during state T2: this is the same requirement as the H8. Instead of a $\overline{\text{MICRO\_READ}}$ and a $\overline{\text{MICRO\_WRITE}}$ signal the V851 uses a R/$\overline{\text{W}}$ and DSTB signal. The address lines are time multiplexed and should be latched using the ASTB signal.

7.5 Interrupt handling

The SAA7356HL may use interrupts to communicate with the microcontroller. The microcontroller will read from the **CmdToMicro** register to find the interrupt reason.
If parameters are required with the command then this is implied in the command byte.These parameters may then be read from the SAA7356HL RAM using the **RAM.Offset** and the **RAM.Next** registers.

7.6 Address map for the SAA7356HL

The address mapping for the 4-bit, 8-bit and 16-bit addressing modes is given in Table 1.

Table 1 Big-endian register map for the SAA7356HL

ADDRESS			MNEMONIC	COMMENT
4-BIT	**8-BIT**	**16-BIT**		
0	9C	FF90	Reserved	reserved
1	9D	FF91	InterruptEnable	enables the **InterruptReason** to assert the microcontroller interrupt line
2	9E	FF92	InterruptReason	provides the interrupt sources
3	9F	FF93	CmdFromMicro	command byte channel from the microcontroller to the SAA7356HL
4	BC	FFB0	CmdToMicro	command byte from the SAA7356HL to the microcontroller
5	BD	FFB1	Sbp2Start	used to complete the SAA7356HL initialization sequence
6	BE	FFB2	InterruptSet	allows setting of the flags in the **InterruptReason** register
7 to B	BF, DC to DF	FFB3, FFD0 to FFD3	Reserved	reserved
C	FC	FFF0	RAM.OffsetB	High-byte of the offset address
D	FD	FFF1	RAM.OffsetA	Low-byte for the offset address
E	FE	FFF2	RAM.Next	RAM access register: forces a post-increment of the **RAM.Offset** address
F	FF	FFF3	RAM.Current	RAM access register: no modification to the **RAM.Offset** address

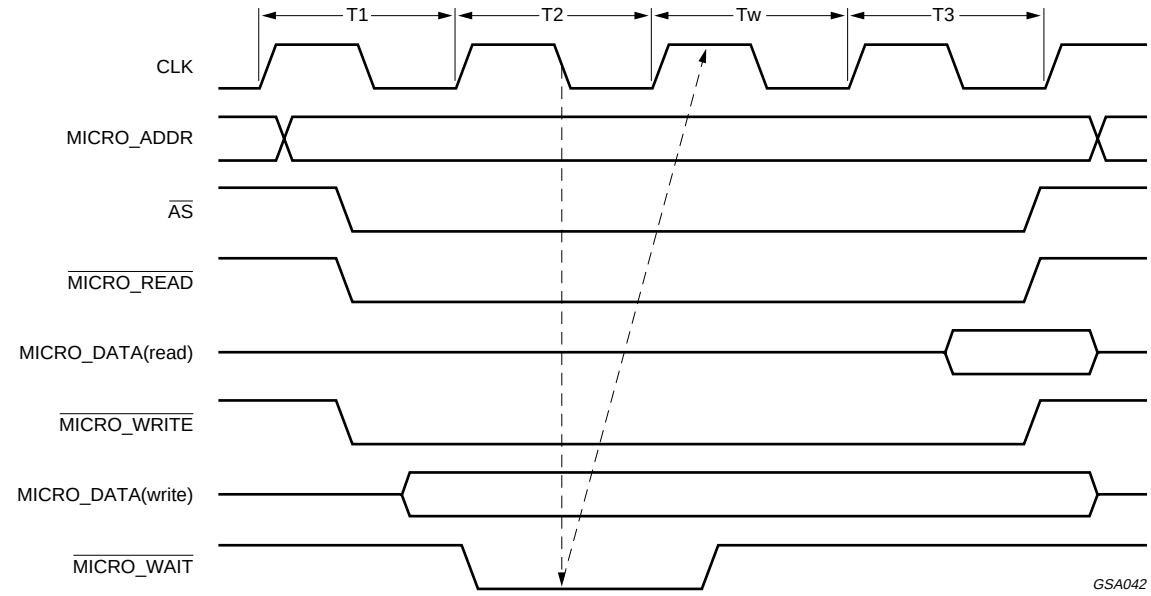


Fig.6 H8 microcontroller interface timing.

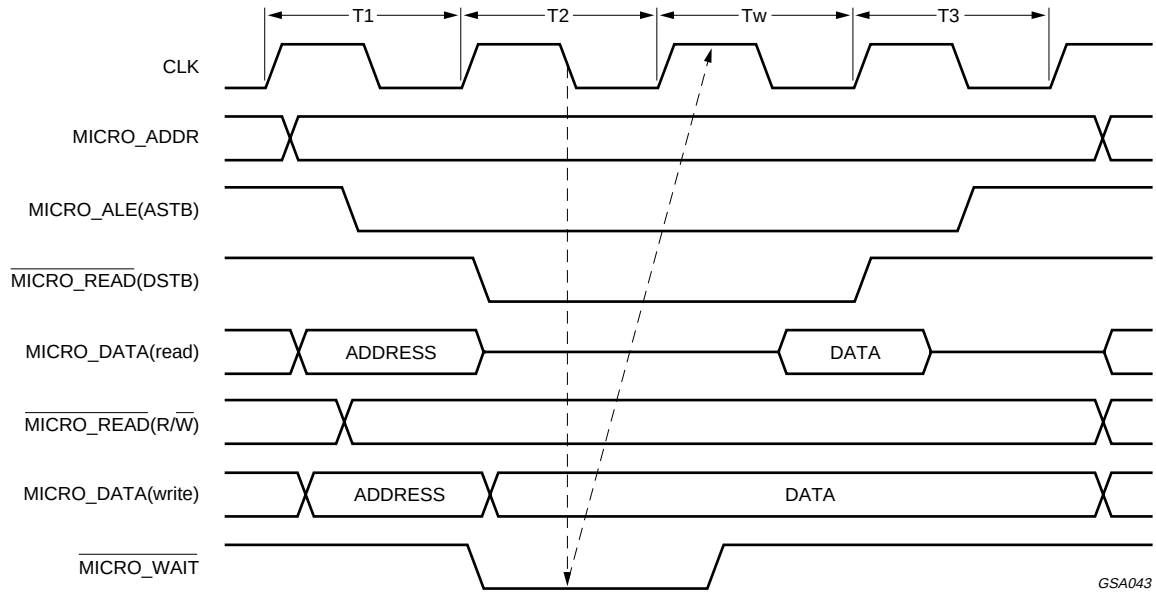


Fig.7 V851 microcontroller interface timing.

8 MICROCONTROLLER COMMUNICATION WITH THE SAA7356HL

The communications protocol from a hardware perspective is described in the following sections.

The automation engine within the SAA7356HL performs all of the functions necessary to support the SBP-2 protocol layer. The microcontroller and the SAA7356HL communicate via command registers and access to the shared RAM resource.

The microcontroller will download the configuration information into the SAA7356HL after a Power-on reset. Once this has been done, the power-on sequence will be completed when the microcontroller writes any value to the **Sbp2Start** register. To download the configuration information, the microcontroller simply copies a binary image (provided by Philips Semiconductors) and writes repetitively into the **RAM.Next** address.

8.1 Communications initiated by the microcontroller

The microcontroller may send a message to the SAA7356HL by writing to the **CmdFromMicro** register. Once the SAA7356HL has used this register, the SAA7356HL will assert the maskable interrupt, **InterruptReason.CmdClr**, to the microcontroller. The value in the **CmdFromMicro** register will remain. On receiving the **InterruptReason.CmdClr** interrupt, the microcontroller will read from the **InterruptReason** register to determine the source of this interrupt. To clear the interrupt, the microcontroller must write a logic 1 to the **InterruptReason.CmdClr** bit: writing a logic 0 to this location has no effect. An alternative control protocol may be used. As the SAA7356HL acknowledges the **CmdFromMicro**, the **InterruptReason.CmdClr** is asserted as before. The user may decide to mask this interrupt and use a polling technique.

On detecting completion of the previous command via **InterruptReason.CmdClr**, the microcontroller may write another command into the **CmdFromMicro** register: this will clear the **InterruptReason.CmdClr** flag and so there is no need for the microcontroller to perform another operation to explicitly clear this flag.

This style of communication is used to realize a simple command-driven communication protocol in which the microcontroller sends command bytes to the SAA7356HL. If no parameters are required, there is no need to write to a shared memory location and hence there is no need to write to the RAM Access **Offset**, **Current** and **Next** registers. The **CmdFromMicro** register definition is given in Table 2.

In addition to the **CmdFromMicro** register, the microcontroller can also write to the **Sbp2Start** register. This is used in the system initialization sequence. The value that is written has no significance and reading from this address will return zeros.

When using this command to initialize the SAA7356HL, the microcontroller may first write to a pre-designated memory area for the parameter passing and then write to the **Sbp2Start** register to start the requested action. The **Sbp2Start** register definition is given in Table 3.

8.2 Communications initiated by the SAA7356HL

The SAA7356HL has only one form of communication to the microcontroller: the SAA7356HL will write to the **CmdToMicro** register. On writing to this register, the maskable **CmdMicro** bit in the **InterruptReason** register is asserted, which in turn may assert the maskable interrupt to the microcontroller. The microcontroller will read from the **InterruptReason** register to determine the cause of the interrupt. If no data is required from the communication then the microcontroller can determine this from the value in the **CmdToMicro** register. The **CmdToMicro** register definition is given in Table 4.

If data or parameters are needed then the SAA7356HL will first write to the RAM and then write to the **CmdToMicro** register. To signal acknowledgment of the interrupt, the microcontroller writes a logic 1 to the **CmdMicro** bit in the **InterruptReason** register which also has the effect of clearing the **CmdMicro** bit and negating the interrupt (if no other interrupts are pending): writing a logic 0 to the **CmdMicro** bit has no effect. On signalling the acknowledgment, the value in the **CmdToMicro** register is unchanged, but now the SAA7356HL is free to modify the **CmdToMicro** register contents.

Table 2 CmdFromMicro register definition (read/write)

BYTE NUMBER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Command(7:0)							

Table 3 Sbp2Start register definition (read/write)

BYTE NUMBER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Command(7:0)							

Table 4 CmdToMicro register definition (read/write)

BYTE NUMBER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Command(7:0)							

8.3 Interrupt registers

As mentioned in the previous section, the communications may be interrupt driven. To facilitate this there is one **InterruptReason** and one **InterruptEnable** register. The interrupt to the microcontroller is of the AND-OR type and is asserted when any of the maskable interrupts are enabled and active: to enable an interrupt, the corresponding field in the **InterruptEnable** register must be set to logic 1. Reading from the **InterruptReason** register provides the un-masked value: this allows polling if desired.

The **InterruptEnable** and **InterruptReason** register definitions are shown in Tables 5 and 6 respectively.

In addition to these two registers, the microcontroller may set the values in the **InterruptReason** register: this may be used for setting initial conditions, for example. To set the required bits, a logic 1 must be written to the flag location in the **InterruptSet** register: writing a logic 0 to any bit-field has no effect. The **InterruptSet** register definition is given in Table 7.

It is recommended that only the **InterruptReason.CmdClr** flag is set as **InterruptReason.CmdMicro** will cause a maskable interrupt to be asserted to the microcontroller.

The definition of the **InterruptReason**, **InterruptEnable** and the **InterruptSet** register fields are shown in Table 8.

Table 5 InterruptEnable register definition (read/write)

BYTE NUMBER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Reserved					CmdMicro	BusReset	CmdClr

Table 6 InterruptReason register definition (read/write)

BYTE NUMBER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Reserved					CmdMicro	BusReset	CmdClr

Table 7 InterruptSet register definition (write only, read via InteruptReason)

BYTE NUMBER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Reserved					CmdMicro	Reserved	CmdClr

Table 8 Definition of the InterruptReason, InterruptEnable and InterruptSet register fields

MNEMONIC	VALUE	COMMENT
CmdClr	0	default condition: no action occurred
	1	the SAA7356HL device has acknowledged the write to the **CmdFromMicro** register
BusReset	0	default condition: no action occurred
	1	the SAA7356HL has detected a serial bus reset
CmdMicro	0	default condition: no action occurred
	1	the SAA7356HL has written a command into the **CmdToMicro** register
Reserved	X	reserved and set to zero

8.4 RAM access for parameter passing

Within the SAA7356HL there is a 16 kbyte RAM. This is shared between: the IEEE1394 transaction FIFOs, the code for the automation engine and its local storage requirements, and the shared memory area for communications with the microcontroller.

The SAA7356HL user must understand how this shared memory is accessed in order to write and read the communications parameters. Each of the read and write accesses to the FIFOs are byte-wide and the offset addresses are byte offsets.

8.4.1 Register Access

The RAM can be directly accessed to upload the code into the SAA7356HL. The C-structure for the registers for the RAM access is shown below.

```
struct RAM {
U16; offset; // absolute offset into the RAM
U8; next; // read/write data at offset and
post-increment
U8; current; // read/write data at offset
};
```

The **RAM.Offset** field allows the microcontroller to access anywhere within the SAA7356HL RAM. The **RAM.Next** accesses will access the **RAM.Offset** address and post-increment the offset pointer.

Accesses to the **RAM.Current** address allow reads and writes to the data in the **RAM.Offset** location without altering the **RAM.Offset** address.

The ability to write to anywhere within the RAM is used for the power-on sequence.

8.4.2 Register definitions for the register access method

This section defines the register structure for the **RAM** registers.

The **RAM.Offset** registers are used to index into the RAM inside the SAA7356HL. The index is a byte address. The **RAM.Offset** register definition is shown in Table 9.

The **RAM.Next** register is used to read or write to the RAM location addressed by the **RAM.Offset** register. Once an access has been made, the value of the **RAM.Offset** register is incremented to simplify the process of reading or writing contiguous memory areas. The **RAM.Next** register definition is shown in Table 10.

The **RAM.Current** register is used to read or write to the RAM location addressed by the **RAM.Offset** register. Once an access has been made there is no change to the **RAM.Offset** register. The **RAM.Current** register definition is shown in Table 11.

Table 9 Definition of the RAM.Offset registers (read/write)

BYTE NUMBER	BIT 7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RAM.Offset(7:0)							
1	Reserved		RAM.Offset (13:8)					

Table 10 Definition of the RAM.Next register (read/write)

BYTE NUMBER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RAM.Next(7:0)							

Table 11 Definition of the RAM.Current register (read/write)

BYTE NUMBER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RAM.Current(7:0)							

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to ground (ground = 0 V); notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+4.0	V
I_{IK}	input clamping diode current		–	–50	mA
V_I	input voltage	microcontroller and DMA pins	–0.5	+5.5	V
		PHY pins	–	V_{DD} + 0.5	V
I_{OK}	output clamping diode current		–	±50	mA
V_O	output voltage		–0.5	V_{DD} + 0.5	V
$I_{O(source)}$	output source current		–	±150	mA
$I_{O(sink)}$	output sink current		–	±150	mA
$I_{SS} - I_{CC}$	V_{CC} or GND current		–	±150	mA
T_{stg}	storage temperature		–60	+150	°C
T_{amb}	ambient temperature		0	70	°C
P_{tot}	total power dissipation	package	–	380	mW
		comma mode	–	82	μW

Notes

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in “Recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 ^{o}C.

10 RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		3.0	3.6	V
V_I	input voltage	microcontroller and DMA pins	0	5.5	V
		PHY pins	0	3.6	V
V_{IH}	HIGH-level input voltage		2.0	–	V
V_{IL}	LOW-level input voltage		–	0.8	V
I_{OH}	HIGH-level output current		–	4	mA
I_{OL}	LOW-level output current		–	–4	mA
$\Delta t_{t(i)(r)}/\Delta V$	input transition rise time		0	20	ns/V
$\Delta t_{t(i)f)}/\Delta V$	input transition fall time		0	20	ns/V
T_{amb}	ambient temperature		0	70	°C
SCLK	system clock		49.147	49.157	MHz
$t_{i(r)}$	input rise time		–	10	ns
$t_{i(f)}$	input fall time		–	10	ns

11 DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	note 1	2.4	–	–	V
V_{IL}	LOW-level input voltage	note 1	–	–	0.8	V
$V_{I(th)(r)}$	input voltage threshold, rising edge	note 2	$0.5V_{DD}$ + 0.12	–	$0.5V_{DD}$ + 0.66	V
$V_{I(th)(f)}$	input voltage threshold, falling edge	note 2	$0.5V_{DD}$ – 0.66	–	$0.5V_{DD}$ – 0.12	V
V_{OH1}	HIGH-level output voltage 1	note 1	2.4	–	–	V
V_{OL1}	LOW-level output voltage 1	note 1	-	–	0.4	V
V_{OH2}	HIGH-level output voltage 2	note 3	2.9	–	–	V
V_{OL2}	LOW-level output voltage 2	note 3	–	–	0.4	V
I_{IL}	input leakage current	note 1	–	–	±1	μA
		note 4	–	–	100	μA
I_{OZ}	3-state output current	note 5	–	–	±5	μA
		note 3	–	–	200	μA
I_{DD}	active supply current	V_{DD} = 3.3 V; note 6	–	–	–	mA

Notes

1. Microcontroller and DMA interface pins.
2. PHY-Link data and control and PHY_SCLK pins.
3. PHY-Link data and control pins.
4. PHY_SCLK pin.
5. Microcontroller, DMA and PHY_LREQ pins.
6. Under idle conditions the average value is 108 mA.

12 AC CHARACTERISTICS

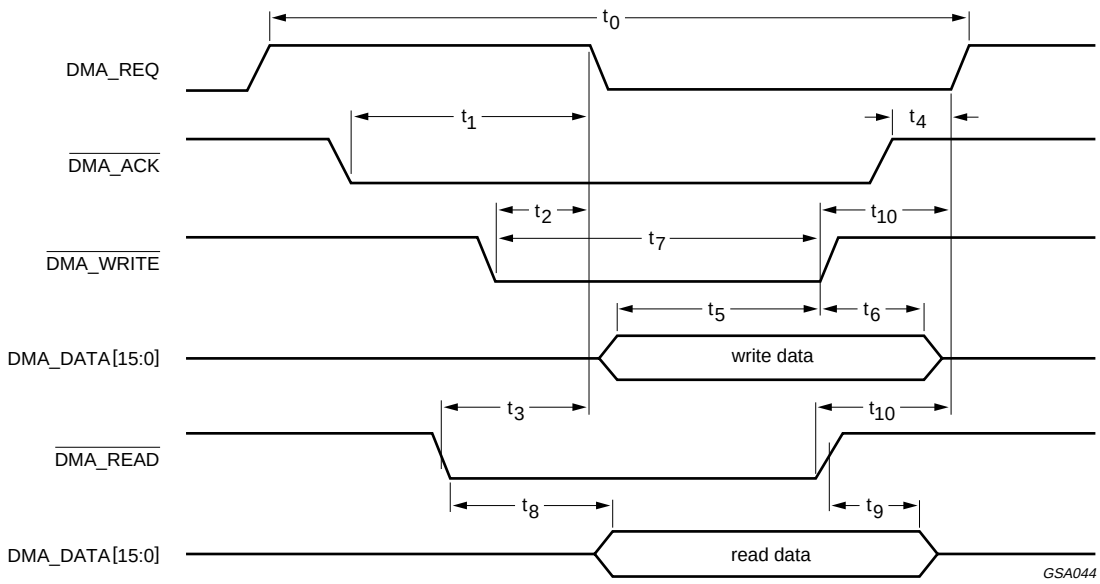
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DMA INTERFACE WRITE/READ TIMING FOR SLAVE MODE 0; see Fig.8						
t_0	cycle time		67	–	–	ns
t_1	DMA_REQ de-assert from $\overline{\text{DMA\_ACK}}$ assert (single word DMA)		–	–	25	ns
t_2	DMA_REQ de-assert from $\overline{\text{DMA\_WRITE}}$ assert (multi-word DMA)		–	–	25	ns
t_3	DMA_REQ de-assert from $\overline{\text{DMA\_READ}}$ assert (multi-word DMA)		–	–	25	ns
t_4	DMA_REQ assert after $\overline{\text{DMA\_ACK}}$ de-assert		8	–	–	ns
t_5	write data set-up		15	–	–	ns
t_6	write data hold		5	–	–	ns
t_7	$\overline{\text{DMA\_WRITE}}$ active pulse duration		25	–	–	ns
t_8	read data stable after $\overline{\text{DMA\_READ}}$ active		–	–	10	ns
t_9	read data 3-state after $\overline{\text{DMA\_READ}}$ inactive		5	–	10	ns
t_{10}	DMA_REQ assert after $\overline{\text{DMA\_READ}}$ and $\overline{\text{DMA\_WRITE}}$ negated		68	–	–	ns
DMA INTERFACE WRITE/READ TIMING FOR SLAVE MODE 1; see Fig.9						
t_0	cycle time		67	–	–	ns
t_1	DMA_REQ de-assert from $\overline{\text{DMA\_ACK}}$ assert (single word DMA)		–	–	25	ns
t_2	DMA_REQ de-assert from $\overline{\text{DMA\_WRITE}}$ assert (multi-word DMA)		–	–	25	ns
t_3	DMA_REQ assert after $\overline{\text{DMA\_ACK}}$ de-assert		5	–	–	ns
t_4	read data stable after $\overline{\text{DMA\_ACK}}$ assert		–	–	10	ns
t_5	read data 3-state after $\overline{\text{DMA\_ACK}}$ inactive		5	–	10	ns
t_6	write data set-up		15	–	–	ns
t_7	write data hold		5	–	–	ns
t_8	$\overline{\text{DMA\_WRITE}}$ active pulse width		25	–	–	ns
DMA INTERFACE WRITE/READ TIMING FOR SLAVE MODE 2; see Fig.10						
t_0	cycle time		67	–	–	ns
t_1	DMA_REQ de-assert from $\overline{\text{DMA\_ACK}}$ assert (single word DMA)		–	–	25	ns
t_2	DMA_REQ assert after $\overline{\text{DMA\_ACK}}$ de-assert		5	–	–	ns
t_3	write data set-up		15	–	–	ns
t_4	write data hold		5	–	–	ns
t_5	$\overline{\text{DMA\_ACK}}$ active pulse duration during data write		25	–	–	ns
t_6	read data stable after $\overline{\text{DMA\_ACK}}$ assert		–	–	10	ns
t_7	read data 3-state after $\overline{\text{DMA\_ACK}}$ de-assert		5	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DMA INTERFACE WRITE/READ TIMING FOR MASTER MODE 0; note 1; see Fig.11						
t_0	cycle time		40	–	–	ns
t_1	DMA_REQ de-assert from $\overline{\text{DMA\_ACK}}$ assert (single word DMA)		–	–	30	ns
t_2	DMA_REQ de-assert from $\overline{\text{DMA\_WRITE}}$ assert (multi-word DMA)		–	–	30	ns
t_3	DMA_REQ de-assert from $\overline{\text{DMA\_READ}}$ assert (multi-word DMA)		–	–	30	ns
t_4	DMA_REQ assert after $\overline{\text{DMA\_ACK}}$ de-assert		0	–	–	ns
t_5	write data set-up		20	–	–	ns
t_6	write data hold		0	–	–	ns
t_7	$\overline{\text{DMA\_WRITE}}$ active pulse duration		20	–	–	ns
t_8	read data stable after $\overline{\text{DMA\_READ}}$ active		–	–	15	ns
t_9	read data 3-state after $\overline{\text{DMA\_READ}}$ inactive		25	–	30	ns
t_{10}	$\overline{\text{DMA\_WRITE}}$ active pulse duration		20	–	–	ns
DMA INTERFACE WRITE/READ TIMING FOR MASTER MODE 1; note 1; see Fig.12						
t_0	cycle time		40	–	–	ns
t_1	DMA_REQ de-assert from $\overline{\text{DMA\_ACK}}$ assert (single word DMA)		–	–	30	ns
t_2	DMA_REQ de-assert from $\overline{\text{DMA\_WRITE}}$ assert (multi-word DMA)		–	–	30	ns
t_3	DMA_REQ assert after $\overline{\text{DMA\_ACK}}$ de-assert		0	–	–	ns
t_4	read data stable after $\overline{\text{DMA\_ACK}}$ assert		–	–	15	ns
t_5	read data 3-state after $\overline{\text{DMA\_ACK}}$ inactive		25	–	30	ns
t_6	write data set-up		20	–	–	ns
t_7	write data hold		0	–	–	ns
t_8	$\overline{\text{DMA\_WRITE}}$ active pulse width		20	–	–	ns
t_9	$\overline{\text{DMA\_ACK}}$ active pulse width		20	–	–	ns
DMA INTERFACE WRITE/READ TIMING FOR MASTER MODE 2; note 1; see Fig.13						
t_0	cycle time		40	–	–	ns
t_1	DMA_REQ de-assert from $\overline{\text{DMA\_ACK}}$ assert (single word DMA)		–	–	30	ns
t_2	DMA_REQ assert after $\overline{\text{DMA\_ACK}}$ de-assert		0	–	–	ns
t_3	write data set-up		20	–	–	ns
t_4	write data hold		0	–	–	ns
t_5	$\overline{\text{DMA\_ACK}}$ active pulse duration during data write		20	–	–	ns
t_6	read data stable after $\overline{\text{DMA\_ACK}}$ assert		–	–	15	ns
t_7	read data 3-state after $\overline{\text{DMA\_ACK}}$ de-assert		25	–	30	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PHY-LINK INTERFACE TIMING; see Figs 14 and 15						
t_1	PHY-Link set-up time		6	–	–	ns
t_2	PHY-Link hold time		0	–	–	ns
t_3	PHY-Link output delay		2	–	10	ns
REGISTER INTERFACE TIMING; see Figs 16, 17, 18, 19, 20, 21 and 22						
t_1	address set-up to MICRO_ALE LOW		10	–	–	ns
t_2	address hold from MICRO_ALE LOW		10	–	–	ns
t_3	MICRO_ALE pulse width	note 2	20	–	–	ns
t_4	MICRO_ALE LOW to $\overline{\text{MICRO\_CS}}$ LOW		10	–	–	ns
t_5	$\overline{\text{MICRO\_CS}}$ LOW to data valid	note 3	–	–	280	ns
t_6	$\overline{\text{MICRO\_CS}}$ HIGH to MICRO_ALE HIGH		0	–	–	ns
t_7	$\overline{\text{MICRO\_CS}}$ set-up to $\overline{\text{MICRO\_READ}}$ LOW	note 4	0	–	–	ns
t_8	$\overline{\text{MICRO\_READ}}$ pulse width	note 5	280	–	–	ns
t_9	$\overline{\text{MICRO\_READ}}$ HIGH to $\overline{\text{MICRO\_CS}}$ HIGH	note 4	0	–	–	ns
t_{10}	$\overline{\text{MICRO\_READ}}$ LOW to data valid	note 6	–	–	280	ns
t_{11}	$\overline{\text{MICRO\_READ}}$ HIGH to data bus disable		2	–	30	ns
t_{12}	$\overline{\text{MICRO\_CS}}$ set-up to $\overline{\text{MICRO\_WRITE}}$ LOW	note 7	0	–	–	ns
t_{13}	$\overline{\text{MICRO\_WRITE}}$ pulse width		30	–	–	ns
t_{14}	$\overline{\text{MICRO\_WRITE}}$ HIGH to $\overline{\text{MICRO\_CS}}$ HIGH	note 7	0	–	–	ns
t_{15}	data set-up to $\overline{\text{MICRO\_WRITE}}$ HIGH		15	–	–	ns
t_{16}	data hold from $\overline{\text{MICRO\_WRITE}}$ HIGH		4	–	–	ns
t_{17}	$\overline{\text{MICRO\_WRITE}}$ HIGH to MICRO_ALE HIGH	note 8	t_{CP} + 5	–	–	ns
t_{18}	$\overline{\text{MICRO\_WRITE}}$ HIGH to $\overline{\text{MICRO\_WRITE}}$ HIGH	note 9	280	–	–	ns
		note 10	460	–	–	ns
t_{19}	$\overline{\text{MICRO\_READ}}$ LOW to $\overline{\text{MICRO\_WAIT}}$ LOW		–	–	4	ns
t_{20}	data valid to $\overline{\text{MICRO\_WAIT}}$ HIGH		–	–	20	ns

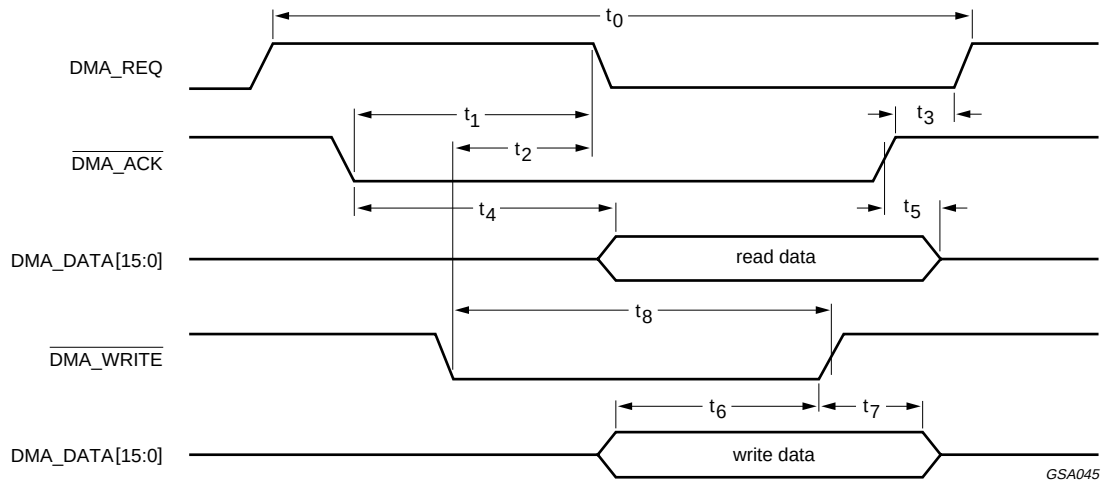
Notes

1. ATA Multi-word Direct Memory Access (MDMA) protocol with all timing based on an internal DMA interface 50 MHz system clock.
2. MICRO_ALE must pulse to capture a new register address for the Intel 8031 and the NEC V851 modes.
3. t_{10} must also be satisfied.
4. If $\overline{\text{MICRO\_READ}}$ is held LOW, the time from $\overline{\text{MICRO\_CS}}$ LOW to stable data is t_5 and the data release time from $\overline{\text{MICRO\_CS}}$ HIGH is t_{11}.
5. This is larger than the typical read strobe timing. To meet these requirements, either the microcontroller clock will be stopped by the buffer manager device, or the microcontroller must insert its own wait states.
6. t_5 must also be satisfied.
7. If $\overline{\text{MICRO\_WRITE}}$ is held LOW, data set-up to $\overline{\text{MICRO\_CS}}$ HIGH is t_{15} and data hold from $\overline{\text{MICRO\_CS}}$ is t_{16}.
8. t_3 minimum = $2 \times 3t_{CP}$ + 5 for successive FIFO reads or a FIFO read or write followed by a read of the FIFO flag registers.
9. This time relates to accesses to addresses other than **RAM.Next** and **RAM.Current**.
10. This time relates to accesses to the addresses **RAM.Next** and **RAM.Current**.



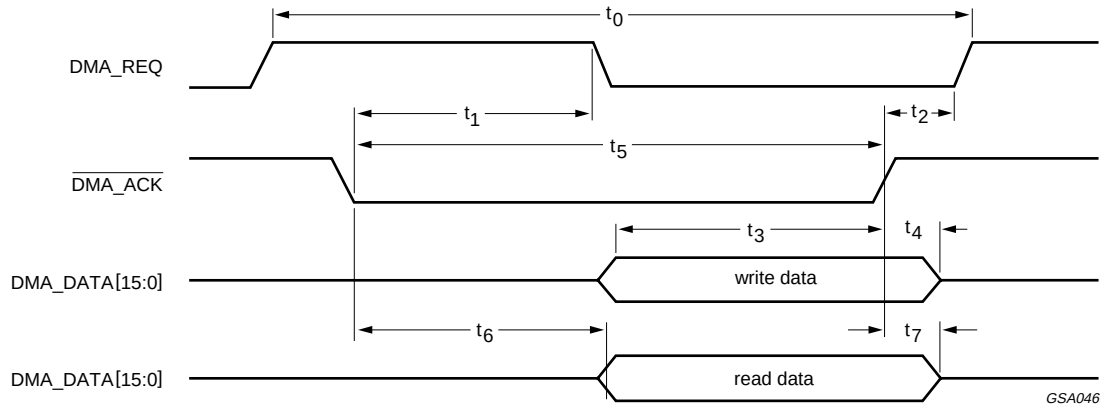
DMA_REQ is configured active HIGH.
DMA_ACK, DMA_WRITE and DMA_READ are configured active LOW.

Fig.8 DMA interface write/read timing diagram for slave mode 0.



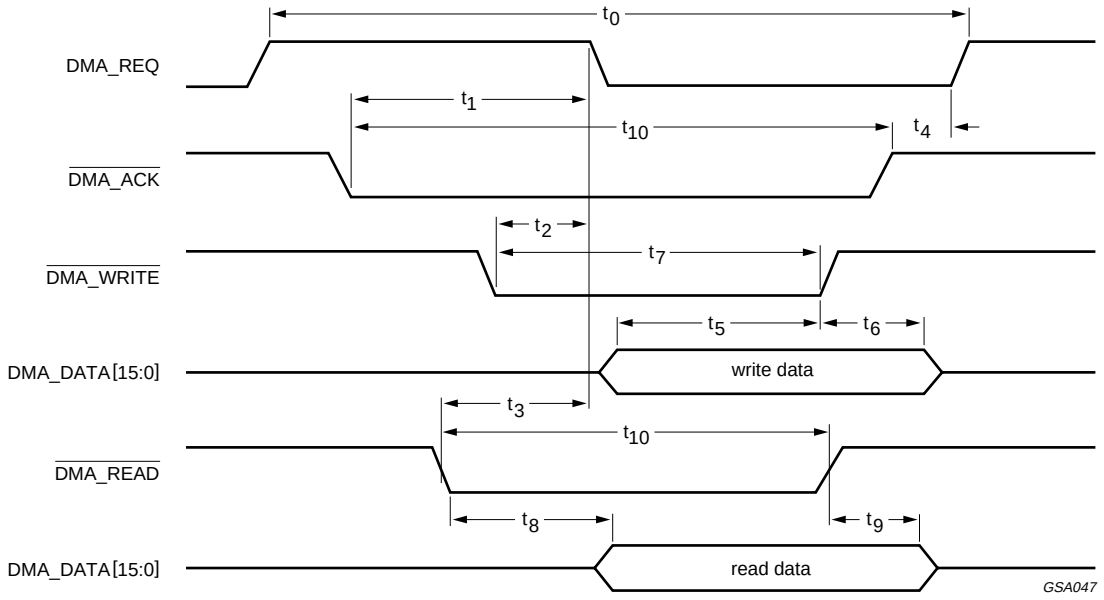
DMA_REQ is configured active HIGH.
DMA_ACK, DMA_WRITE and DMA_READ are configured active LOW.

Fig.9 DMA interface write/read timing diagram for slave mode 1.



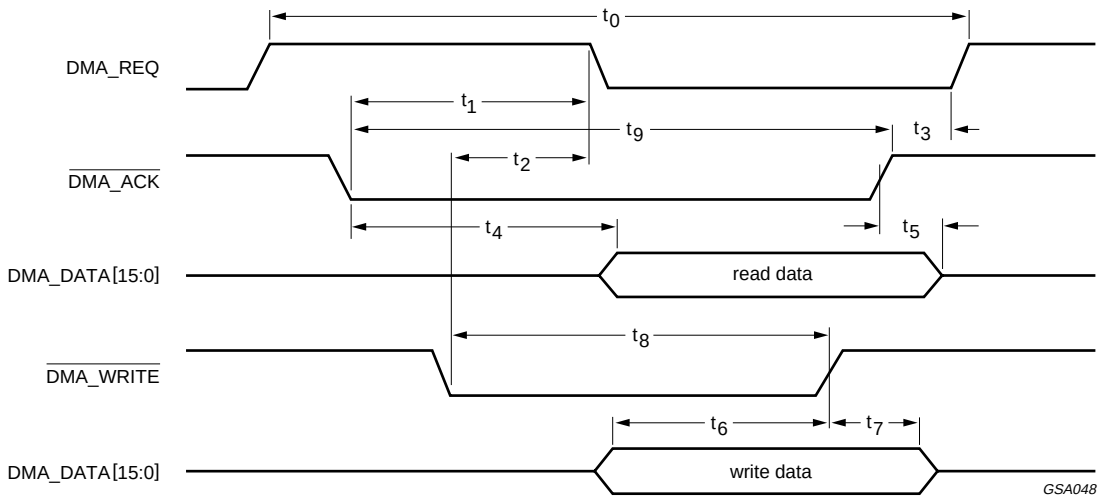
DMA_REQ is configured active HIGH.
DMA_ACK is configured active LOW.

Fig.10 DMA interface write/read timing diagram for slave mode 2.



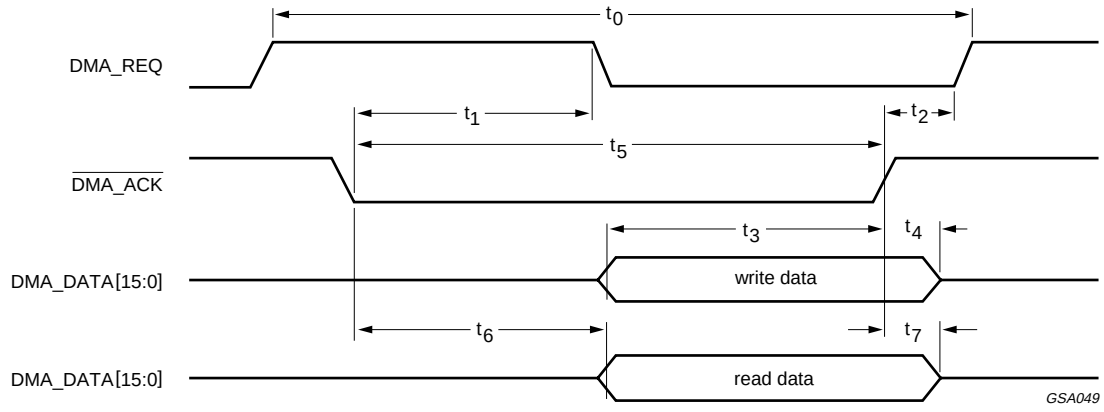
DMA_REQ is configured active HIGH.
DMA_ACK, DMA_WRITE and DMA_READ are configured active LOW.

Fig.11 DMA interface write/read timing diagram for master mode 0.



DMA_REQ is configured active HIGH.
$\overline{\text{DMA\_ACK}}$ and $\overline{\text{DMA\_WRITE}}$ are configured active LOW.

Fig.12 DMA interface write/read timing diagram for master mode 1.



DMA_REQ is configured active HIGH.
$\overline{\text{DMA\_ACK}}$ is configured active LOW.

Fig.13 DMA interface write/read timing diagram for master mode 2.

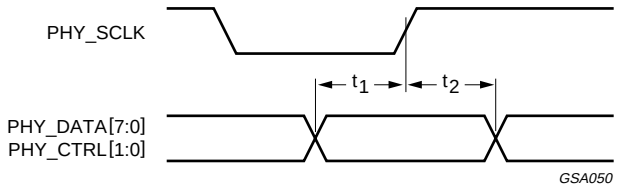


Fig.14 Data and control input set-up and hold timing waveforms.

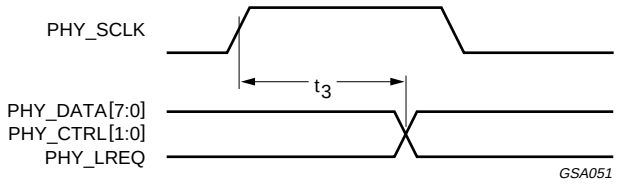


Fig.15 Data, control and PHY_LREQ output delay timing waveforms.

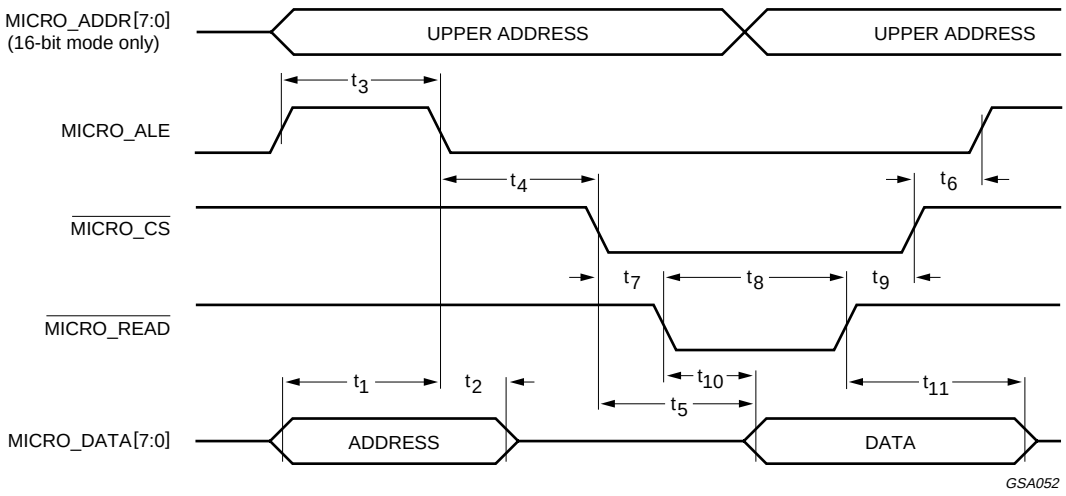


Fig.16 8 or 16-bit addressed 8031 register read timing diagram.

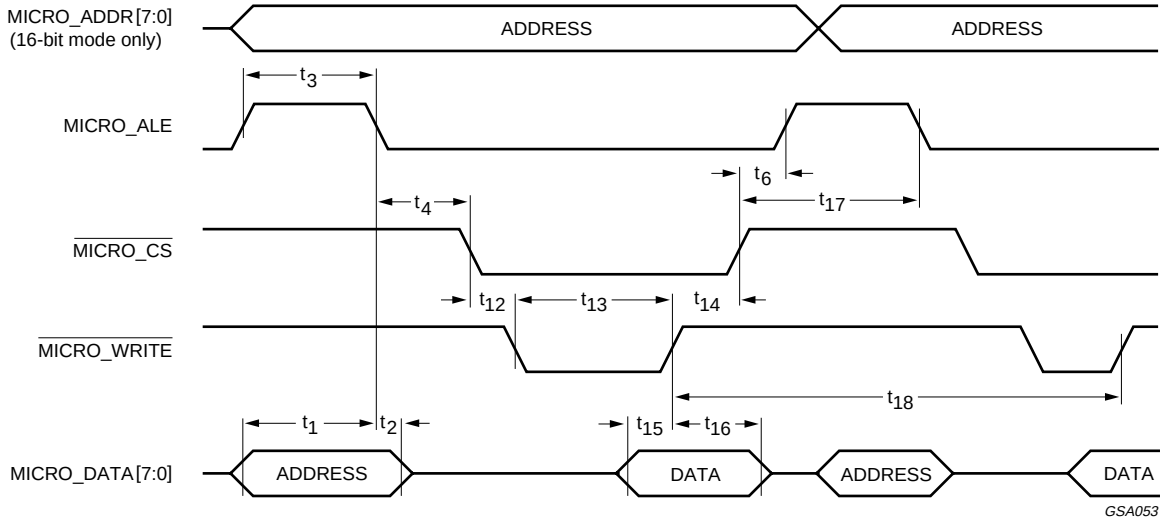


Fig.17 8 or 16-bit addressed 8031 register write timing diagram.

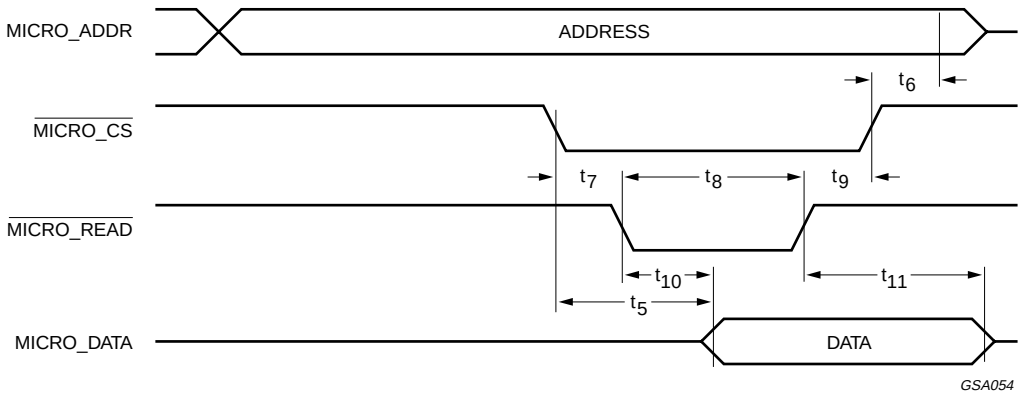


Fig.18 8-bit addressed H8 register read timing diagram.

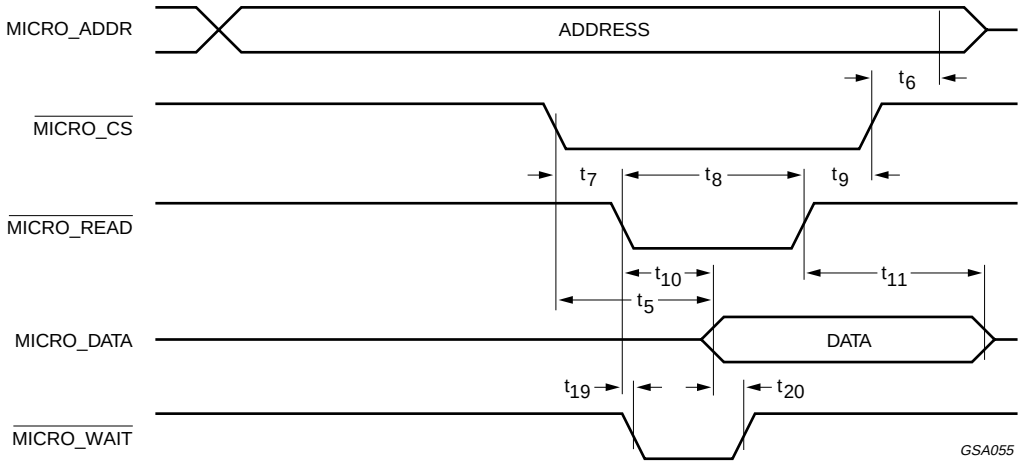


Fig.19 8-bit addressed H8 register read timing diagram with $\overline{\text{MICRO\_WAIT}}$ asserted.

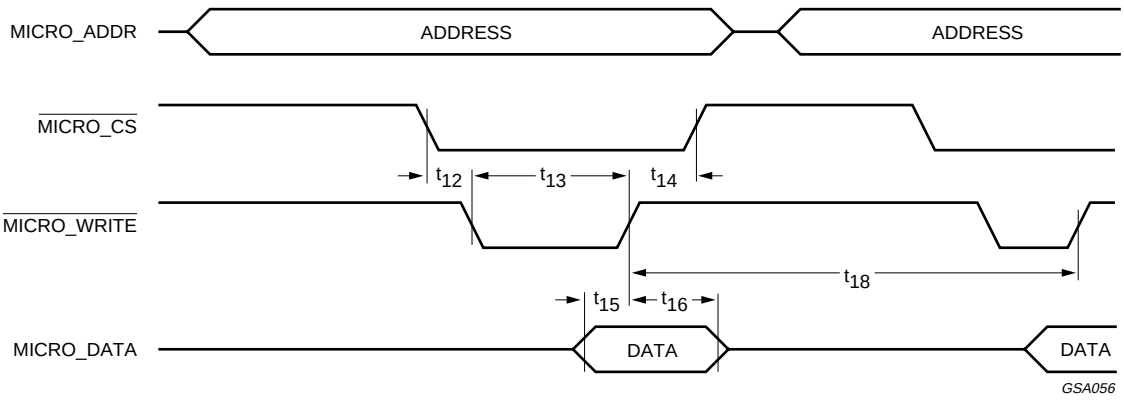


Fig.20 8-bit addressed H8 register write timing diagram.

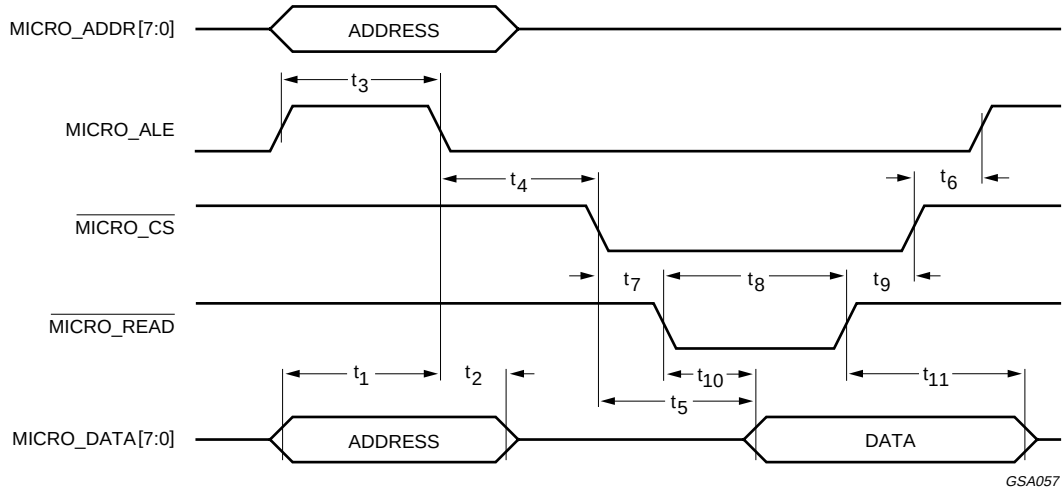


Fig.21 16-bit addressed V851 register read timing diagram.

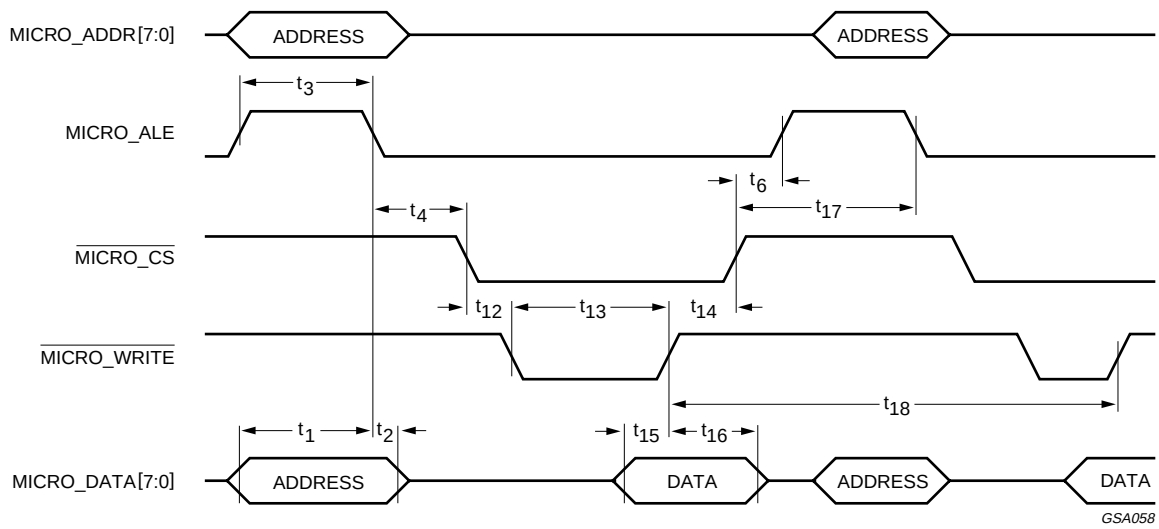


Fig.22 16-bit addressed V851 register write timing diagram.

13 APPLICATION INFORMATION

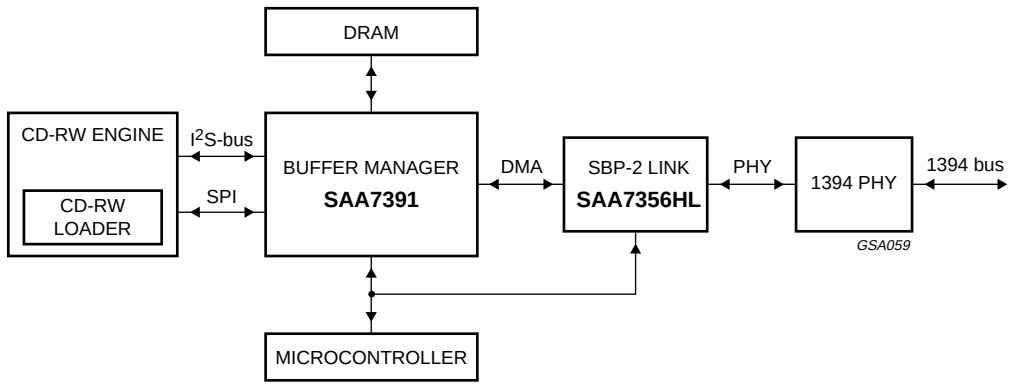
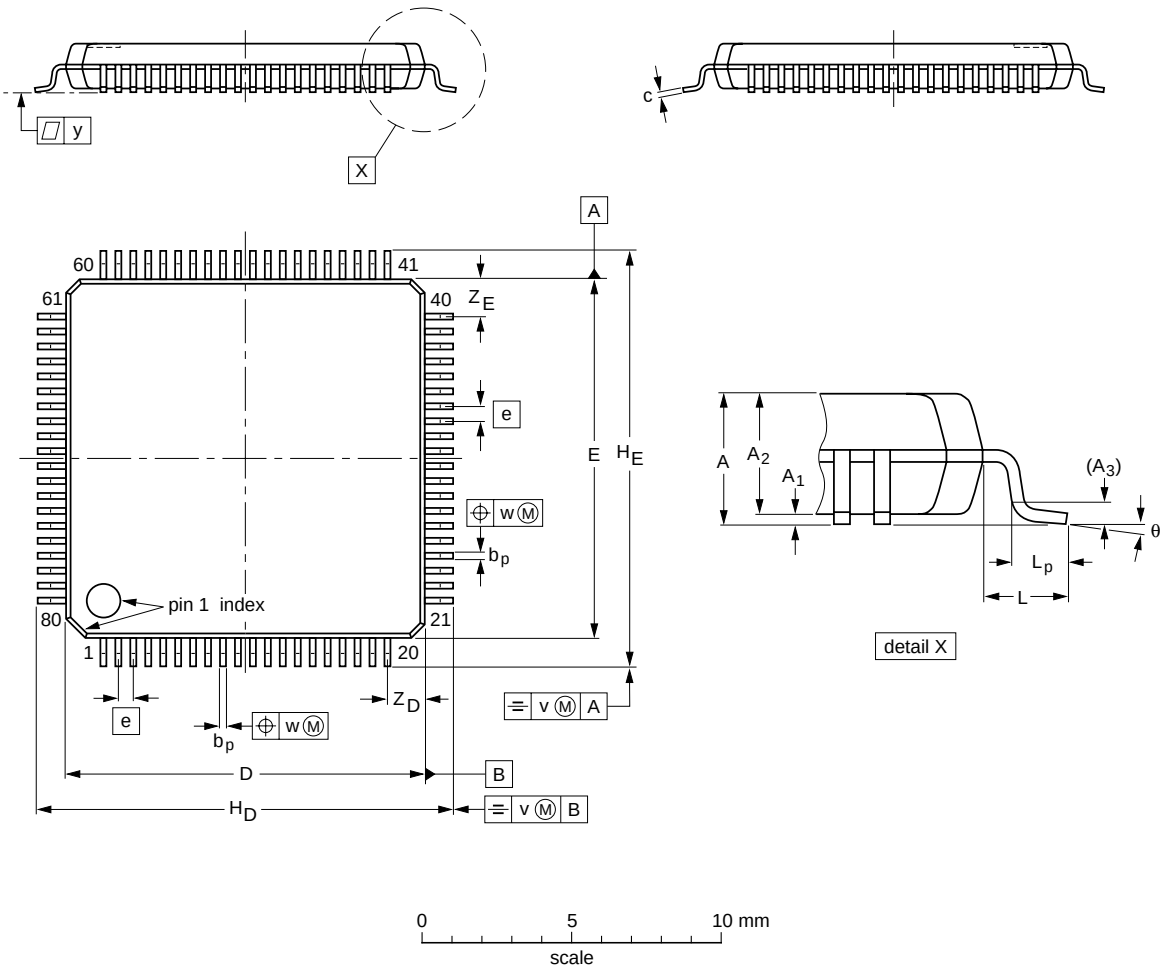


Fig.23 Application diagram.

14 PACKAGE OUTLINE

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1	136E15	MS-026				~~99-12-27~~ 00-01-19

15 SOLDERING

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

16 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

17 DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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