TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT   SILICON MONOLITHIC
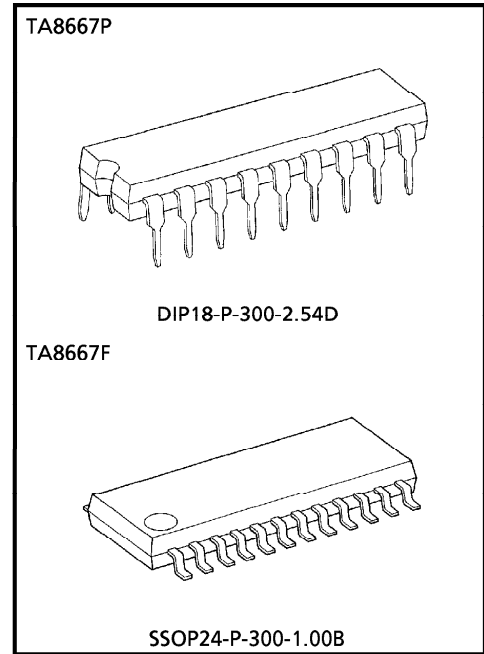
TA8667P, TA8667F

HORIZONTAL AFC IC

The TA8667P, TA8667F is generation of high-frequency clock synchronized with horizontal sync signal.
(The TA8667P/F is H AFC IC for TC9086F (3DYCS), TC9097F (WAC).)
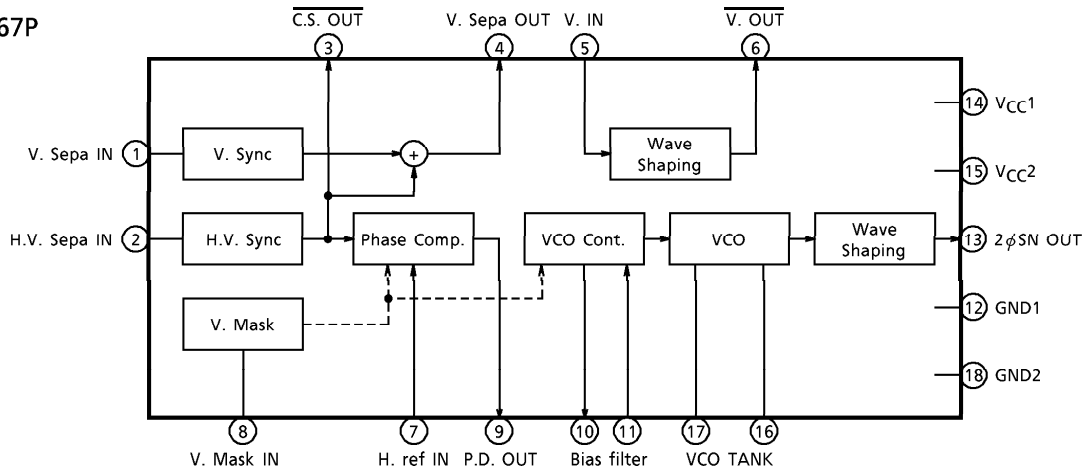
FEATURES

● Generate of Typ. 28MHz (1820fH) clock.

● Generate of vertical sync signal.

● Generate of composite sync signal.

TA8667P

DIP18-P-300-2.54D

TA8667F

SSOP24-P-300-1.00B

Weight
DIP18-P-300-2.54D   : 1.47g (Typ.)
SSOP24-P-300-1.00B : 0.32g (Typ.)

BLOCK DIAGRAM

TA8667P

961001EBA2

TOSHIBA

TERMINAL CONNECTION DIAGRAM

TA8667P

V. Sepa IN ①	⑱ GND2
H.V. Sepa IN ②	⑰ } VCO TANK
C.S. OUT ③	⑯
V. Sepa OUT ④	⑮ $V_{CC}2$
V. IN ⑤	⑭ $V_{CC}1$
V. OUT ⑥	⑬ 2φSN OUT
H. ref IN ⑦	⑫ GND1
V. Mask IN ⑧	⑪ filter
P.D. OUT ⑨	⑩ Bias

TA8667F

V. Sepa IN ①	㉔ GND2
H.V. Sepa IN ②	㉓ } VCO TANK
③	㉒
④	㉑
C.S. OUT ⑤	⑳ $V_{CC}2$
V. Sepa OUT ⑥	⑲ $V_{CC}1$
V. IN ⑦	⑱ 2φSN OUT
V. OUT ⑧	⑰ GND1
⑨	⑯
H. ref IN ⑩	⑮
V. Mask IN ⑪	⑭ filter
P.D. OUT ⑫	⑬ Bias
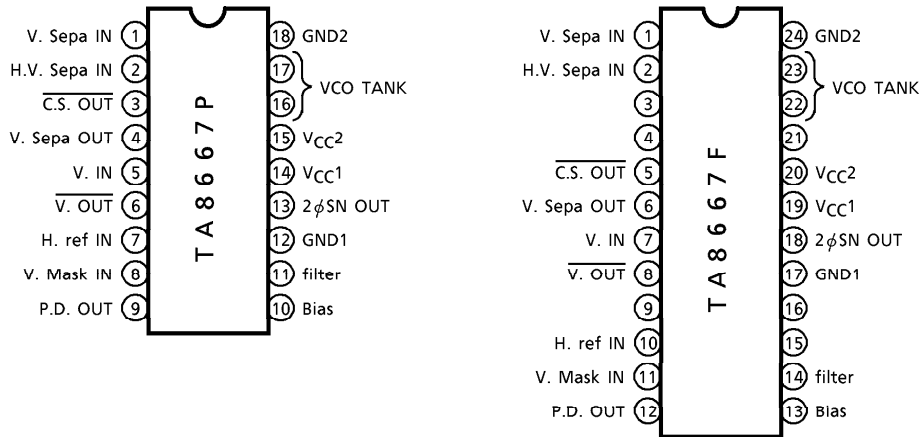
TERMINAL FUNCTION

| TA8667P PIN No.	TA8667F PIN No.	PIN NAME	TYP. DC VOLTAGE	I / O CIRCUIT	FUNCTION
1 2	1 2	V. Sepa IN H.V. Sepa IN	(6.0V)		• V. Sepa IN : Inputs vertical sync signal separated from video signal. • H.V. Sepa IN : Inputs horizontal and vertical sync signals separated from video signal.
3	5	C.S. OUT	—		• Outputs horizontal and vertical sync signals after wave shaping.
4	6	V. Sepa OUT	—		• Outputs vertical sync signal. Horizontal sync signal remains in V. Sepa OUT.

TA8667P PIN No.	TA8667F PIN No.	PIN NAME	TYP. DC VOLTAGE	I/O CIRCUIT	FUNCTION
5	7	V. IN	—		• Inputs the signal outputted from V. Sepa OUT after horizontal sync signal was removed.
6	8	V. OUT	—		• Outputs wave-shaped vertical sync signal.
7	10	H. ref IN	—		• Phase Comp Input. The reference input is the 15.7kHz signal derived through dividing the 2ϕSN OUT signal by N (1820~2426) with an external frequency divider (duty : 50%).
8	11	V. Mask IN	(L : 0V) (H : 5V)		• Driving the V. Mask IN signal to high turns off the phase-comparison operation. Inputs the signal which masks serrated and equalizing pulses of video signal.
9	12	P.D. OUT	—		• Connect an external filter.
10	13	Bias	6V		

TA8667P PIN No.	TA8667F PIN No.	PIN NAME	TYP. DC VOLTAGE	I/O CIRCUIT	FUNCTION
11	14	filter	6V		• Connects an external filter.
12 18 14 15	17 24 19 20	GND1 GND2 $V_{CC}1$ $V_{CC}2$			• Power-supply voltage and GND.
13	18	2ϕSN OUT	—		• Outputs the stable sin wave of N times the fH frequency.
16 17	22 23	VCO TANC	5.2V 5.2V		• Sets the oscillating frequency by adjusting the value of external variable coil.
	3 4 9 15 16 21	NC			

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATINGS	UNIT
Power Supply Voltage		V_{CC} max	12	V
Input Signal Voltage		e_{in} max	6	V_{p-p}
Power	TA8667P	P_D	1320	mW
Consumption	TA8667F		830	
Operating Temperature		T_{opr}	−20~70	°C
Storage Temperature		T_{stg}	−55~150	°C

Ta-P_D
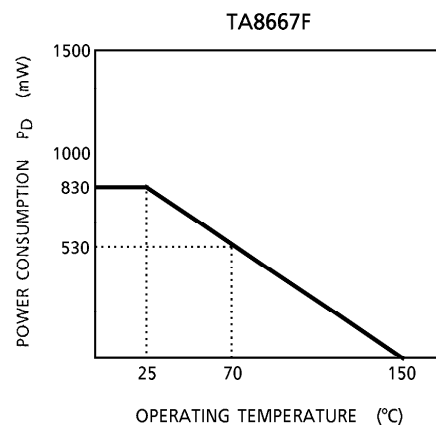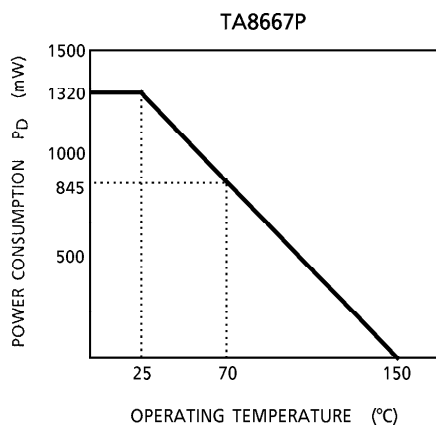
TA8667P

TA8667F

RECOMMENDED OPERATING CONDITION

PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
14	$V_{CC}1$	8.5	9.0	9.5	V
15	$V_{CC}2$				

ELECTRICAL CHARACTERISTICS ($V_{CC} = 9.0V$, Ta = 25°C)
All the pin numbers in the below description are those of the TA8667P.

CHARACTERISTIC		SYMBOL	TEST PIN	TEST CONDITION (SEE "TEST CIRCUIT")	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage		V_{CC}			8.1	9.0	9.9	V
Operating Power Supply Current		I_{CC}			15	27	40	mA
Output Voltage	High Level	$V_{OH}(1)$	3 , 6	1) Measure Voltages V3 and V6 of Pin 3 and Pin 6, respectively. 2) Connect variable voltage source to Pin 2 and Pin 5. 3) Change variable voltage source and measure voltages V3 and V6 when high.	2.5	4.0	5.5	V
		$V_{OH}(2)$	4	1) Measure Voltage V4 of Pin 4. 2) Connect variable voltage source to Pin 1. 3) Change variable voltage source and measure voltage V4 when high.	7.0	—	8.3	
	Low Level	$V_{OL}(1)$	3 , 6	1) Measure Voltages V3 and V6 of Pin 3 and Pin 6, respectively. 2) Connect variable voltage source to Pin 2 and Pin 5. 3) Change variable voltage source and measure voltages V3 and V6 when low.	—	0.3	0.5	
		$V_{OL}(2)$	4	1) Measure Voltage V4 of Pin 4. 2) Connect variable voltage source to Pin 1. 3) Change variable voltage source and measure voltage V4 when low.	—	0.3	0.5	
Input Voltage	High Level	V_{IH}	7 , 8		2.5	4.0	—	
	Low Level	V_{IL}	7 , 8		—	0.3	0.8	
Input Current	High Level	I_{IH}	7 , 8	Connect an ammeter to Pin 7 and Pin 8. $V_{IH} = 4.0V$.	—	—	20	μA
	Low Level	I_{IL}	7 , 8	Connect an ammeter to Pin 7 and Pin 8. $V_{IL} = 0.3V$.	—	0	—	μA

CHARACTERISTIC	SYMBOL	TEST PIN	TEST CONDITION (SEE "TEST CIRCUIT")	MIN.	TYP.	MAX.	UNIT
Sync Separator Input Sensitivity Current	I_{INS}	1 , 2	1) Measure Voltage V4 (V3) of Pin 4 (Pin 3). 2) Connect variable voltage source to Pin 1 (Pin 2) through an ammeter. 3) Change variable voltage source and measure the current outflowed from Pin 1 (Pin 2) on the high to low transition of V4 (V3).	—	23	—	μA
Oscillating Frequency	f_O	13	1) SW1 : Off, SW2 : On 2) Measure the level of TP1 with counter. 3) Adjust the value of the variable coil until it reaches 15.73kHz $\times$ N.	—	28.6 (Note 1)	—	MHz
				—	32.0 (Note 2)	—	
Output Level	V_O	13	Measure the level of TP1 at the time when f_O is measured.	2.0	3.2	4.0	V_{p-p}
Output Jitter	T_G	13	1) Switch on SW1 in the same condition that f_O is measured. 2) Input the sync signal of 15.73kHz to Pin 2. 3) Measure the output waveform of the frequency divider.	—	14	—	ns

(Note 1) VCO TANC : TRF3518D used
(Note 2) VCO TANC : TRF3503K used

| CHARACTERISTIC	SYMBOL	TEST PIN	TEST CONDITION (SEE "TEST CIRCUIT")	MIN.	TYP.	MAX.	UNIT
Horizontal Frequency Phase Comparison Range2	f_c		1) SW1 : Off, SW2 : On. Pin 2 : Open. 2) Measure the frequency of TP1. 3) Adjust the value of the variable coil until it reaches 15.73kHZ × N (f_O = 32.2MHz). 4) SW1 : On 5) Connect S.G* to Pin 2. 6) Measure the power supply of TP2. 7) Raise the S.G* frequency starting from around 13.6kHz and measure the frequency when PLL is locked. 8) Raise the S.G* frequency further and measure it when PLL is unlocked. 9) Lower the frequency and measure it when PLL is locked again. 10) Lower the frequency further and measure it when PLL is unlocked again (See Figure 1).	±700	—	—	Hz
Horizontal Frequency Hold Range	f_H						
C.S. OUT Delay Time (See Figure 2)	t_{csd}	3	 Pin 2 ⎍⎍⎍ 6.0V 5.0V ⎍⎍ 63.5μs t_{csd} Pin 3 ⎍⎍⎍ ⎍⎍	—	—	350	ns
H. ref IN - C.S. OUT Steady-State Phase Difference (See Figure 3)	t_{afce}	7	1) Switch on SW1 in the same condition that f_O is measured. 2) Adjust the value of the variable coil until it reaches 15.73kHz × N (f_O = 32.2MHz). 3) Input the sync signal of 15.73kHz to Pin 2. 4) Measure the signal waveforms of Pin 3 and Pin 7 simultaneously.	—	—	±350	

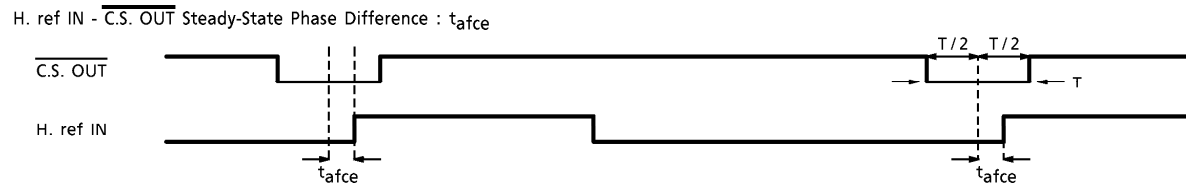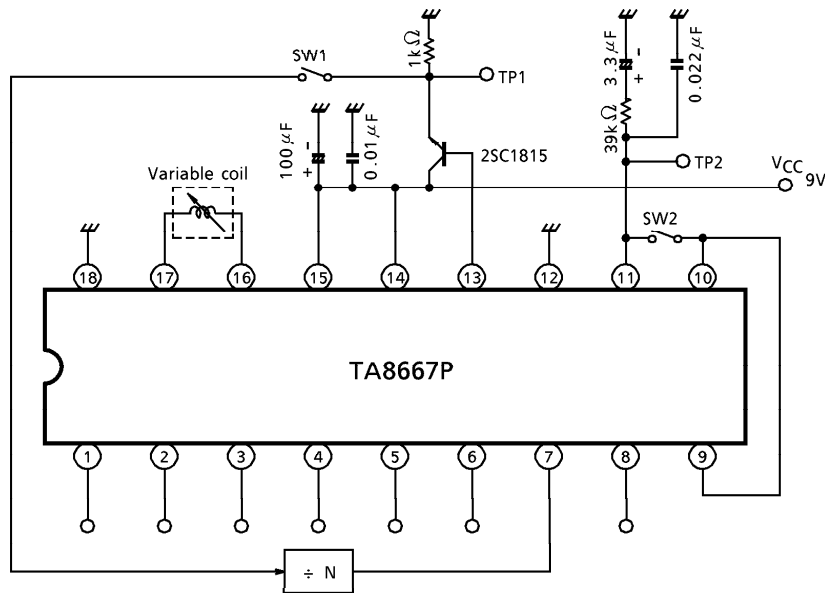* : S.G = Sync Generator

Figure 1
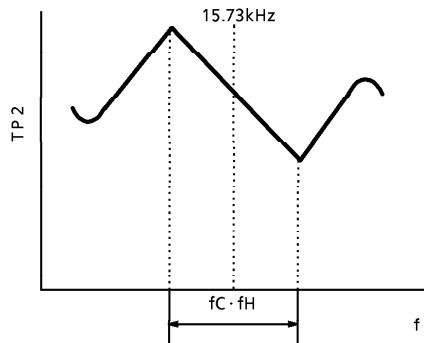
Figure 2
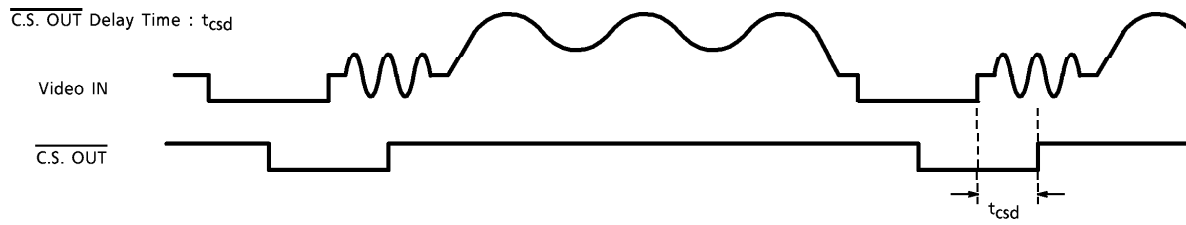
Figure 3

## TEST CIRCUIT (Pin assignment for TA8667P)

Variable coil (VCO TANK) : Select an inductance suited for the oscillating frequency.

PRECAUTIONS

V. Mask IN (See Figure 4, "An example of V. Mask IN timing")

Driving the V. Mask IN signal to high stops phase-comparison operation.
Adjust the signal so that equalizing pulse of video signal and vertical sync signal are masked.
Masking some parts of horizontal sync signal and video signal do not cause a problem.
However, the rise and fall of V. Mask IN must not occur while horizontal sync signal and
equalizing pulse are low - the time indicated with " ↓ " in Figure 4, for example.

Figure 4 "An example of V. Mask IN timing"
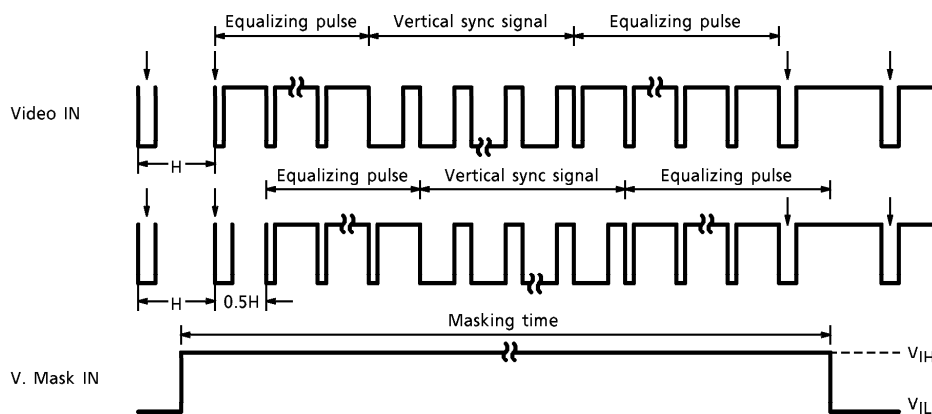
○ Example of VCO TANK Specification for 32MHz clock (TRF3503K)

When f = 7.96MHz :
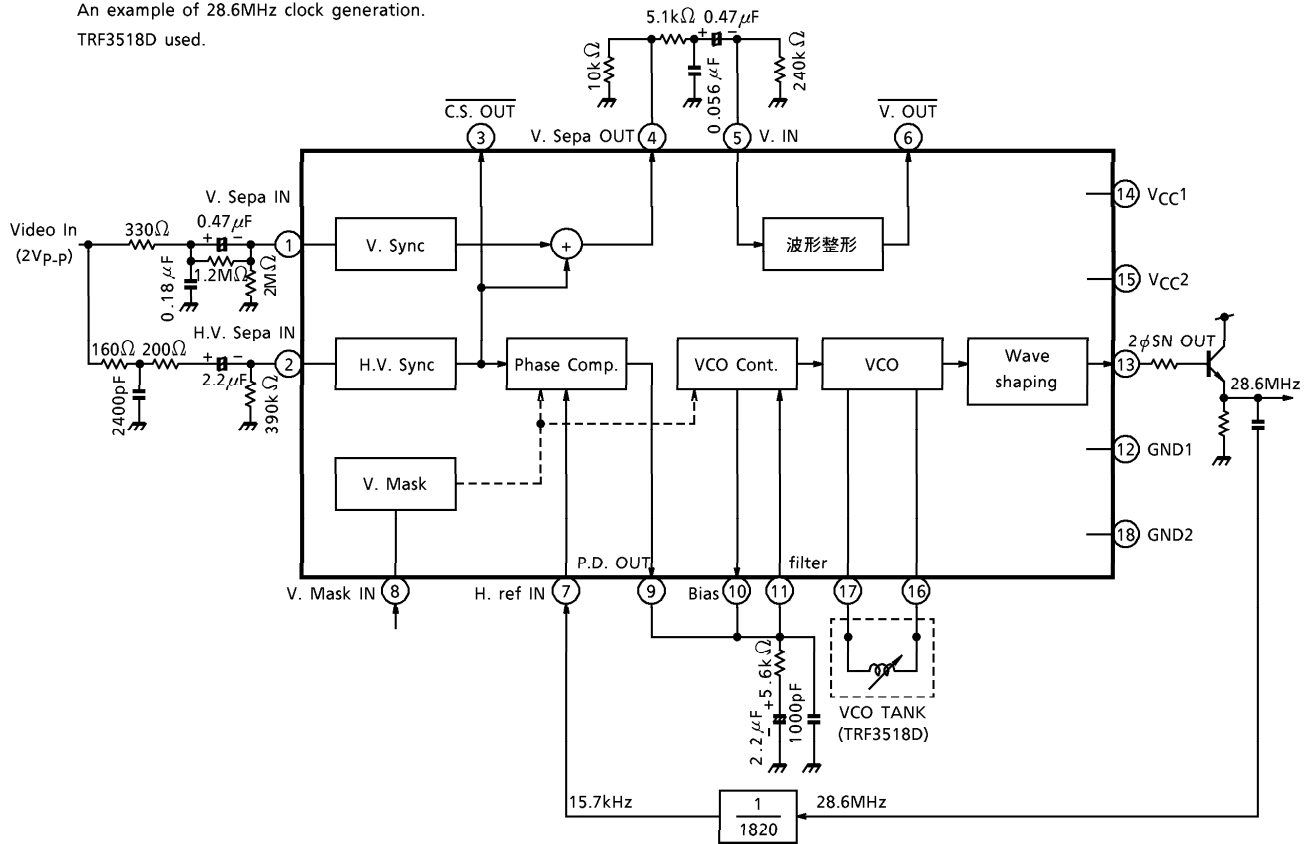$$\begin{cases} L = 2.35\mu H \text{ (Varied within more than } \pm 15\%) \\ Q = 47 \end{cases}$$

○ Example of VCO TANK Specification for 28MHz clock (TRF3518D)

When f = 7.96MHz :
$$\begin{cases} L = 3.5\mu H \text{ (Varied within more than } \pm 15\%) \\ Q = 42 \end{cases}$$

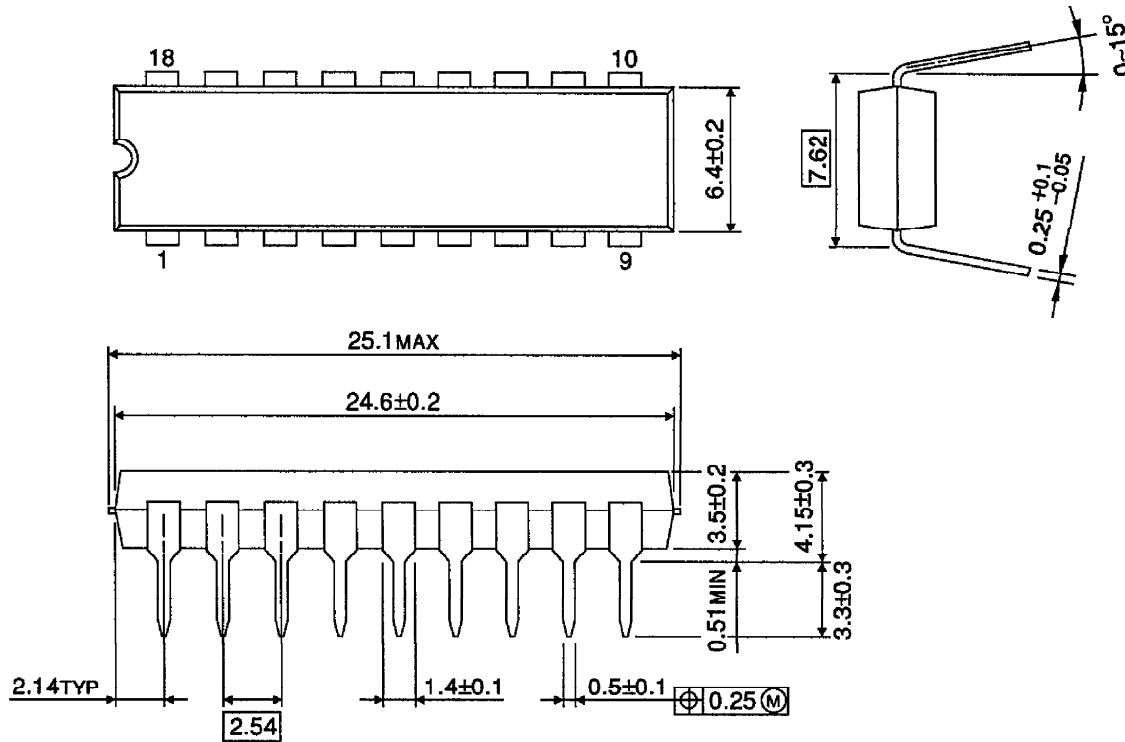**SAMPLE APPLICATION 1** (Pin Assignment for TA8667P)

An example of 28.6MHz clock generation.
TRF3518D used.

The above illustration shows an example for application and may require modification in constant and circuit for practical design.
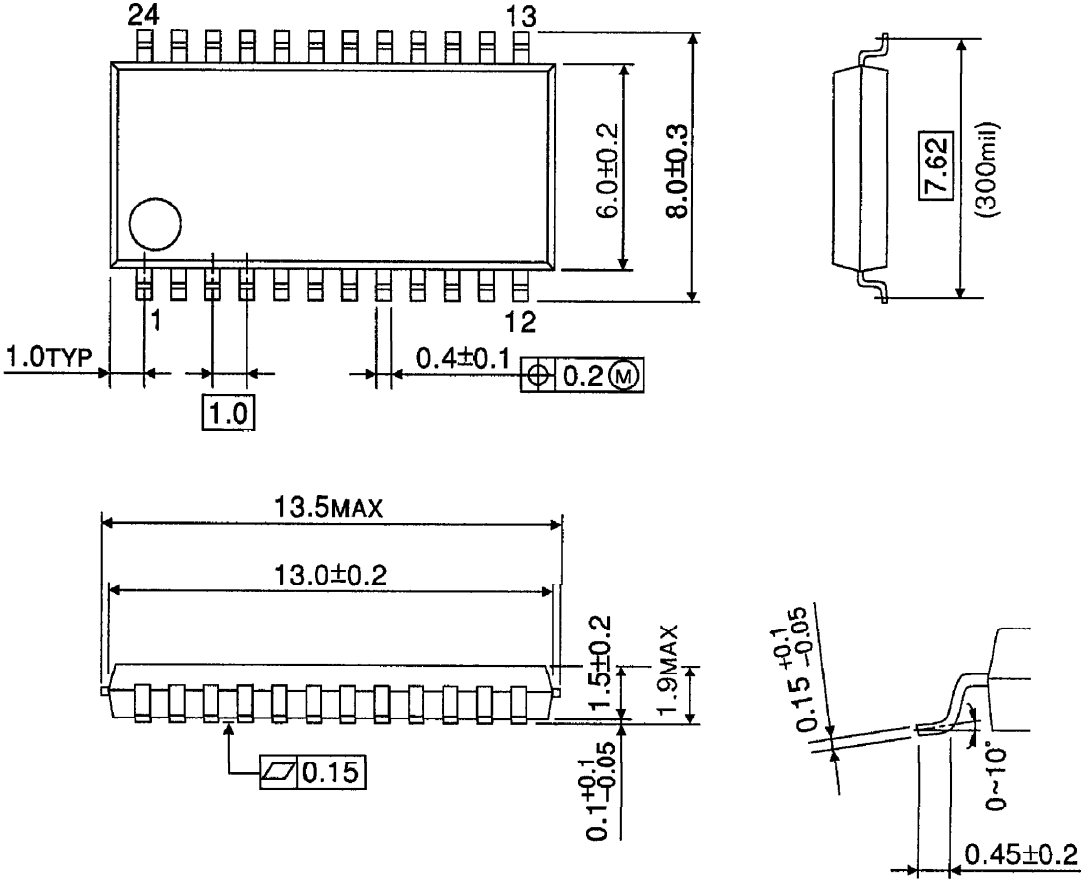
OUTLINE DRAWING
DIP18-P-300-2.54D

Unit : mm

Weight : 1.47g (Typ.)

OUTLINE DRAWING

SSOP24-P-300-1.00B

Unit : mm

Weight : 0.32g (Typ.)