Precision Dual Voltage Regulator Controller

ADM1052

FEATURES
Two Independent Controllers on One Chip
Two 2.525 V Outputs
Shutdown Inputs to Control Each Channel
±2.5% Accuracy Over Line, Load, and Temperature
Low Quiescent Current
Low Shutdown Current
Works with External N-Channel MOSFETs for Low Cost
"Hiccup Mode" Fault Protection
No External Voltage or Current Setting Resistors
Small, 8-Lead SO Package

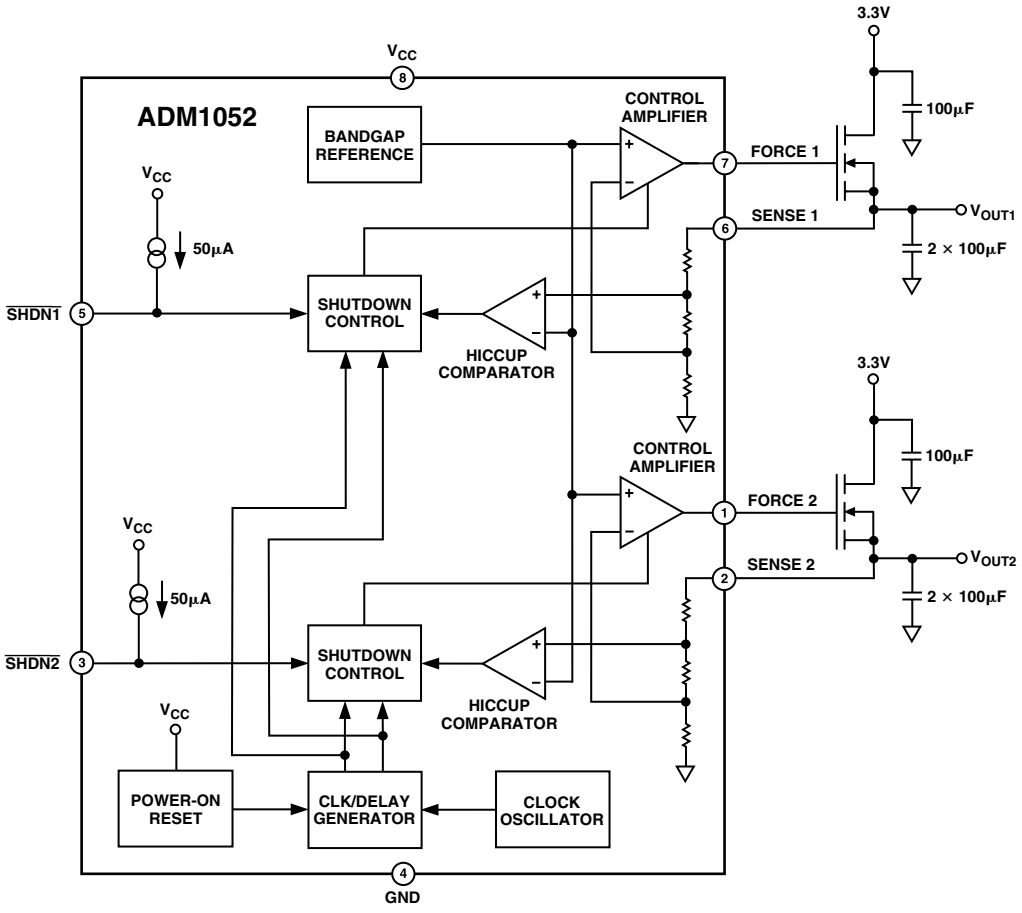
APPLICATIONS
Desktop Computers
Servers
Workstations

GENERAL DESCRIPTION

The ADM1052 is a dual, precision, voltage regulator controller intended for power rail generation and active bus termination on personal computer motherboards. It contains a precision 1.2 V bandgap reference and two channels consisting of control amplifiers driving external power devices. Each channel has a shutdown input to turn off amplifier output and "Hiccup Mode" protection circuitry for the external power device.

The ADM1052 operates from a 12 V supply. This gives sufficient headroom for the amplifiers to drive external N-channel MOSFETs, operating as source-followers, as the external series pass devices. This has the advantage that N-channel devices are cheaper than P-channel devices of similar performance, and the circuit is easier to stabilize than one using P-channel devices in a common-source configuration.

FUNCTIONAL BLOCK DIAGRAM



REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

ADM1052–SPECIFICATIONS (V_{CC} = 12 V ± 6%, V_{IN} = 3.3 V, T_A = 0°C to 70°C, both channels, unless otherwise noted. See Test Circuit.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE					
Channel 1, Channel 2		2.525		V	$\overline{SHDN1}$, $\overline{SHDN2}$ Floating
OUTPUT VOLTAGE ACCURACY	–2.5		+2.5	%	V_{IN} = 3.0 V to 3.6 V, I_{OUT} = 10 mA to 1 A
Load Regulation	–5		+5	mV	V_{IN} = 3.3 V, I_{OUT} = 10 mA to 1 A[1]
Line Regulation	–5		+5	mV	V_{IN} = 3.0 V to 3.6 V, I_{OUT} = 1 A[1]
CONTROL AMPLIFIER					
Control Amplifier Open-Loop Gain		100		dB	
Control Amplifier Slew Rate		3		V/µs	
Closed-Loop Settling Time		5		µs	I_O = 10 mA to 2 A
Turn-On Time			5	µs	To 90% of Force High Output Level (C_L = 470 pF)
Sense Input Impedance[1]		50		kΩ	
Force Output Voltage Swing, V_F (High)		10		V	R_L = 10 kΩ to GND
Force Output Voltage Swing, V_F (Low)		2		V	R_L = 10 kΩ to V_{CC}
HICCUP MODE					
Hiccup Mode Hold-Off Time	30	60	90	ms	Figure 2
Hiccup Mode Threshold			0.8 × V_{OUT}	V	
Hiccup Comparator Glitch Immunity		100		µs	
Hiccup Mode On-Time	0.5	1.0	1.5	ms	
Hiccup Mode Off-Time	20	40	60	ms	
Power-On Reset Threshold	6		9	V	
SHUTDOWN, $\overline{SHDN1}$, $\overline{SHDN2}$					
Shutdown Input Low Voltage, V_{IL}			0.8	V	
Shutdown Input High Voltage, V_{IH}	2.0			V	
Supply Current, Normal Operation		2.4	4.0	mA	Shutdown Inputs Floating
Supply Current, Shutdown Mode		600	1000	µA	Both Channels Shut Down

NOTES

[1]Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} to GND . . . . . 14 V
$\overline{SHDN1}$, $\overline{SHDN2}$ to GND . . . . . –0.3 V to (V_{CC} + 0.3 V)
SENSE1, SENSE2 to GND . . . . . –0.3 V to +5.5 V
FORCE1, FORCE2 . . . . . Short-Circuit to GND or V_{CC}
Continuous Power Dissipation (T_A = 70°C) . . . . . 650 mW
8-Lead SOIC . . . . . (Derate 8.3 mW/°C above 70°C)
Operating Temperature Range
Commercial (J Version) . . . . . 0°C to 70°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

THERMAL CHARACTERISTICS

8-Lead Small Outline Package: θ_{JA} = 150°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1052JR	0°C to 70°C	8-Lead SOIC	SO-8

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	FORCE 2	Output of Channel 2 control amplifier to gate of external N-channel MOSFET.
2	SENSE 2	Input from source of external MOSFET to inverting input of Channel 2 control amplifier, via output voltage-setting feedback resistor network.
3	$\overline{SHDN2}$	Digital Input. Active-low shutdown control with 50 µA internal pull-up. The output of Channel 2 control amplifier goes to ground when $\overline{SHDN2}$ is taken low.
4	GND	Device Ground Pin.
5	$\overline{SHDN1}$	Digital Input. Active-low shutdown control with 50 µA internal pull-up. The output of Channel 1 control amplifier goes to ground when $\overline{SHDN1}$ is taken low.
6	SENSE 1	Input from source of external MOSFET to inverting input of Channel 1 control amplifier, via output voltage-setting feedback resistor network.
7	FORCE 1	Output of Channel 2 control amplifier to gate of external N-channel MOSFET.
8	V_{CC}	12 V Supply.

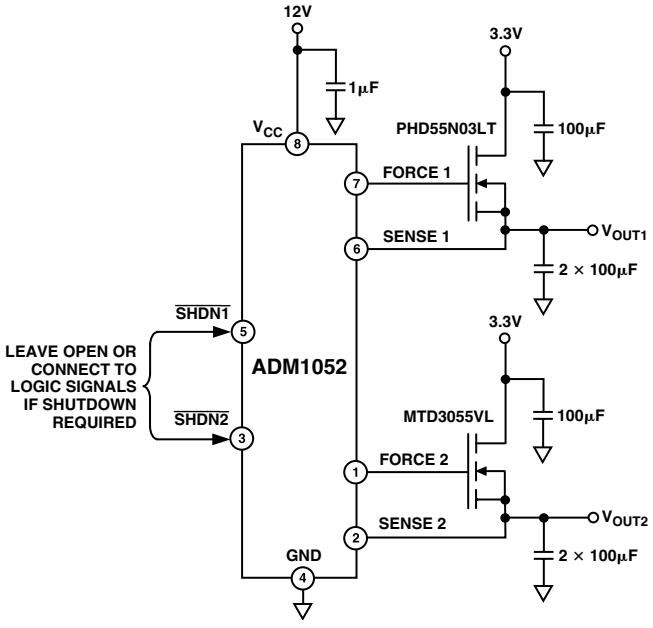
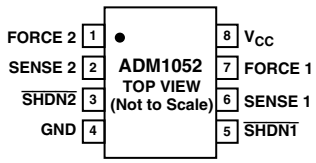


Figure 1. Test Circuit

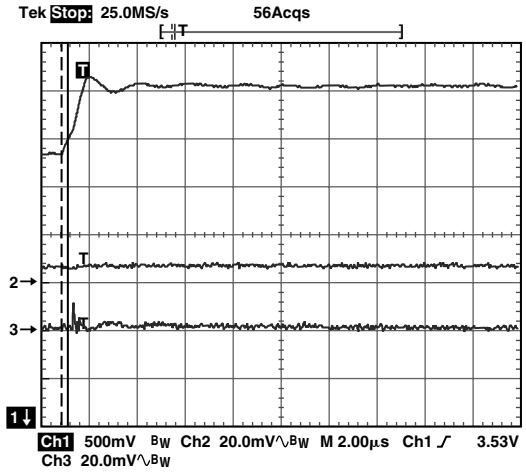
PIN CONFIGURATION



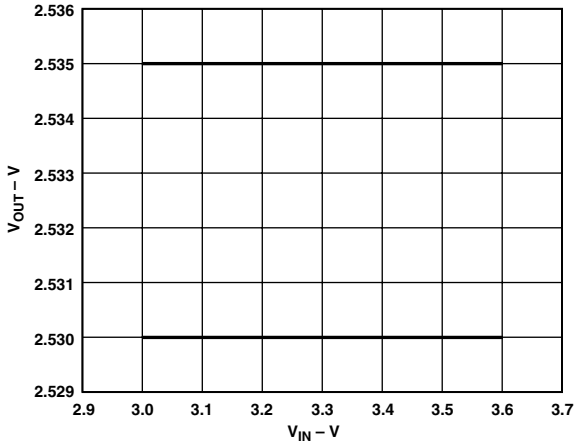
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1052 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

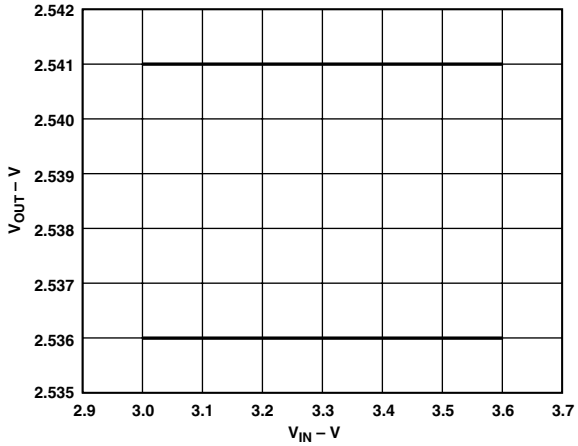
ADM1052–Typical Performance Characteristics



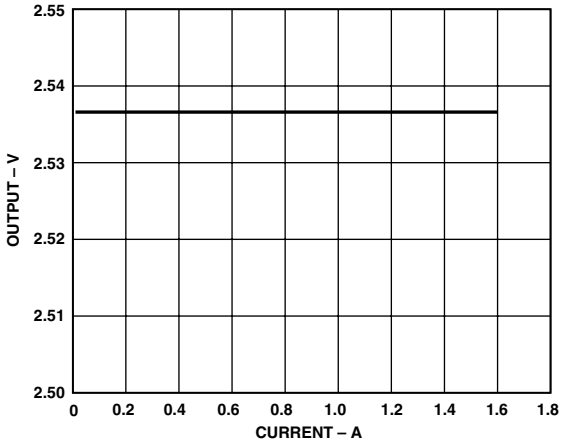
TPC 1. Line Transient Response, Channel 1 and Channel 2



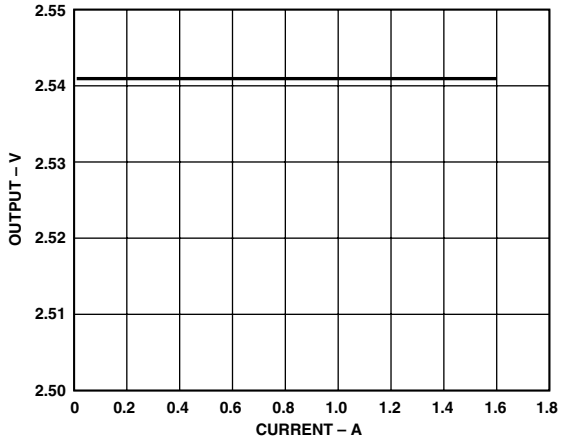
TPC 2. Line Regulation, Channel 1



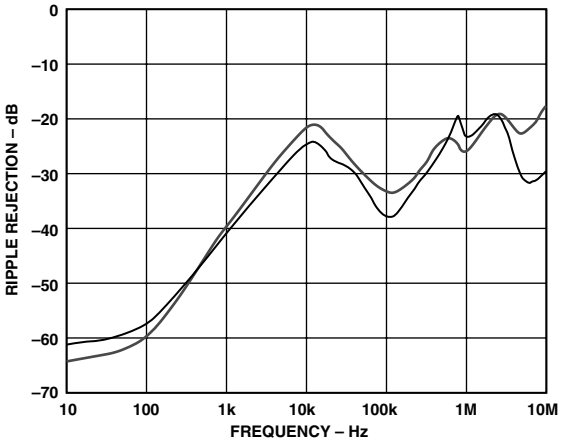
TPC 3. Line Regulation, Channel 2



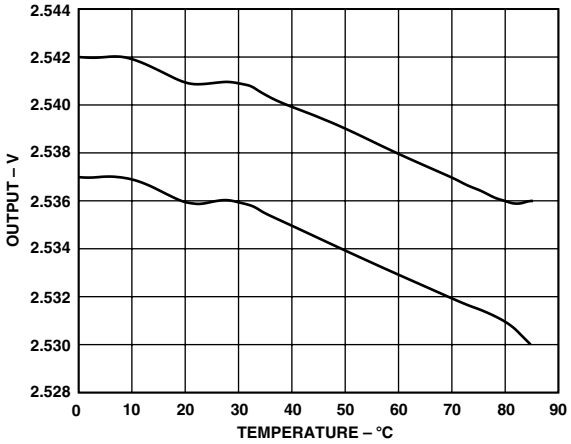
TPC 4. Load Regulation, Channel 1



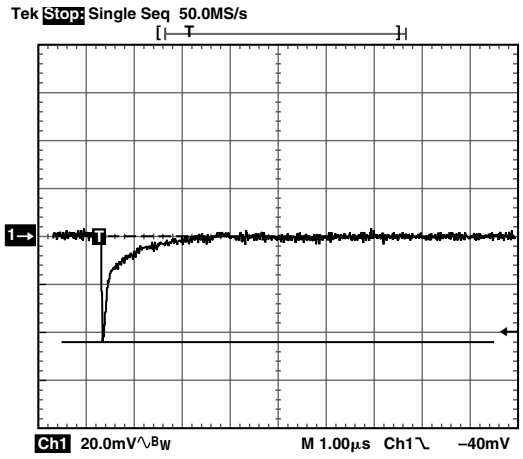
TPC 5. Load Regulation, Channel 2



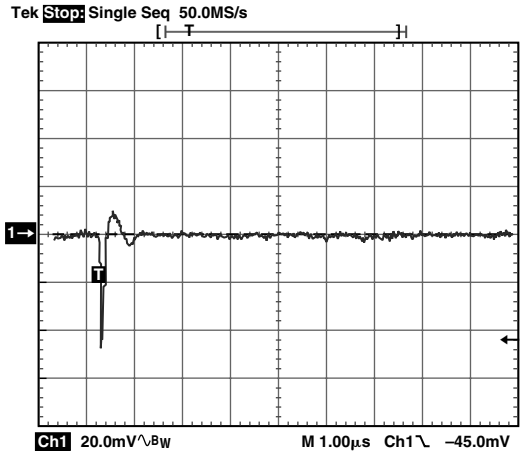
TPC 6. V_{CC} Supply Ripple Rejection



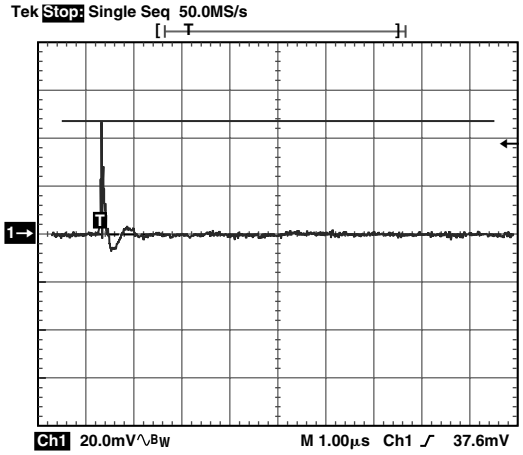
TPC 7. Regulator Output Voltage vs. Temperature



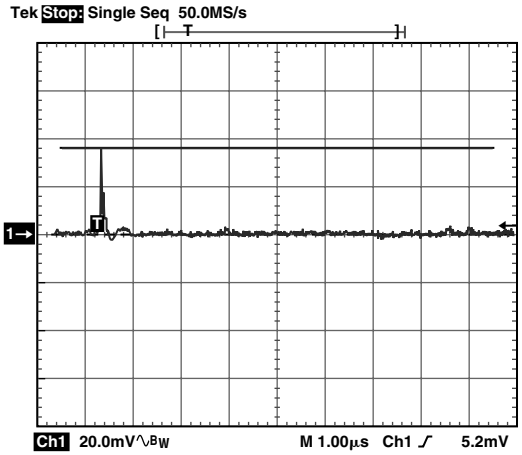
TPC 10. Transient Response Channel 2, 10 mA to 2 A Output Load Step



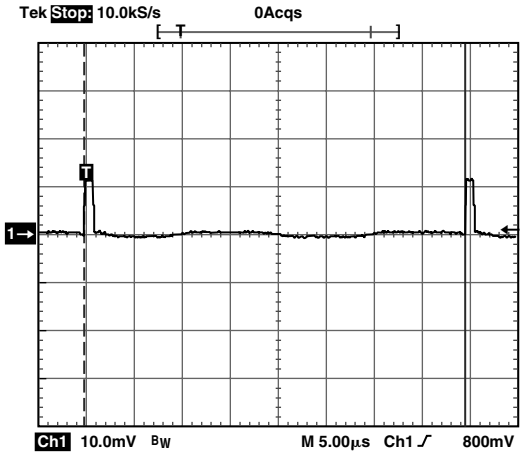
TPC 8. Transient Response Channel 1, 10 mA to 2 A Output Load Step



TPC 11. Transient Response Channel 2, 2 A to 10 mA Output Load Step



TPC 9. Transient Response Channel 1, 2 A to 10 mA Output Load Step



TPC 12. Force Output In Hiccup Mode, Channel 1

GENERAL DESCRIPTION

The ADM1052 is a dual, precision, voltage regulator controller intended for power rail generation and active bus termination on personal computer motherboards. It contains a precision 1.2 V bandgap reference and two channels consisting of control amplifiers driving external power devices. Both channels have an output of nominally 2.525 V. Each channel has a shutdown input to turn off amplifier output and protection circuitry for the external power device.

The ADM1052 operates from a 12 V V_{CC} supply. The output is disabled until V_{CC} climbs above the reset threshold (6 V–9 V). The output from the ADM1052 is used to drive external N-channel MOSFETs, operating as source-followers. This has the advantage that N-channel devices are cheaper than P-channel devices of similar performance, and the circuit is easier to stabilize than one using P-channel devices in a common-source configuration.

The external power devices are protected by a "Hiccup Mode" circuit that operates if the circuit goes out of regulation due to an output short-circuit. In this case the power device is pulsed on/off with a 1:40 duty cycle to limit the power dissipation until the fault condition is removed.

CIRCUIT DESCRIPTION

CONTROL AMPLIFIERS

The reference voltage is amplified and buffered by the control amplifiers and external MOSFETs, the output voltage of each channel being determined by the feedback resistor network between the sense input and the inverting input of the control amplifier.

A power-on reset circuit disables the amplifier output until V_{CC} has risen above the reset threshold (6 V–9 V).

Each amplifier output drives the gate of an N-channel power MOSFET, whose drain is connected to the unregulated supply input and whose source is the regulated output voltage, which is also fed back to the appropriate sense input of the ADM1052. The control amplifiers have high current-drive capability so that they can quickly charge and discharge the gate capacitance of the external MOSFET, thus giving good transient response to changes in load or input voltage.

SHUTDOWN INPUTS

Each channel has a separate shutdown input, which may be controlled by a logic signal and allows the output of the regulator to be turned on or off. If the shutdown input is held high or not connected, the regulator operates normally. If the shutdown input is held low, the enable input of the control amplifier is turned off and the amplifier output goes low, turning off the regulator.

"HICCUP MODE" FAULT PROTECTION

Hiccup mode fault protection is a simple method of protecting the external power device without the added cost of external sense resistors or a current sense pin on the ADM1052. In the event of a short-circuit condition at the output, the output voltage will fall. When the output voltage of a channel falls 20% below the nominal voltage, this is sensed by the hiccup comparator and the channel will go into hiccup mode, where the enable signal to the control amplifier is pulsed on and off with a 1:40 duty cycle.

To prevent the device inadvertently going into hiccup mode during power-up or during channel enabling, the hiccup mode is held off for approximately 60 ms on both channels. By this time the output voltage should have reached its correct value. In the case of power-up, the hold-off period starts when V_{CC} reaches the power-on reset threshold of 6 V–9 V. In the case of channel enabling, the hold-off period starts when $\overline{SHDN}$ is taken high. Note that the hold-off timeout applies to both channels even if only one channel is disabled/enabled.

As the 3.3 V input to the drain of the MOSFET is not monitored, it should ideally rise at the same or a faster rate than V_{CC}. At the very least it must be available in time for V_{OUT} to reach its final value before the end of the power-on delay. If the output voltage is still less than 80% of the correct value after the power-on delay, the device will go into hiccup mode until the output voltage exceeds 80% of the correct value during a hiccup mode on-period. Of course, if there is a fault condition at the output during power-up, the device will go into hiccup mode after the power-up delay and remain there until the fault condition is removed.

The effect of power-on delay is illustrated in Figure 2, which shows an ADM1052 being powered up with a fault condition. The output current rises to a very high value during the power-on delay, the device goes into hiccup mode, and the output is pulsed on and off at 1:40 duty cycle. When the fault condition is removed, the output voltage recovers to its normal value at the end of the hiccup mode off period.

The load current at which the ADM1052 will go into hiccup mode is determined by three factors:

- The input voltage to the drain of the MOSFET, V_{IN}
- The output voltage V_{OUT} (–20%)
- The on-resistance of the MOSFET, R_{ON}

$$I_{HICCUP} = (V_{IN} - (0.8 \times V_{OUT}))/R_{ON}$$

It should be emphasized that the hiccup mode is not intended as a precise current limit but as a simple method of protecting the external MOSFET against catastrophic fault conditions such as output short circuits.

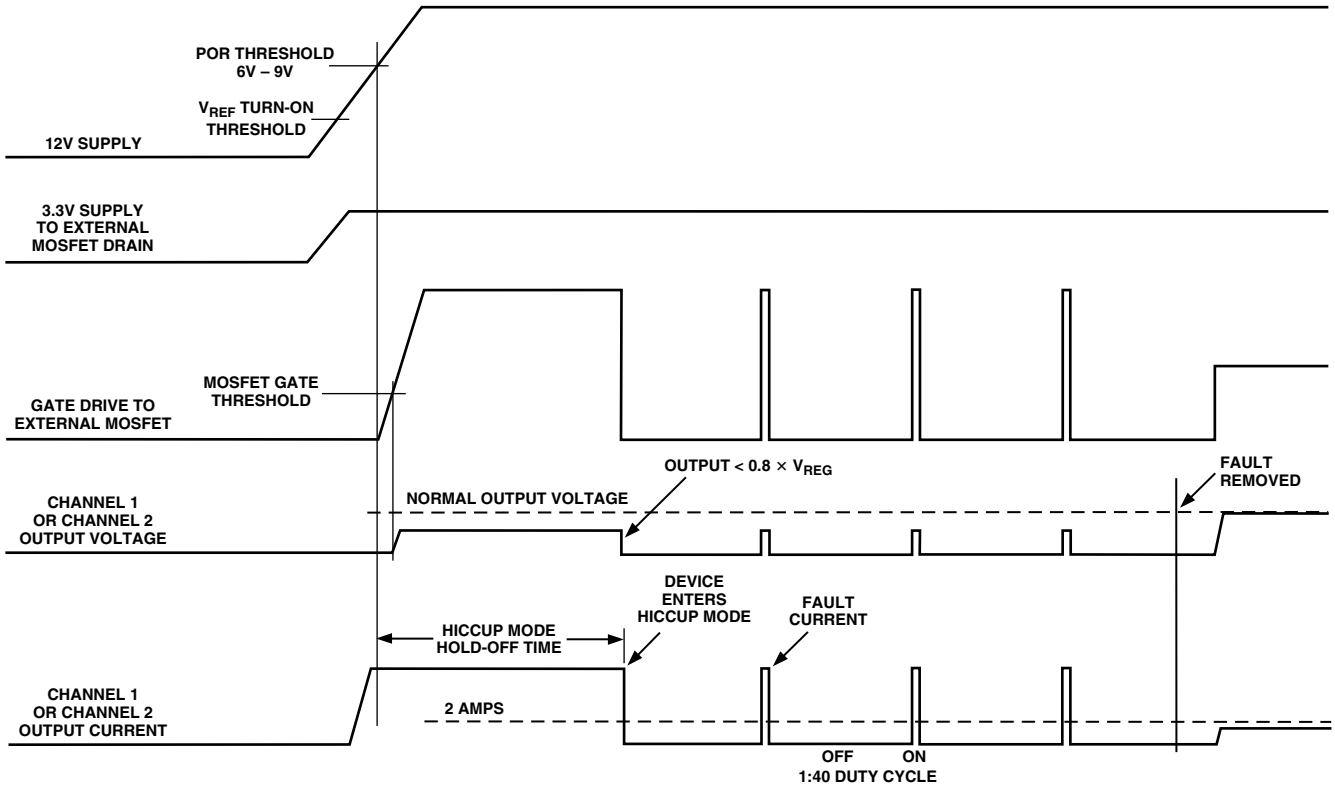


Figure 2. Power-On Reset and Hiccup Mode

APPLICATIONS INFORMATION

PCB LAYOUT

For optimum voltage regulation, the loads should be placed as close as possible to the source of the output MOSFETs and feedback to the sense inputs should be taken from a point as close to the loads as possible. The PCB tracks from the loads back to the sense inputs should be separate from the output tracks and not carry any load current.

Similarly, the ground connection to the ADM1052 should be made as close as possible to the ground of the loads, and the ground track from the loads to the ADM1052 should not carry load current. Correct and incorrect layout practice is illustrated in Figure 3.

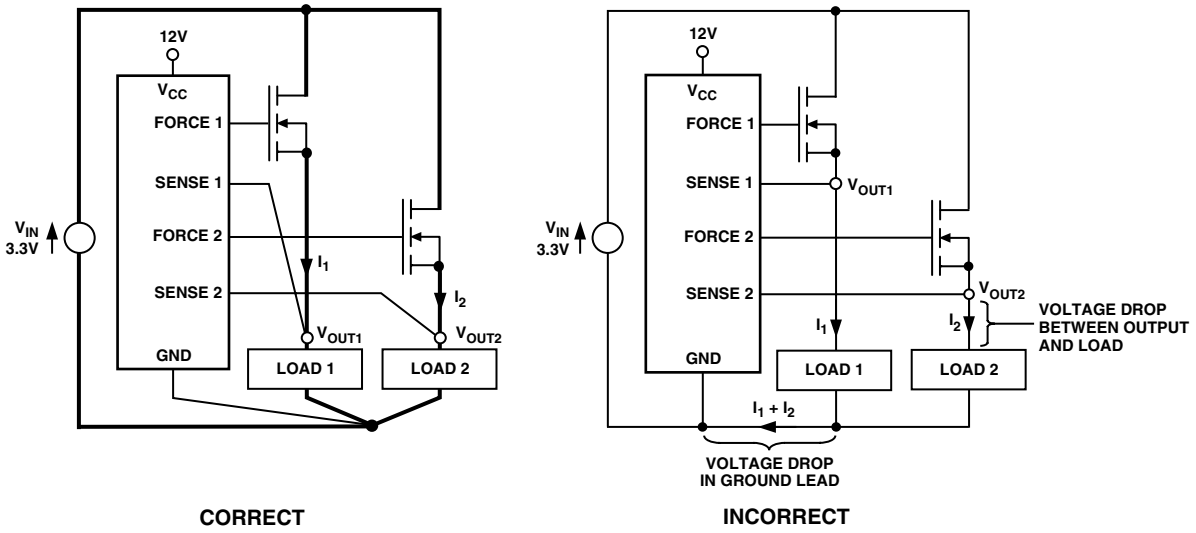


Figure 3. Correct and Incorrect Layout Practice

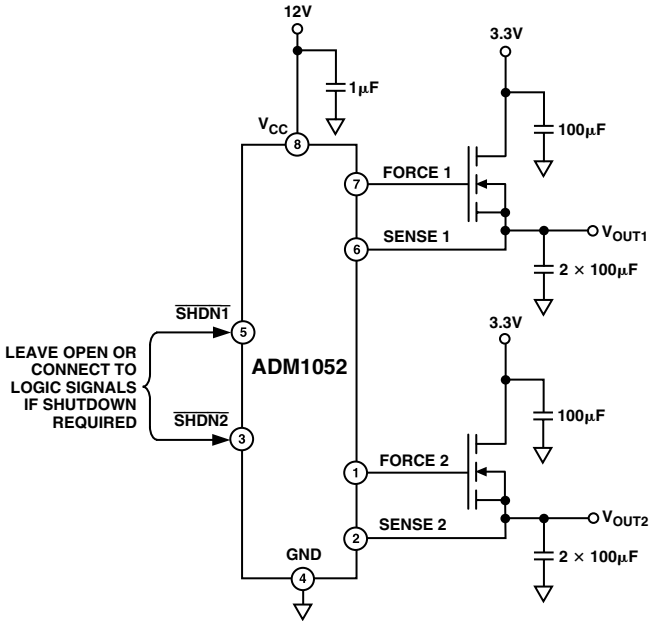


Figure 4. Typical Application Circuit

SUPPLY DECOUPLING

The supply to the drain of an external MOSFET should be decoupled as close as possible to the drain pin of the device, with a 100 µF capacitor to ground. The output from the source of the MOSFET should be decoupled as close as possible to the source pin of the device. Decoupling capacitors should be chosen to have a low Equivalent Series Resistance (ESR). With the MOSFETs specified and two 100 µF capacitors in parallel, the circuit will be stable for load currents up to 2 A. The V_{CC} pin of the ADM1052 should be decoupled with a 1 µF capacitor to ground, connected as close as possible to the V_{CC} and GND pins.

In practice, the amount of decoupling required will depend on the application. PC motherboards are notoriously noisy environments, and it may be necessary to employ distributed decoupling to achieve acceptable noise levels on the supply rails.

CHOICE OF MOSFET

As previously discussed, the load current at which an output goes into hiccup mode depends on the on-resistance of the external MOSFET. If the on-resistance is too low this current may be very high. While the Test Circuit (Figure 1) shows the use of the lower resistance PHD55N03LT from Philips on Channel 1 and the use of the higher resistance MTD3055VL from Motorola on Channel 2, the MTD3055VL is, in fact, suitable for both channels. Similarly, the PHB11N06LT from Philips is also suitable for both channels.

THERMAL CONSIDERATIONS

Heat generated in the external MOSFET must be dissipated and the junction temperature of the device kept within acceptable limits. The power dissipated in the device is, of course, the drain-source voltage multiplied by the load current. The required thermal resistance to ambient is given by

$$\theta_{JA} = T_{J(MAX)} - T_{AMB(MAX)}/(V_{DS(MAX)} \times I_{OUT(MAX)})$$

Surface-mount MOSFETs such as those specified must rely on heat conduction through the device leads and the PCB. One square inch of copper (645 sq. mm) gives a thermal resistance of around 60°C/W for a SOT-223 surface-mount package and 80°C/W for a SO-8 surface-mount package.

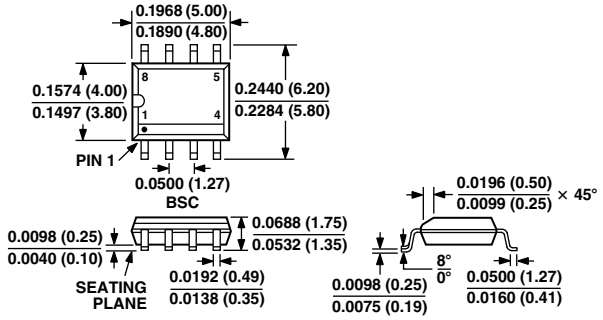
For higher power dissipation than can be accommodated by a surface-mount package D^2PAK or TO-220 devices are recommended. These should be mounted on a heatsink with a thermal resistance low enough to maintain the required maximum junction temperature.

C02127–0–1/01 (rev. A)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Small Outline Package
(Narrow Body, SO-8)



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