AK9813A

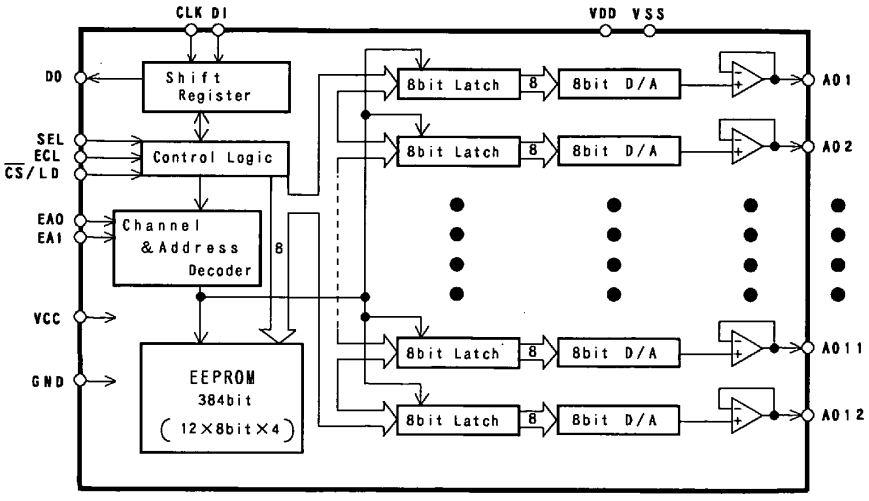
12ch 8bit D/A Converter with EEPROM

General Description

The AK9813A includes 12 channel, 8bit D/A converters with on-chip output buffer amps and it is capable to store the input digital data of each DAC by on-chip non-volatile CMOS EEPROM. The AK9813A is optimally designed for various circuit adjustments for consumer and industrial equipments and it is ideally suited for replacing mechanical trimmers.

Features

- EEPROM SECTION
  - 12 words × 8bit × 4 organization for DAC
- D/A converter section
  - 12 channels
  - Resolution : 8bit
  - DNL : -1~+2 LSB
  - INL : ±1.5 LSB
  - Analog Output Voltage Range : GND ~ VCC
- Operating Voltage Range
  - Digital section : 2.7V~5.5V
  - Analog section : 5.0V±0.5V,3.3V±0.3V
- 24pin VSOP

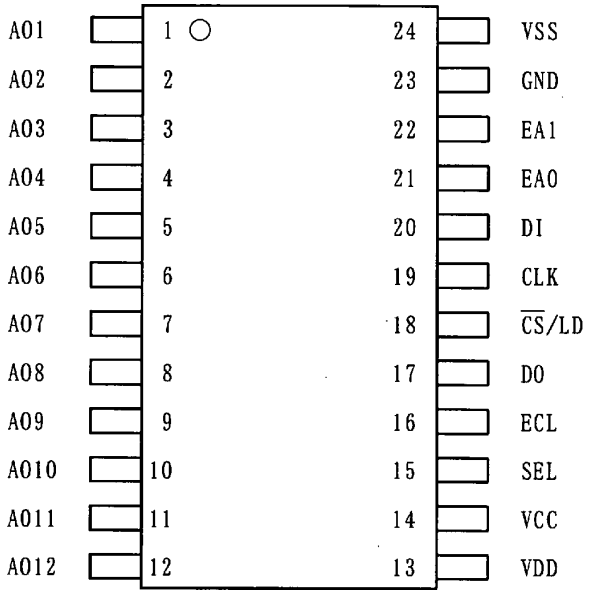


Block Diagram

■ Ordering Guide

AK9813AF	-10 to +85°C	24-pinVSOP

■ Pin Layout



■ **Pin Description(1)**

No.	Pin Name	I/O	Function
20	DI	I	Serial Data Input Pin SEL=High : 16bit data input format SEL=Low : 14bit data input format
17	DO	O	(SEL=High:CS I/F) AK9813A reads out the data with LSB first in the 16bit shift register to DO pin synchronously with falling edge of CLK. When the $\overline{CS}$ pin is high level, the DO pin becomes high impedance. In STATUS mode, the DO pin outputs Ready/$\overline{Busy}$ status. (SEL=Low:LD I/F) AK9813A reads out the data with MSB first in the 14bit shift register to DO pin synchronously with falling edge of CLK. In WRITE mode, the DO pin outputs $\overline{Ready}$/Busy status.
19	CLK	I	Shift Clock Input Pin(Schmitt-trigger input) AK9813A takes in the data from DI pin synchronously with rising edge of the CLK pin. The data are transferred to the internal shift register.
18	$\overline{CS}$/LD	I	Chip Select Input Pin(Schmitt-trigger input) The CS/LD is internally pulled up to VCC. (SEL=High:CS I/F) After the $\overline{CS}$ pin changes from high level to low level while the CLK pin is high level, the AK9813A can input the data to the internal shift register and takes in the data from the DI pin synchronously with the rising edge of the CLK pin. After the $\overline{CS}$ pin changes from high level to low level while the CLK pin is low level, the AK9813A becomes the status mode and reads out the Ready/$\overline{Busy}$ status to the DO pin. When the $\overline{CS}$ pin changes from low level to high level regardless of Low/High level of the CLK pin, the AK9813A removes from the status mode to the normal mode. The $\overline{CS}$ pin usually should be kept at high level. (SEL=Low:LD I/F) When the LD pin receives high pulse, the data of the internal shift register is transferred to the internal decoder or the register for D/A. The LD pin usually should be kept at low level.

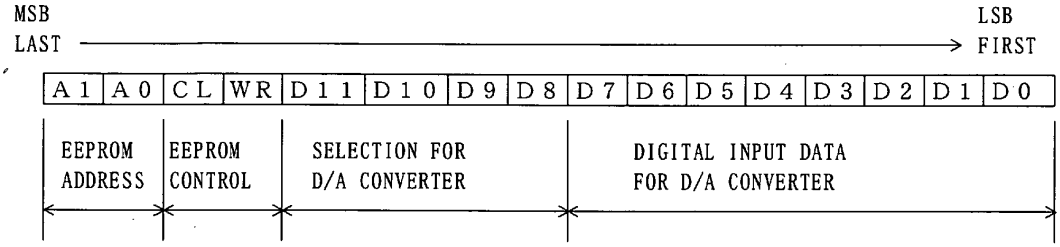
■ **Pin Description(2)**

No.	Pin Name	I/O	Function
1 | 12	AO1 | AO12	O	8bit D/A outputs with OP-AMP
14	Vcc	-	Digital section Power Supply Pin
23	GND	-	Digital section Ground Pin
13	Vdd	-	OP-AMP and D/A section Power Supply
24	Vss	-	OP-AMP and D/A section Ground
21 22	EA0 EA1	I	(SEL=High:CS I/F) In AUTO READ operation and ECL operation, the address of EEPROM is selected by the EA0 and the EA1 pins. (SEL=Low:LD I/F) The address of EEPROM is selected by the EA0 and the EA1 pins.
16	ECL	I	When the ECL pin receives high pulse, the data in EEPROM is automatically loaded to each corresponding D/A, starting from AO1 to AO12 in order. Then each D/A output is settled to pre-determined value.
15	SEL	I	Input Data Format Select Pin SEL=High : CS I/F SEL=Low : LD I/F After power-up, this pin should be kept either at "high" or "Low."

Data Configuration

AK9813A have a shift register in order to control the chip.
When the SEL pin is "H"(CS I/F), the shift register becomes 16bit configuration and the data on the DI pin should be loaded with LSB first. When the SEL pin is "L"(LD I/F), the shift register becomes 14bit configuration and the data on the DI pin is loaded with MSB first.
The following description shows the configuration of the shift register.
The data set consist of 2-bits for the control of the internal EEPROM, 2-bits for the address of the EEPROM (CS I/F only), 4-bits for select of D/A converter and 8-bits for the digital input data of the 8bit D/A converter and total data set is 16bits or 14bits.

① Shift register configuration : SEL=High(CS I/F)



OUTPUT VOLTAGE FOR D/A CONVERTER

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE FOR D/A
0	0	0	0	0	0	0	0	≒ GND=VSS
0	0	0	0	0	0	0	1	≒ VDD/255 × 1
0	0	0	0	0	0	1	0	≒ VDD/255 × 2
1	1	1	1	1	1	1	0	≒ VDD/255 × 254
1	1	1	1	1	1	1	1	≒ VDD

A1	A0	EEPROM ADDRESS
0	1	ADDRESS : 0
0	1	ADDRESS : 1
1	0	ADDRESS : 2
1	1	ADDRESS : 3

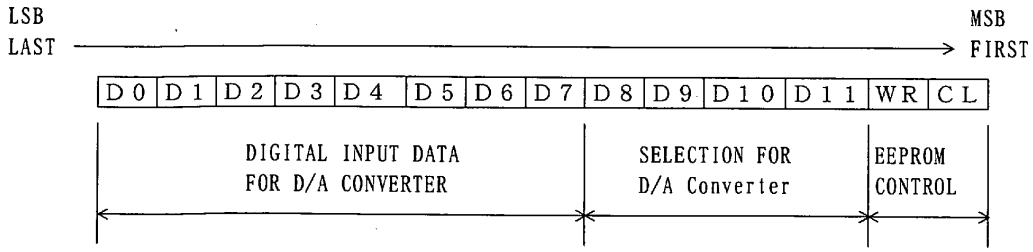
D/A CONVERTER CHANNEL SELECTION

D11	D10	D9	D8	D/A CHANNEL
0	0	0	0	Don't Care
0	0	0	1	AO1
0	0	1	0	AO2
0	0	1	1	AO3
0	1	0	0	AO4
0	1	0	1	AO5
0	1	1	0	AO6
0	1	1	1	AO7

D11	D10	D9	D8	D/A CHANNEL
1	0	0	0	AO8
1	0	0	1	AO9
1	0	1	0	AO10
1	0	1	1	AO11
1	1	0	0	AO12
1	1	0	1	Can't use
1	1	1	0	Can't use
1	1	1	1	Don't Care

(NOTE) Above "Don't care" state is valid only when AK9813A is in DAC mode or WRITE mode.
Refer to the following section "Instruction Set" about mode.

② Shift register configuration:SEL=Low(LD I/F)



OUTPUT VOLTAGE FOR D/A CONVERTER

D0	D1	D2	D3	D4	D5	D6	D7	OUTPUT VOLTAGE FOR D/A
0	0	0	0	0	0	0	0	≒ GND=VSS
1	0	0	0	0	0	0	0	≒ VDD/255 × 1
0	1	0	0	0	0	0	0	≒ VDD/255 × 2
0	1	1	1	1	1	1	1	≒ VDD/255 × 254
1	1	1	1	1	1	1	1	≒ VDD

EA1	EA0	EEPROM ADDRESS
0	0	ADDRESS : 0
0	1	ADDRESS : 1
1	0	ADDRESS : 2
1	1	ADDRESS : 3

NOTE)
EEPROM ADDRESS is selected by the EA0 and EA1 pins.

D/A CONVERTER CHANNEL SELECTION

D8	D9	D10	D11	D/A CHANNEL
0	0	0	0	Don't Care
0	0	0	1	AO1
0	0	1	0	AO2
0	0	1	1	AO3
0	1	0	0	AO4
0	1	0	1	AO5
0	1	1	0	AO6
0	1	1	1	AO7

D8	D9	D10	D11	D/A CHANNEL
1	0	0	0	AO8
1	0	0	1	AO9
1	0	1	0	AO10
1	0	1	1	AO11
1	1	0	0	AO12
1	1	0	1	CAN'T USE
1	1	1	0	CAN'T USE
1	1	1	1	Don't Care

(NOTE) Above "Don't care" state is valid only when AK9813A is in DAC mode or WRITE mode.
Refer to the following section "Instruction Set" about mode.

Instruction Set

The AK9813A can be controlled for the following mode. The following mode is common to the LD I/F and the CS IF. When LD I/F is selected, "A1" and "A0" are set by the external pins (EA0 pin and EA1 pin).

① DAC mode(External DI pin -> D/A converter) [×:Don't Care]

A1	A0	CL	WR	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
×	×	0	0	D/A Channel				Digital data for D/A								D/A output

② CALL mode(Internal EEPROM -> D/A converter) [×:Don't Care]

A1	A0	CL	WR	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
ADDRESS		1	0	D/A Channel				×	×	×	×	×	×	×	×	READ

- The output of D/A converter is set by the data in the internal EEPROM.

③ ALL CALL mode(Internal EEPROM -> D/A converter) [×:Don't Care]

A1	A0	CL	WR	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
ADDRESS		1	0	0	0	0	0	×	×	×	×	×	×	×	×	ALL CHANNEL READ

- The outputs of all D/A converters are set by the data in the internal EEPROM.

・・・Internal ECL function

④ WRITE ENABLE mode(Internal EEPROM WRITE ENABLE) [×:Don't Care]

A1	A0	CL	WR	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
×	×	1	1	0	0	0	0	×	×	×	×	×	×	×	×	WRITE ENABLE

- After WRITE ENABLE mode is executed, the programming to the internal EEPROM is enabled. Upon power-up and after the execution of the ECL function, the AK9813A is in the programming disable state.

⑤ WRITE DISABLE mode(Internal EEPROM WRITE DISABLE) [×:Don't Care]

A1	A0	CL	WR	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
×	×	1	1	1	1	1	1	×	×	×	×	×	×	×	×	WRITE DISABLE

- After WRITE DISABLE mode is executed, the programming to the internal EEPROM is disabled.

⑥ WRITE mode(External DI pin -> Internal EEPROM) [×:Don't Care]

A1	A0	CL	WR	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
ADDRESS		0	1	D/A Channel				Digital data for D/A								WRITE

- The digital data for D/A (D0~D7) is written into the specified address in the internal EEPROM. The state of the internal EEPROM must be the programming enable state.

⑦ READ mode(Internal EEPROM -> External DO pin) [×:Don't Care]

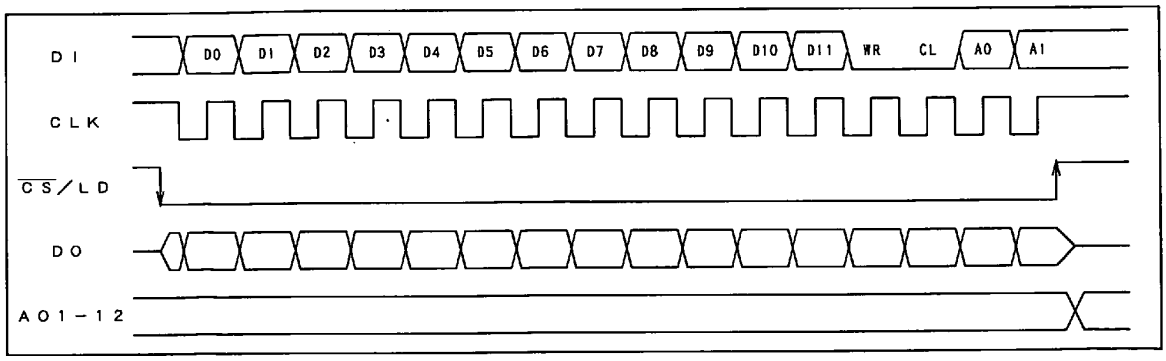
A1	A0	CL	WR	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
ADDRESS		1	1	D/A Channel				×	×	×	×	×	×	×	×	EEPROM DATA output

- The DO pin outputs the data in the internal EEPROM synchronously with the falling edge of of the input pulse of the CLK pin.

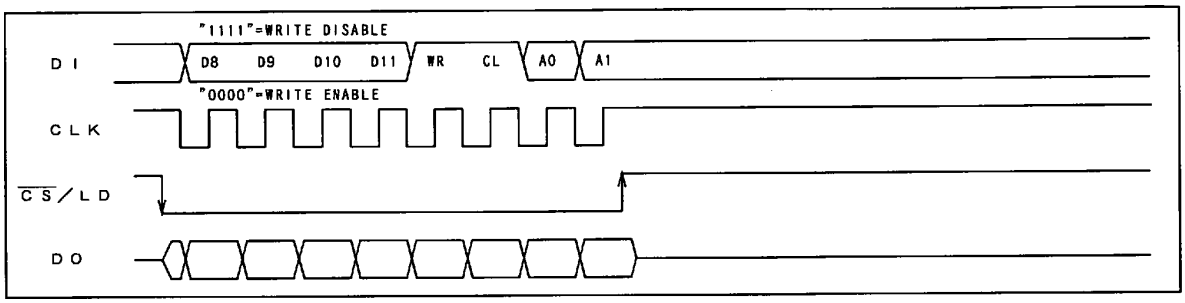
Functional Description

① Timing Diagram for CS I/F (SEL="H")

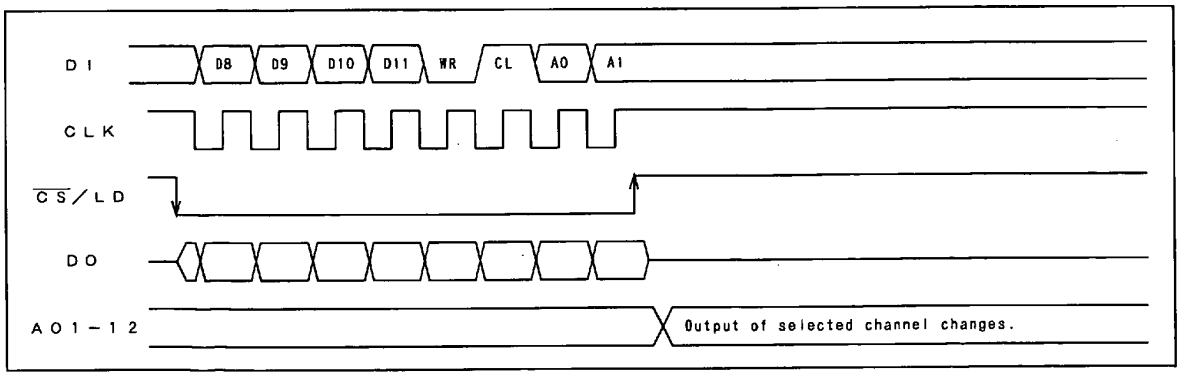
1.DAC mode:The internal EEPROM is not used.



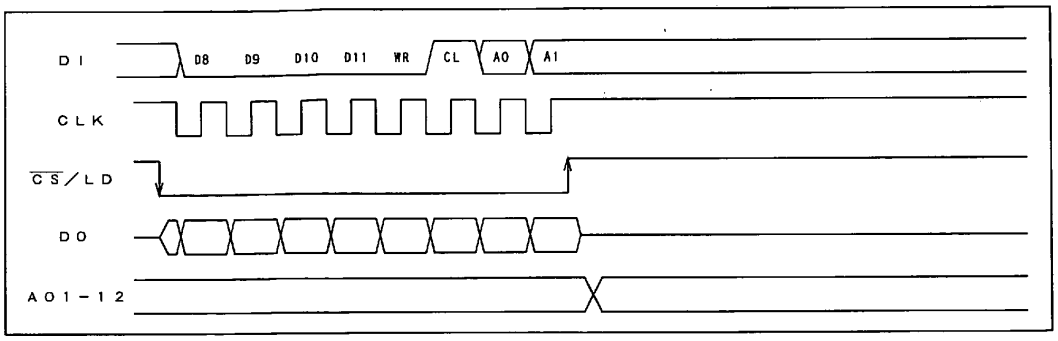
2.WRITE ENABLE/DISABLE mode:The programming state of the internal EEPROM is set.



3.CALL mode: The output of the D/A is set by the data in the internal EEPROM.

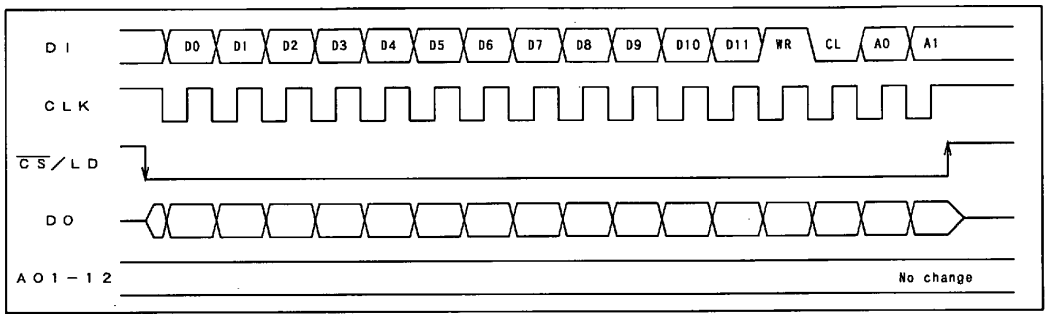


4.ALL CALL mode : The outputs of the all D/As are set by the data in the internal EEPROM.

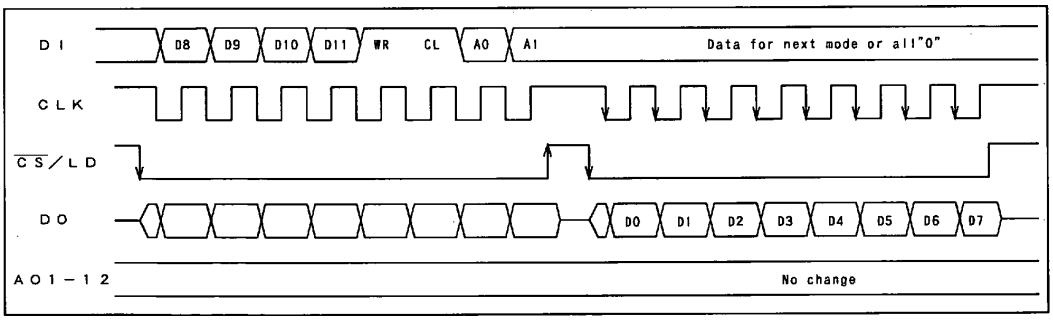


• The D/A outputs are set from AO1 to AO12 in order.

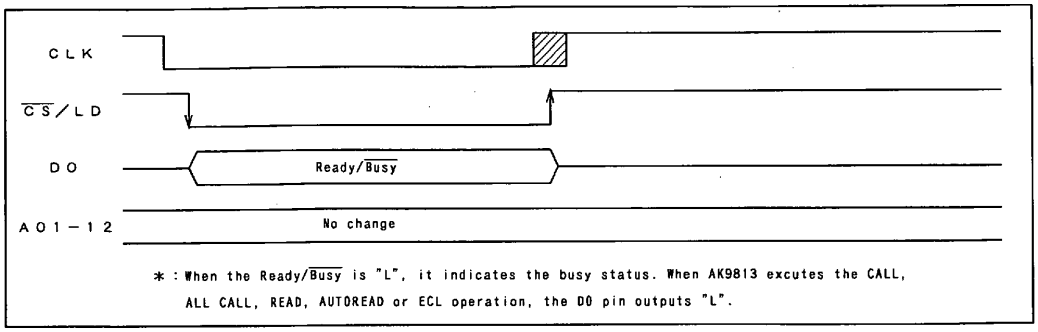
5.WRITE mode:The digital input data for D/A converter is written into the internal EEPROM.



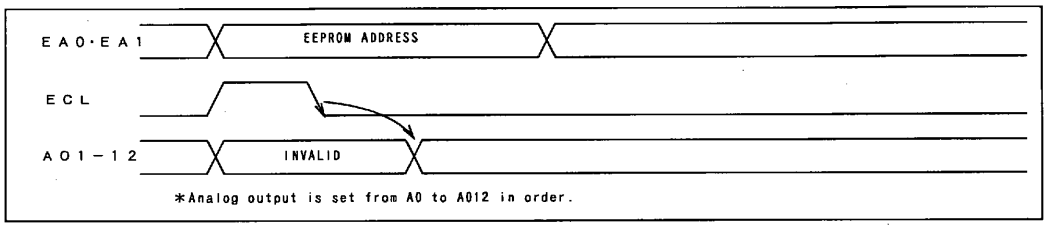
6.READ mode:The data in the internal EEPROM is read from the DO pin.



7.STATUS mode: The DO pin outputs the Ready/$\overline{\text{Busy}}$ status from the DO pin.



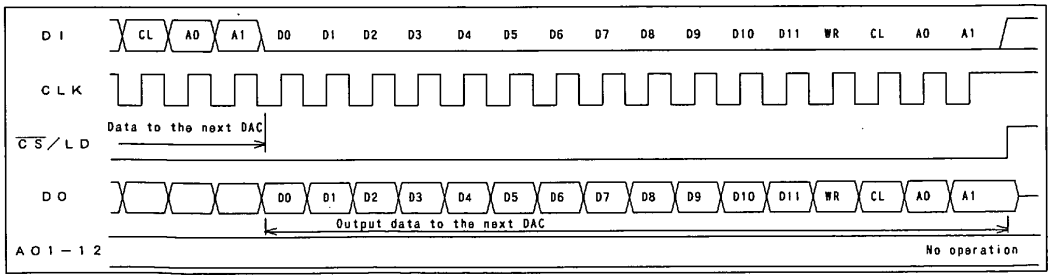
8.ECL function : For "H" pulse to the ECL pin, the data in the selected address in the internal EEPROM is automatically loaded. Then each D/A converter output is settled to pre-determined value.



9. Transfer mode for the cascade connection

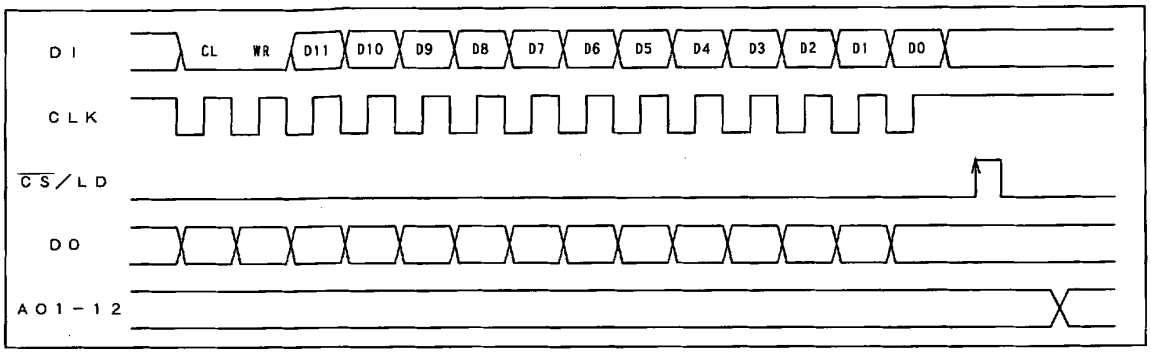
In case that AK9813A devices are connected in cascade, the AK9813A under programming cycle can transfer the data to the other AK9813A. The some AK9813A devices can be operated by the common $\overline{\text{CS}}$ signal at the same time.

Please note that the input data into to the AK9813A under programming cycle should be all"0" when the $\overline{\text{CS}}$ pin is changed from "L" to "H". If data except all"0" is input into the AK9813A under programming cycle, accidental data disturbance may occur.

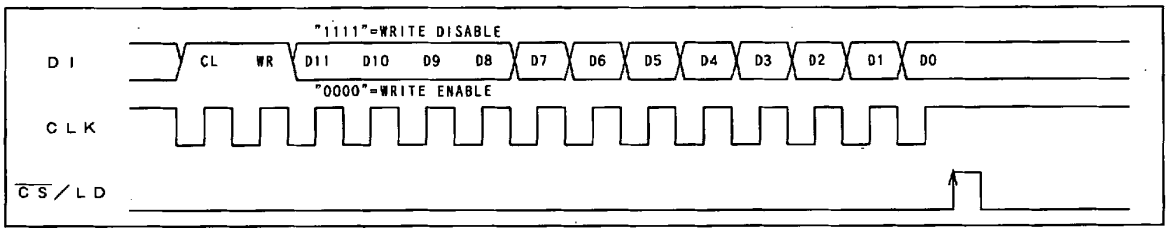


② Timing Diagram for LD I/F (SEL ="L")

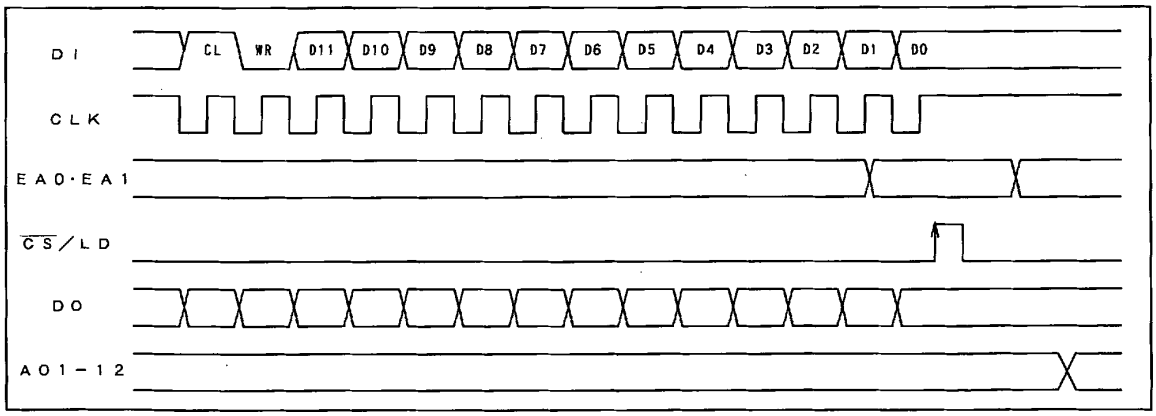
1.DAC mode:The internal EEPROM is not used.



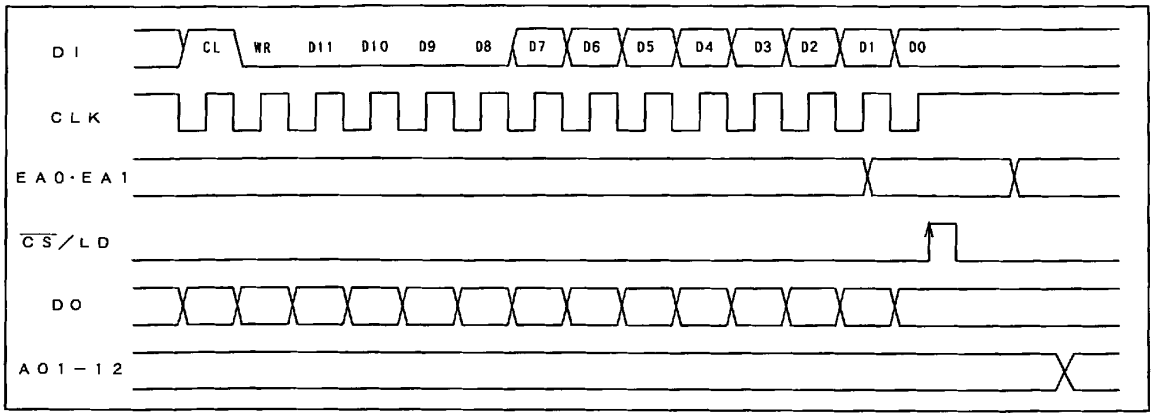
2.WRITE ENABLE/DISABLE mode:The programming state of internal EEPROM is set.



3.CALL mode: The output of the D/A is set by the data in the internal EEPROM.

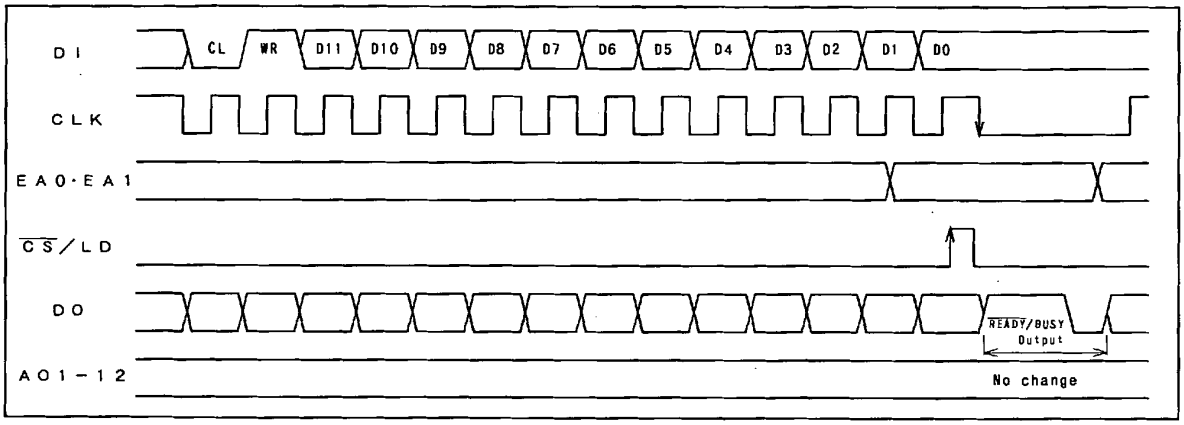


4.ALL CALL mode : The outputs of the all D/As are set by the data in the internal EEPROM.



• The D/A outputs are set from AO1 to AO12 in order.

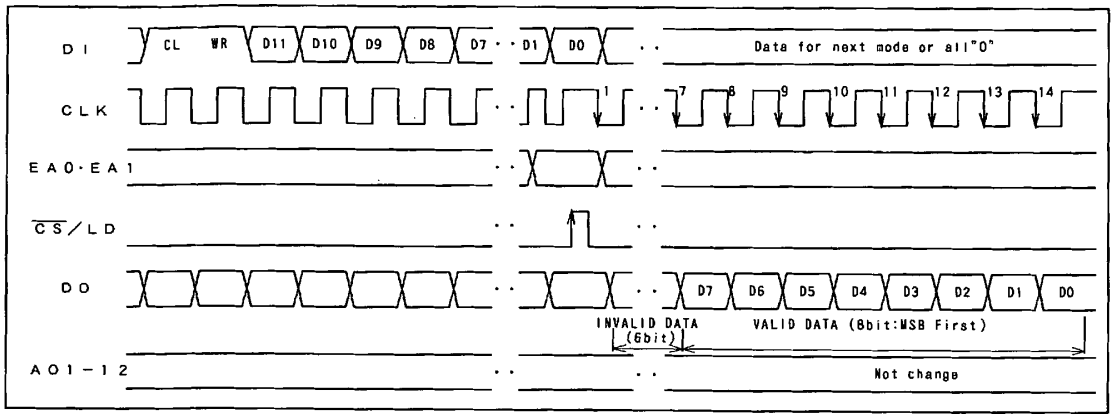
5.WRITE mode:The digital input data for D/A converter is written into the internal EEPROM.



(NOTE)

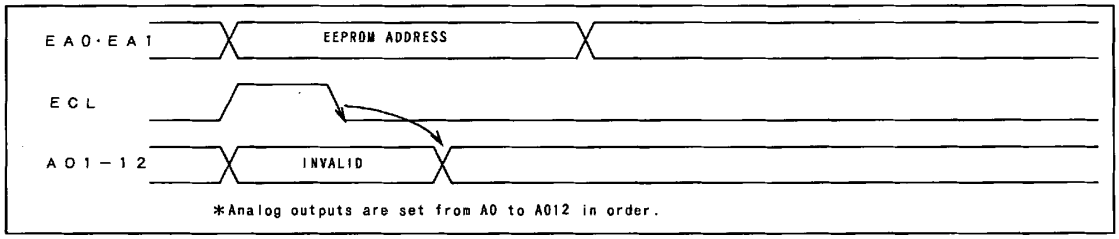
* In case that AK9813A devices are connected in cascade, when a AK9813A device is under programming cycle, the AK9813A device under programming cycle can not transfer the data to the other AK9813A device and some AK9813A devices can not be operated by the common $\overline{CS}$ signal at the same time.
* While programming cycle, the $\overline{CS}$/LD pin should be "L".
* When the $\overline{Ready}$/Busy signal from the DO pin is verified, the $\overline{CS}$ pin should be changed from "H" to "L" and kept at "L". If the $\overline{CS}$ pin is kept at "H", the $\overline{Ready}$/Busy signal does not output correctly.

6.READ mode:The data in the internal EEPROM is read from the DO pin.



7.ECL function:

When the ECL pin received high pulse, the data in EEPROM is automatically loaded to each corresponding D/A, and starting from AO1 to AO12 in order. Then each D/A output is settled to pre-determined value.



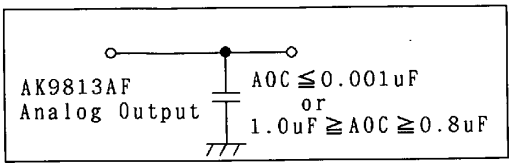
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Spec.	Units
Power Supply	VCC	relative to GND	-0.3~+6.5	V
Input Voltage	VIO	relative to GND	-0.3~VCC+0.3	V
Ambient Temperature	Ta		-10~+85	°C
Storage Temperature	TST		-65~+150	°C

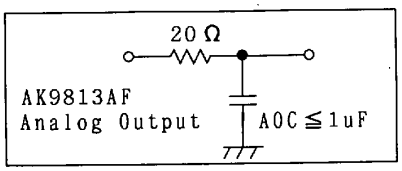
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	min	typ	max	Units
Power Supply 1 (Digital section)	VCC		2.7		5.5	V
Power Supply 2	VDD1	VDD≥VCC	4.5	5.0	5.5	V
(DAC,AMP sections)	VDD2		3.0	3.3	3.6	
Analog Output Source Current 1	IAL	VDD=5.0V±0.5V			1	mA
Analog Output Sink Current 1	IAH				1	mA
Analog Output Source Current 2	IAL	VDD=3.3V±0.3V			500	uA
Analog Output Sink Current 2	IAH				500	uA
Analog Output Load Capacitance	AOC	Load Crcuit-A			0.001	uF
			0.8		1.0	uF
		Load Circuit-B			1.0	uF

•Load Circuit-A



•Load Circuit-B



ELECTRICAL CHARACTERISTICS

■ **DC Characteristics**

(1)Digital Section

(VCC=2.7V~5.5V,VDD=5.0V±0.5V or 3.3V±0.3V(VDD≥VCC),GND,VSS=0V,Ta=-10~85°C)

Parameter	Symbol	Pin	Conditions	min	max	Units
Power Supply (Digital Section)	VCC			2.7	5.5	V
Operating Current (READ) (1)(2)	ICC	VCC	CLK=1MHz		1.5	mA
Leakage Current	ILI	CLK,DI $\overline{CS}$/LD EA0,EA1 ECL,SEL	VIN=VCC	-10.0	10.0	uA
High Level Input Voltage1	VIH	DI EA0,EA1 ECL,SEL		0.5×VCC		V
Low Level Input Voltage1	VIL				0.2×VCC	V
High Level Input Voltage2	VIH	$\overline{CS}$/LD CLK		0.6×VCC		V
Low Level Input Voltage2	VIL				0.15×VCC	V
High Level Output Voltage	VOH1	DO	4.5V≤VCC≤5.5V IOH=-400uA	VCC-0.4		V
	VOH2		2.7V≤VCC<4.5V IOH=-200uA	0.7×VCC		V
Low Level Output Voltage	VOL1		4.5V≤VCC≤5.5V IOL=1.0mA		0.4	V
	VOL2		2.7V≤VCC<4.5V IOL=1.0mA		0.4	V

(1) All input pins are connected to either VCC or GND.

(2) DO=OPEN

(2)Analog Section
(2-1)VDD=5.0V±0.5V

(VCC=2.7V~5.5V,VDD=5.0V±0.5V (VDD≥VCC),GND,VSS=0V,Ta=-10~85°C)

Parameter	Symbol	Pin	Conditions	min	typ	max	Units
Power Supply1 (Analog Section)	VDD1	VDD	VDD≥VCC	4.5	5.0	5.5	V
Power Dissipation1 (Analog Section)	IDD1		AO1~AO12=OPEN			10.0	mA
Resolution	Res	AO1 | AO12			8		bits
Integral (3) Non-Linearity :INL	LE		AO1~AO12=OPEN 0.05V≤AO ≤VDD-0.1V	-1.5		1.5	LSB
Differential Non-Linearity :DNL	D_{LE}			-1.0		2.0	LSB
Buffer-AMP Minimum Output Voltage 1	VAOL1	AO1 | AO12	IAL = 0uA Data= 00(Hex)	GND		0.05	V
Buffer-AMP Minimum Output Voltage 2	VAOL2		IAL = 500uA Data= 00(Hex)	-0.1		0.1	V
Buffer-AMP Minimum Output Voltage 3	VAOL3		IAH = 500uA Data= 00(Hex)	GND		0.1	V
Buffer-AMP Minimum Output Voltage 4	VAOL4		IAL = 1mA Data= 00(Hex)	-0.2		0.2	V
Buffer-AMP Minimum Output Voltage 5	VAOL5		IAH = 1mA Data= 00(Hex)	GND		0.2	V
Buffer-AMP Maximum Output Voltage 1	VAOH1		IAH = 0uA Data= FF(Hex)	VDD-0.1		VDD	V
Buffer-AMP Maximum Output Voltage 2	VAOH2		IAL = 500uA Data= FF(Hex)	VDD-0.2		VDD	V
Buffer-AMP Maximum Output Voltage 3	VAOH3		IAH = 500uA Data= FF(Hex)	VDD-0.2		VDD+0.2	V
Buffer-AMP Maximum Output Voltage 4	VAOH4		IAL = 1mA Data= FF(Hex)	VDD-0.3		VDD	V
Buffer-AMP Maximum Output Voltage 5	VAOH5		IAH = 1mA Data= FF(Hex)	VDD-0.3		VDD+0.3	V

(3) Integral Non-Linearity is the error between the actual line and the ideal line.
The ideal line exhibits a perfect linear D/A converter output characteristic between the input digital data"00" and the input digital data"FF".

(2-2) VDD=3.3V±0.3V

(VCC=2.7V~3.6V,VDD=3.3V±0.3V (VDD≥VCC),GND,VSS=0V,Ta=-10~85°C)

Parameter	Symbol	Pin	Conditions	min	typ	max	Units
Power Supply 2 (Analog Section)	VDD2	VDD	VDD ≥ VCC	3.0	3.3	3.6	V
Power Dissipation2 (Analog Section)	IDD2		AO1~AO12=OPEN			7.0	mA
Resolution	Res	AO1 | AO12			8		bits
Integral (3) Non-Linearity :INL	LE		AO1~AO12=OPEN 0.15V≤AO ≤VDD-0.15V	-1.5		1.5	LSB
Differential Non-Linearity :DNL	D_{LE}			-1.0		2.0	LSB
Output Voltage for Input data "05"			AO1~AO12=OPEN VDD=3.3V		0.1	0.15	V
Output Voltage for Input data "FA"				3.15	3.25		V
Buffer-AMP Minimum Output Voltage 6	VAOL6	AO1 | AO12	IAL = 0uA Data= 00(Hex)	GND		0.05	V
Buffer-AMP Minimum Output Voltage 7	VAOL7		IAL = 250uA Data= 00(Hex)	-0.1		0.1	V
Buffer-AMP Minimum Output Voltage 8	VAOL8		IAH = 250uA Data= 00(Hex)	GND		0.1	V
Buffer-AMP Minimum Output Voltage 9	VAOL9		IAL = 500uA Data= 00(Hex)	-0.2		0.2	V
Buffer-AMP Minimum Output Voltage 10	VAOL10		IAH = 500uA Data= 00(Hex)	GND		0.2	V
Buffer-AMP Maximum Output Voltage 6	VAOH6		IAH = 0uA Data= FF(Hex)	VDD-0.1		VDD	V
Buffer-AMP Maximum Output Voltage 7	VAOH7		IAL = 250uA Data= FF(Hex)	VDD-0.2		VDD	V
Buffer-AMP Maximum Output Voltage 8	VAOH8		IAH = 250uA Data= FF(Hex)	VDD-0.2		VDD+0.2	V
Buffer-AMP Maximum Output Voltage 9	VAOH9		IAL = 500uA Data= FF(Hex)	VDD-0.3		VDD	V
Buffer-AMP Maximum Output Voltage 10	VAOH10		IAH = 500uA Data= FF(Hex)	VDD-0.3		VDD+0.3	V

(3) Integral Non-Linearity is the error between the actual line and the ideal line.
The ideal line exhibits a perfect linear D/A converter output characteristics between the input digital data"05" and the input digital data"FA".

■ **AC Characteristics**

(1) CS I/F, LD I/F : Common Timing

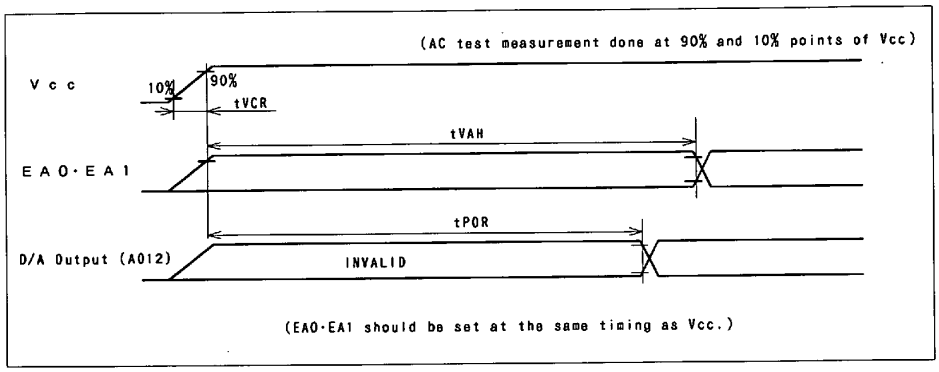
(VCC=2.7V~5.5V,VDD=5.0V±0.5V or 3.3V±0.3V (VDD≥VCC),GND,VSS=0V,Ta=-10~85°C)

Parameter	Symbol	Conditions	min	max	Units
Vcc Rise Time	tVCR			50	ms
Auto Address Hold Time	tVAH		3.5		ms
Auto Read Time	tPOR	Test Load2		3.5	ms
ECL "H" Pulse Width	tECW1	*1	100		ns
	tECW2	*2	250		ns
External Call Time	tECL	Test Load2		3.5	ms
Address Set Up Time	tESU1	*1	50		ns
	tESU2	*2	100		ns
ECL Address Hold Time	tEAH		3.5		ms
Repeat Call Prohibition Time	tECC1	*1	20		ns
	tECC2	*2	100		ns

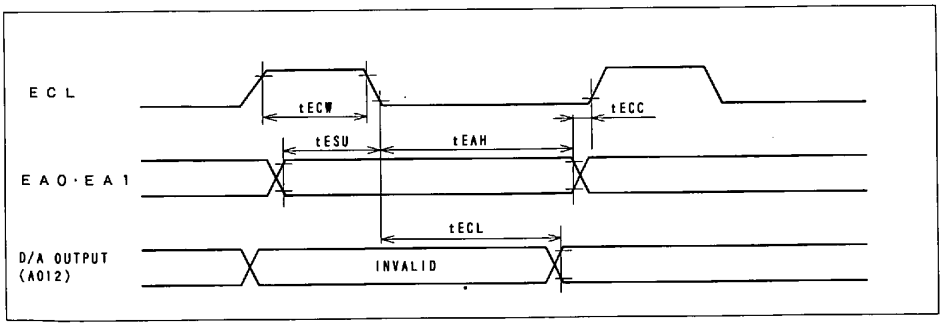
*1:4.5V≤Vcc≤5.5V

*2:2.7V≤Vcc<4.5V

<AUTO READ>



<ECL FUNCTION>



(2)CS I/F Timing

(VCC=2.7V~5.5V,VDD=5.0V±0.5V or 3.3V ± 0.3V (VDD≥VCC),GND,VSS=0V,Ta=-10~85°C)

Parameter	Symbol	Conditions	min	max	Units
Clock "L" Pulse Width	tCKL1	*5	200		ns
	tCKL2	*6	500		ns
Clock "H" Pulse Width	tCKH1	*5	200		ns
	tCKH2	*6	500		ns
Clock Rising Time	tCr				
Clock Falling Time	tCf			200	ns
Data Set Up Time	tDSU1	*5	30		ns
	tDSU2	*6	150		ns
Data Hold Time	tDHD1	*5	60		ns
	tDHD2	*6	150		ns
$\overline{CS}$ Set Up Time	tCSU1	*5	100		ns
	tCSU2	*6	250		ns
$\overline{CS}$ Hold Time	tCCH		200		ns
$\overline{CS}$ "H" Hold Time	tCSH	DAC etc *3,*4,*5	100		ns
		*3,*4,*6	250		ns
		WRITE *4,*5	10		ms
		*4,*6	15		ms
		CALL•READ	15		us
		ALL CALL	3.5		ms
Data Output Enable Time	tDOD1	*5		200	ns
	tDOD2	*6		500	ns
Data Output Float Delay	tDOZ1	*5		200	ns
	tDOZ2	*6		500	ns
Data Output Delay	tDOC1	Test Load1 *5		170	ns
	tDOC2	*6		300	ns
D/A Output Setting Time	tCSD	DAC Test Load2		200	us
		CALL Test Load2		250	us
		ALL CALL Test Load2		3.5	ms
Status Set Up Time	tSSU		100		ns
Status Hold Time	tSHD1	*5	100		ns
	tSHD2	*6	250		ns

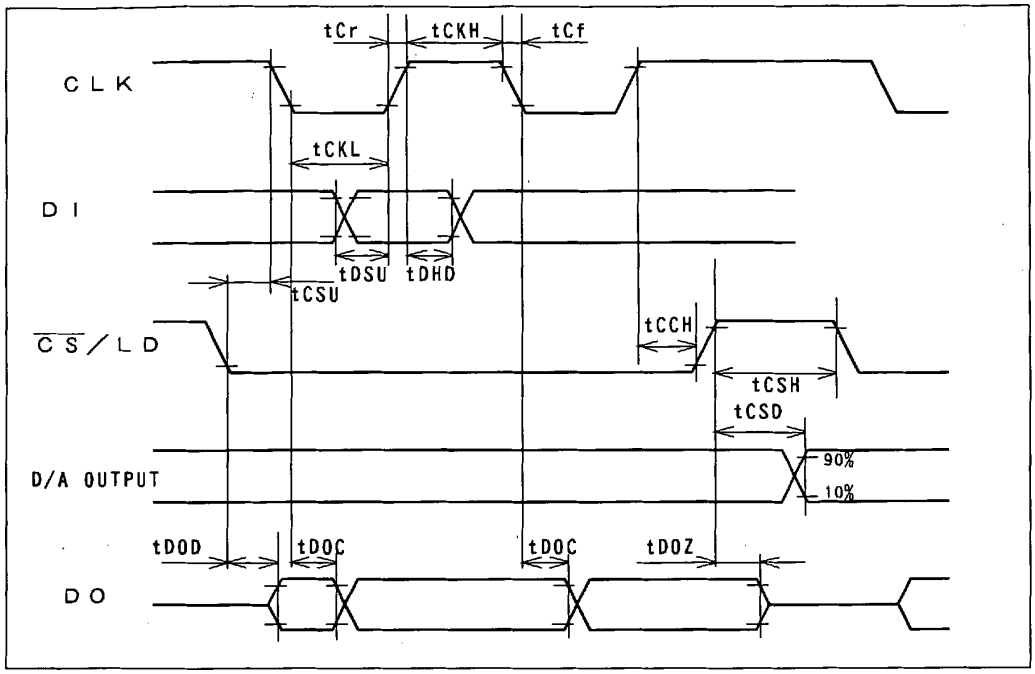
*3: Please refer to "DAC etc" regarding $\overline{CS}$ "H" Hold Time before status mode execute.

*4: If READY/$\overline{BUSY}$="H" is confirmed in status mode in the WRITE mode, the $\overline{CS}$ pin can be changed to "L" shorter than the values specified on above.
Please refer to "DAC etc" regarding $\overline{CS}$ "H" Hold Time in case that AK9813 to be connected in cascade is under programming cycle(READY/$\overline{BUSY}$="L").

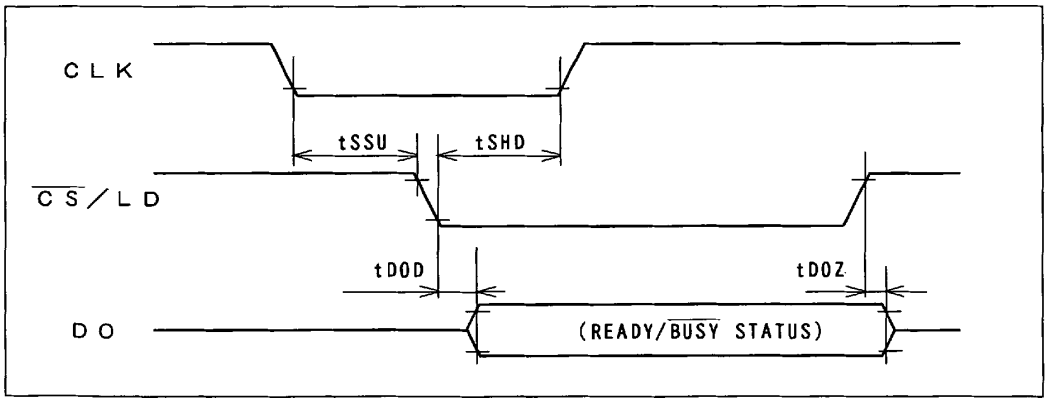
*5: 4.5V≤Vcc≤5.5V

*6: 2.7V≤Vcc<4.5V

<Input/Output Waveform>



<STATUS Output>



(3)LD I/F Timing

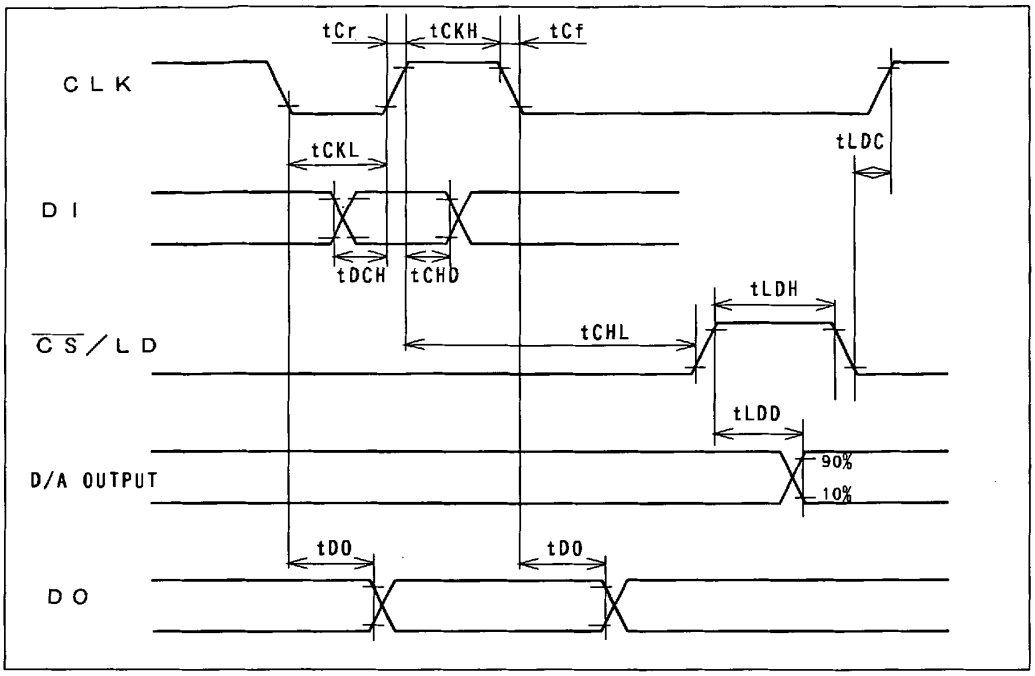
(VCC=2.7V~5.5V,VDD=5.0V±0.5V or 3.3V ± 0.3V (VDD≥VCC),GND,VSS=0V,Ta=-10~85°C)

Parameter	Symbol	Conditions	min	max	Units
Clock "L" Pulse Width	tCKL1	*5	200		ns
	tCKL2	*6	500		ns
Clock "H" Pulse Width	tCKH1	*5	200		ns
	tCKH2	*6	500		ns
Clock Rising Time	tCr				
Clock Falling Time	tCf			200	ns
Data Set Up Time	tDCH1	*5	30		ns
	tDCH2	*6	150		ns
Data Hold Time	tCHD1	*5	60		ns
	tCHD2	*6	150		ns
Load Set Up Time	tCHL		200		ns
Load Hold Time	tLDC1	*5	100		ns
	tLDC2	*6	250		ns
Load "H" Pulse Width	tLDH1	modes except *5	100		ns
	tLDH2	READ mode *6	250		ns
	tLDH3	READ mode	5		us
Data Output Delay	tDO1	Test Load1 *5		170	ns
	tDO2	Test Load1 *6		300	ns
D/A Output Setting Time	tLDDD	DAC Test Load2		200	us
		CALL Test Load2		250	us
		ALL CALL Test Load2		3.5	ms
Address Set Up Time	tASU1	*5	100		ns
	tASU2	*6	200		ns
Write Address Hold Time	tWAHD1	*5	20		ns
	tWAHD2	*6	100		ns
Programming Cycle	tWRT	*7		15	ms
Ready Signal Delay	tRYD	Test Load1		0.4	us
Repeat Write Prohibition Time	tRYH1	Test Load1 *5	20		ns
	tRYH2	Test Load2 *6	100		ns
Read Hold Time	tRHD	CALL,READ mode	15		us
		ALL CALL mode	3.5		ms
Read Address Hold Time	tRAHD	CALL,READ mode	15		us
		ALL CALL mode	3.5		ms

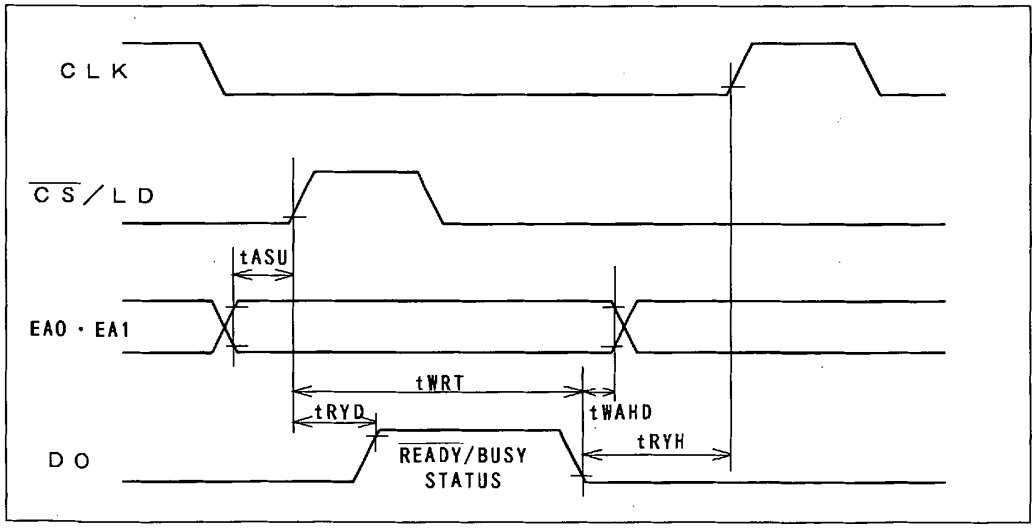
*7: If $\overline{\text{READY}}$/BUSY="L" is confirmed in status mode in the WRITE mode, the next operation can be started.

<Input/Output Waveform>

<Data Timing>

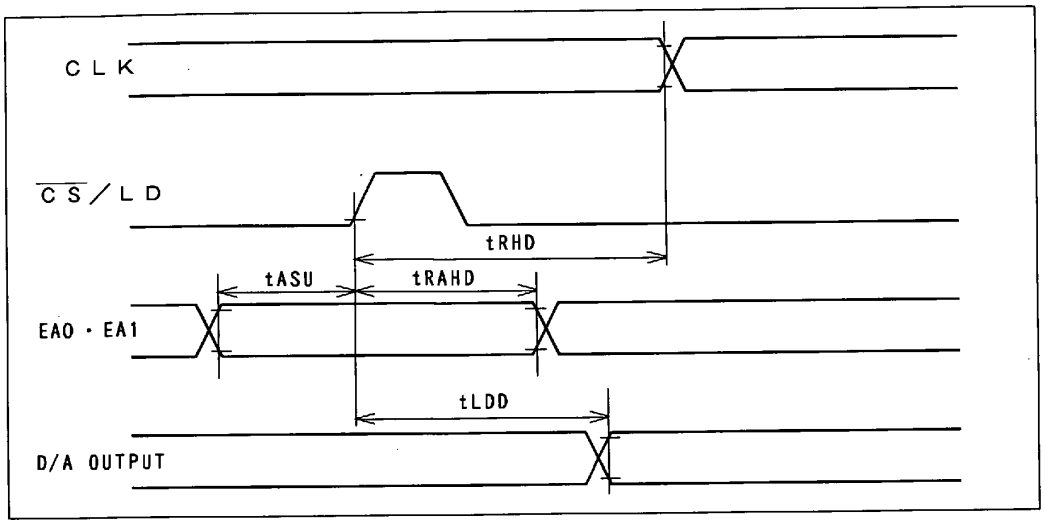


<Write mode>



* Please refer to the data timing regarding the input timing for the DI pin

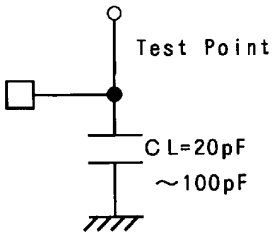
<Call mode>
<All Call mode>
<Read mode>



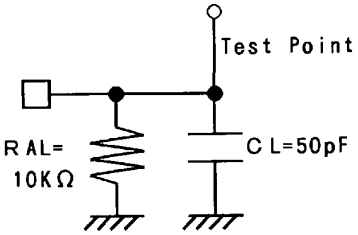
* Please refer to the data timing regarding the input timing for the DI pin

✧ AC measurement circuit

• Test Load1



• Test Load2



• AC test point

Digital Input/Output Level : 50% • 20% of Vcc
Analog Output Level : 90% • 10% of Vcc

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