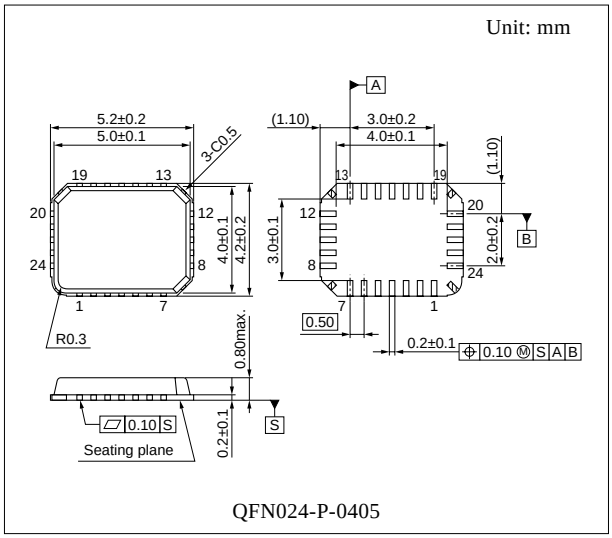
AN6096FHN

Transmission and reception IC for cellular telephone

■ Overview

The AN6096FHN is a transmission and reception IC for a cellular telephone. It is encapsulated in the QFN package which is very thin and very small outline by using our exclusive process method.

It integrates QPSK (Quadrature phase shift keying) modulator for transmission and an IF circuit for reception in a single chip. It contributes to realization of thinner and lighter equipment by adopting a very small package and designing a low power consumption circuit.



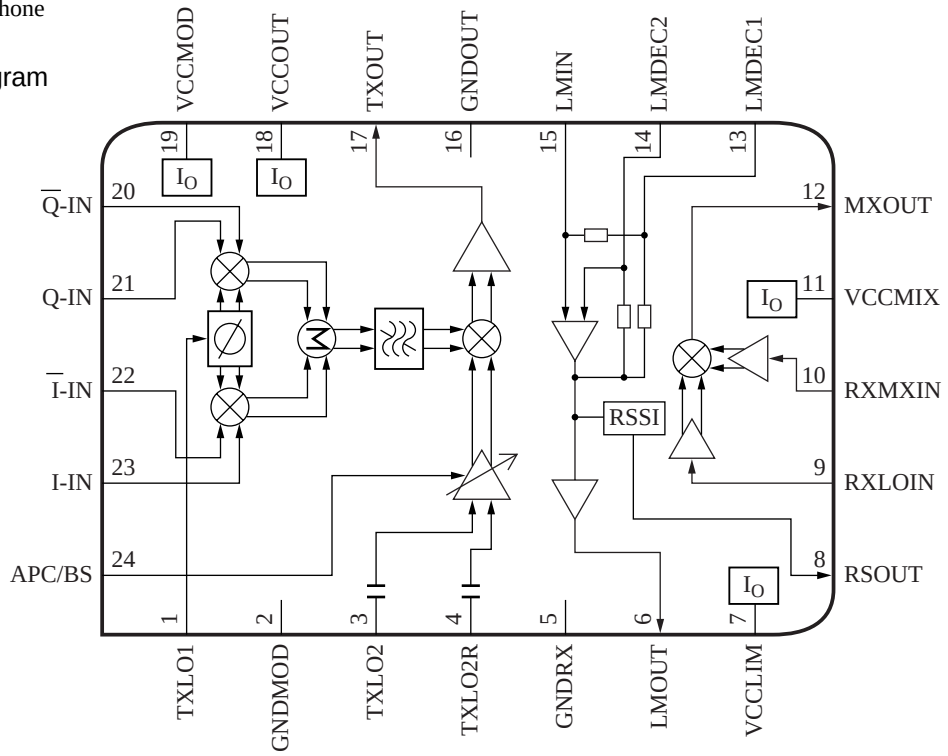
■ Features

- Integrating an orthogonal modulation circuit for transmission and an IF circuit for reception on a single chip
- Low power consumption by using an indirect modulation system in transmission block
- Built-in APC circuit for transmission output adjustment
- High input sensitivity by optimizing circuit in reception circuit
- Built-in RSSI circuit of wide dynamic range in reception block

■ Applications

- Cellular telephone

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	TXLO1	TX local 1-in	13	LMDEC1	Lim. decouple 1
2	GNDMOD	GND TX-mod.	14	LMDEC2	Lim. decouple 2
3	TXLO2	TX local 2	15	LIMIN	Lim. in
4	TXLO2R	TX local 2-ref.	16	GNDOUT	GND TX-out
5	GNDRX	GND-RX	17	TXOUT	TX-output
6	LMOUT	Lim. out	18	VCCOUT	V_{CC} TX-out
7	VCCLIM	V_{CC} lim.	19	VCCMOD	V_{CC} TX-mod.
8	RSOUT	RSSI out	20	$\overline{Q}$-IN	$\overline{Q}$ input
9	RXLOIN	RX local-in	21	Q-IN	Q input
10	RXMXIN	RX mix.-in	22	$\overline{I}$-IN	$\overline{I}$ input
11	VCCMIX	V_{CC} mix.	23	I-IN	I input
12	MXOUT	Mix. out	24	APC / BS	APC / BS

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.2	V
Supply current	I_{CC}	60	mA
Power dissipation *2	P_D	125	mW
Operating ambient temperature *1	T_{opr}	−30 to +80	°C
Storage temperature *1	T_{stg}	−55 to +125	°C

Note) ∗1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

∗2: The power dissipation shown is for the independent IC without a heat sink at T_a = 80°C. Refer to "■ Application Notes".

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	2.7 to 4.0	V

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Consumption current *1 (Transmission)	I_{CCTX}	Lo1 = 178 MHz, –25 dBm Lo2 = 1 619 MHz, –20 dBm V_{APC} = 2.3 V	—	25	33	mA
Sleep current *1	I_{SLTX}	No signal, $V_{APC/BS}$ = 0 V	—	0	10	µA
Output level 1 *1	P_{O1}	Lo1 = 178 MHz, –25 dBm Lo2 = 1 607 MHz, –20 dBm V_{APC} = 2.3 V	–16	–13	—	dBm
Output level 2 *1	P_{O2}	Lo1 = 178 MHz, –25 dBm Lo2 = 1 631 MHz, –20 dBm V_{APC} = 2.3 V	–16	–13	—	dBm
Minimum output level *1	P_{min}	Lo1 = 178 MHz, –25 dBm Lo2 = 1 619 MHz, –20 dBm V_{APC} = 1.0 V	—	–50	–43	dBm
Consumption current (Reception) *2	I_{CCRX}	No signal	—	3.2	4.5	mA
Mix. conversion gain *2	G_{MX}	V_{M1} = 60 dBµ, SW1 = b Filter loss: except for –5.5 dB	21	23.5	26	dB
Mix. maximum output amplitude *2	V_{MX}	V_{M1} = 105 dBµ, SW1 = b Filter loss: except for –5.5 dB	101	107	—	dBµ
Lim. voltage gain *2	G_{LM}	V_{L1} = 15 dBµ	80	85	90	dB
Lim. maximum output amplitude *2	V_{LM}	V_{L1} = 80 dBµ, 400 kHz component	0.90	1.25	1.60	V[p-p]
RSSI output voltage 1 *2	V_{S1}	V_{L1} = 0 dBµ	0	0.23	0.6	V
RSSI output voltage 2 *2	V_{S2}	V_{L1} = 115 dBµ	2.31	2.6	2.91	V
RSSI reference output inclination *3	D_S	$V_S (V_{IS}) = V_{S1} + 0.12$ V $D_S = V_S (V_{IS} + 75$ dBµ$) – V(V_{IS})$	1.39	1.8	2.19	V
RSSI output inclination variation 1 *3	ΔD_{S1}	$\Delta D_{S1} = 5\{V_S (V_{IS} + 15$ dBµ$)$ $– V_S (V_{IS})\}/ D_S$	0.75	1	1.25	—
RSSI output inclination variation 2 *3	ΔD_{S2}	$\Delta D_{S2} = 5\{V_S (V_{IS} + 30$ dBµ$)$ $– V_S (V_{IS} + 15$ dBµ$)\}/ D_S$	0.75	1	1.25	—
RSSI output inclination variation 3 *3	ΔD_{S3}	$\Delta D_{S3} = 5\{V_S (V_{IS} + 45$ dBµ$)$ $– V_S (V_{IS} + 30$ dBµ$)\}/ D_S$	0.75	1	1.25	—
RSSI output inclination variation 4 *3	ΔD_{S4}	$\Delta D_{S4} = 5\{V_S (V_{IS} + 60$ dBµ$)$ $– V_S (V_{IS} + 45$ dBµ$)\}/ D_S$	0.75	1	1.25	—
RSSI output inclination variation 5 *3	ΔD_{S5}	$\Delta D_{S5} = 5\{V_S (V_{IS} + 75$ dBµ$)$ $– V_S (V_{IS} + 60$ dBµ$)\}/ D_S$	0.75	1	1.25	—

Note) ∗1: V_{CC} = 3.0 V, IQ signal amplitude: 0.35 V[p-p] (single phase), DC bias: 1.6 V, π/4 QPSK modulation wave
Output frequency of P_{O1}: 1 429.002 5 MHz, Output frequency of P_{O2}: 1 453.002 5 MHz,
Output frequency of P_{min}: 1 441.002 5 MHz
Lo input level is a setting value of signal source (output impedance 50 Ω).

∗2: V_{CC2} = 3.0 V, SW1 = a, V_{LO3} = 90 dBµ: f = 129.6 MHz, V_{M1}: f = 130 MHz, V_{L1}: f = 400 kHz (input level of pin 15 excluding the attenuation by matching circuit and filter.) V_{MX} and V_{LM} are measured in high impedance unless otherwise specified. Lo input level is a setting value of signal source (output impedance 50 Ω).

∗3: V_{IS} is the input level of which the RSSI output voltage becomes V_{S1} + 0.12 V.

■ Electrical Characteristics at T_a = 25°C (continued)

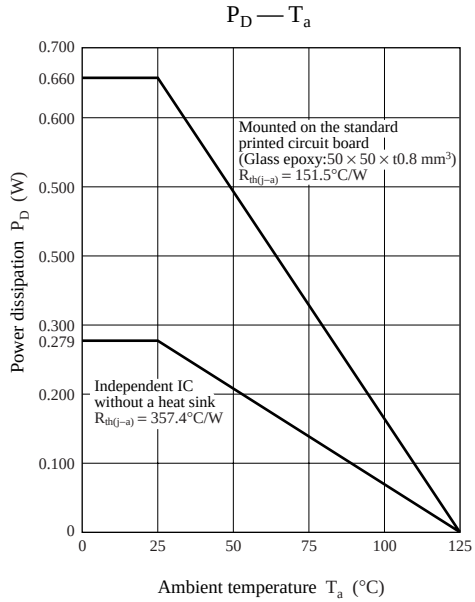
- Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.
V_{CC1} = 3.0 V unless otherwise specified.
Lo input level is a setting value of signal source (output impedance 50 Ω).

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Carrier leak suppression amount ($f_{LO2} - f_{LO1}$)	CL	Lo1 = 178 MHz, −25 dBm Lo2 = 1 619 MHz, −20 dBm V_{APC} = 2.3 V IO: DC offset adjustment	—	−35	—	dBc
Image leak suppression amount	IL	Lo1 = 178 MHz, −25 dBm Lo2 = 1 619 MHz, −20 dBm V_{APC} = 2.3 V, IO: level adjustment	—	−35	—	dBc
Near spurious suppression amount	DU	Lo1 = 178 MHz, −25 dBm Lo2 = 1 619 MHz, −20 dBm V_{APC} = 2.3 V	—	−70	−65	dBc
Base band distortion suppression amount	BD	Lo1 = 178 MHz, −25 dBm Lo2 = 1 619 MHz, −20 dBm V_{APC} = 2.3 V	—	−40	—	dBc
Adjacent channel leakage power suppression amount (30 kHz detuning)	BL1	Lo1 = 178 MHz, −25 dBm Lo2 = 1 619 MHz, −20 dBm V_{APC} = 2.3 V	—	−45	−38	dBc
Adjacent channel leakage power suppression amount (50 kHz detuning)	BL2	Lo1 = 178 MHz, −25 dBm Lo2 = 1 619 MHz, −20 dBm V_{APC} = 2.3 V	—	−70	−60	dBc
Adjacent channel leakage power suppression amount (100 kHz detuning)	BL3	Lo1 = 178 MHz, −25 dBm Lo2 = 1 619 MHz, −20 dBm V_{APC} = 2.3 V	—	—	−65	dBc
APC variable width	L_{APC}	Lo1 = 178 MHz, −25 dBm Lo2 = 1 619 MHz, −20 dBm V_{APC} = 1.0 V to 2.3 V	30	37	—	dB
APC output level control sensitivity	S_{APC}	Lo1 = 178 MHz, −25 dBm Lo2 = 1 619 MHz, −20 dBm V_{APC} = 1.0 V / 1.6 V	—	46	—	dB/V
In-band output level deviation	ΔP	Lo1 = 178 MHz, −25 dBm Lo2 = 1 607 MHz to 1 631 MHz, −20 dBm V_{APC} = 2.3 V	−1.5	—	+1.5	dB
Modulation precision	EVM	Lo1 = 178 MHz, −25 dBm Lo2 = 1 619 MHz, −20 dBm V_{APC} = 2.3 V	—	2.0	—	%rms

■ Application Notes

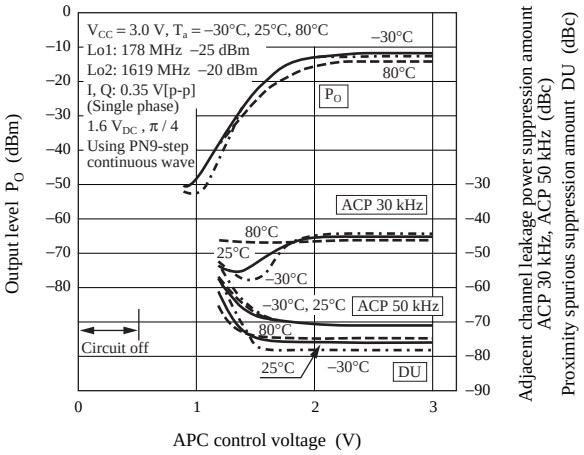
- P_D — T_a curves of QFN024-P-0405



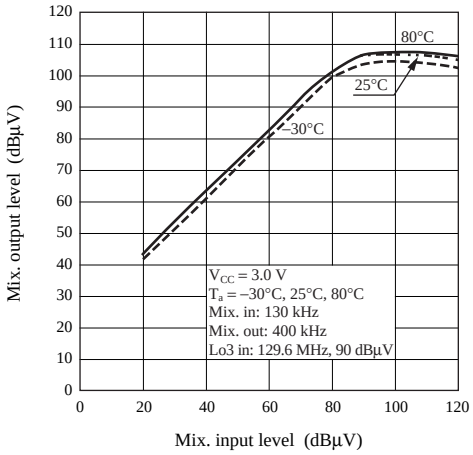
- Main characteristics

Note) Test conditions are the same as "■ Electrical Characteristics" unless otherwise specified.
The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

APC control voltage characteristics



Mix. characteristics

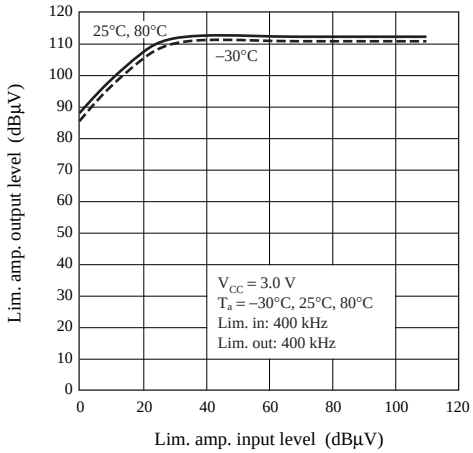


■ Application Notes (continued)

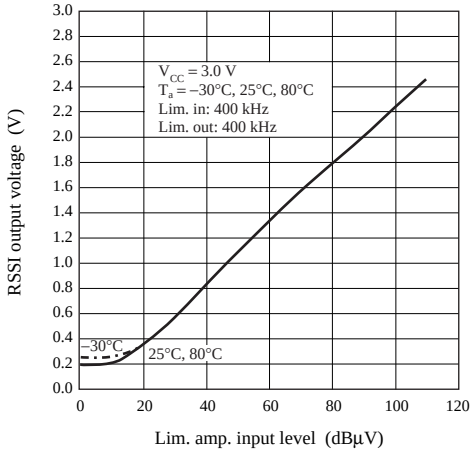
- Main characteristics (continued)

Note) Test conditions are the same as "■ Electrical Characteristics" unless otherwise specified.
The characteristic values below are theoretical values for designing and not guaranteed.

Proximity spurious suppression



RSSI characteristics



■ Application Circuit Example