

HAT2033R/HAT2033RJ

Silicon N Channel Power MOS FET
High Speed Power Switching

HITACHI

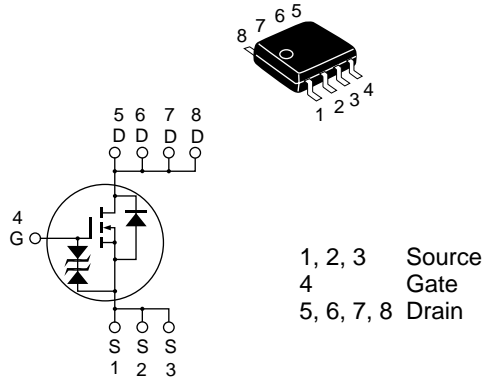
ADE-208-664B (Z)
3rd. Edition
February 1999

Features

- For Automotive Application (at Type Code “J “)
- Low on-resistance
- Capable of 4 V gate drive
- High density mounting

Outline

SOP-8



Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item		Symbol	Ratings	Unit
Drain to source voltage		V_{DSS}	60	V
Gate to source voltage		V_{GSS}	± 20	V
Drain current		I_D	7	A
Drain peak current		$I_{D(pulse)}$ ^{Note1}	56	A
Body-drain diode reverse drain current		I_{DR}	7	A
Avalanche current	HAT2033R	I_{AP} ^{Note4}	—	—
	HAT2033RJ		7	A
Avalanche energy	HAT2033R	E_{AR} ^{Note4}	—	—
	HAT2033RJ		4.2	mJ
Channel dissipation		P_{ch} ^{Note2}	2.5	W
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature		T_{stg}	- 55 to + 150	$^\circ\text{C}$

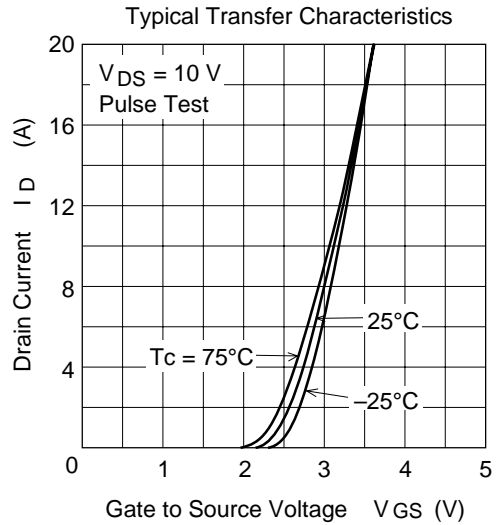
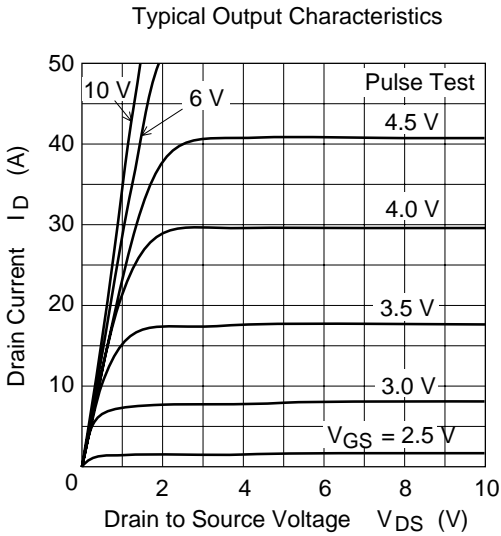
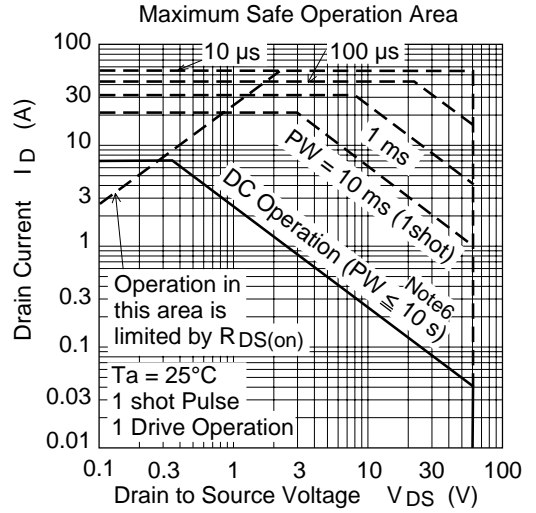
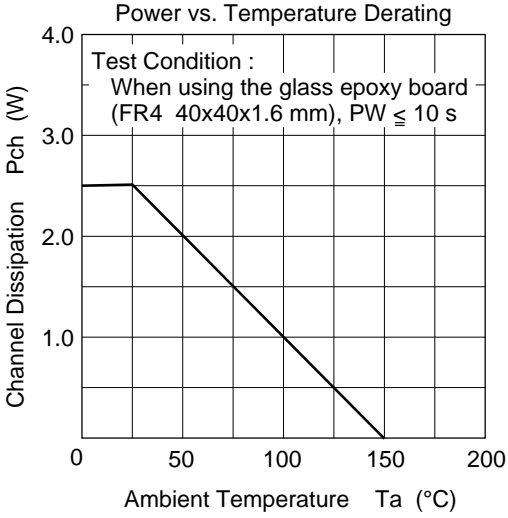
- Note:
1. $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$
 2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10\text{s}$
 3. Value at $T_{ch}=25^\circ\text{C}$, $R_g \geq 50\Omega$

Electrical Characteristics (Ta = 25°C)

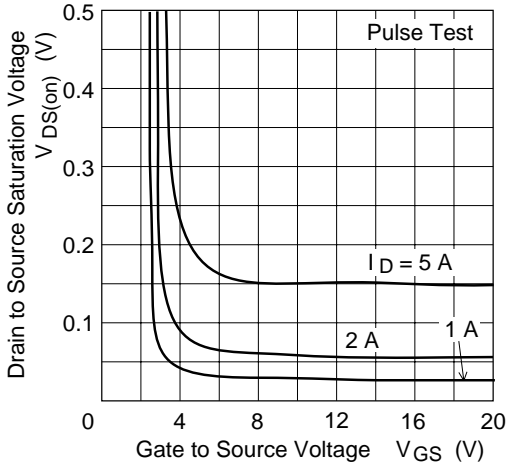
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage		$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current		I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage	HAT2033R	I_{DSS}	—	—	1	μA	$V_{DS} = 60 \text{ V}, V_{GS} = 0$
drain current	HAT2033RJ	I_{DSS}	—	—	0.1	μA	
Zero gate voltage	HAT2033R	I_{DSS}	—	—	—	μA	$V_{DS} = 4 \text{ 8V}, V_{GS} = 0$
drain current	HAT2033RJ	I_{DSS}	—	—	10	μA	Ta = 125°C
Gate to source cutoff voltage		$V_{GS(off)}$	1.2	—	2.2	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state		$R_{DS(on)}$	—	0.03	0.038	Ω	$I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
resistance		$R_{DS(on)}$	—	0.04	0.053	Ω	$I_D = 4 \text{ A}, V_{GS} = 4 \text{ V}$ ^{Note4}
Forward transfer admittance		$ y_{fs} $	6.5	10	—	S	$I_D = 4 \text{ A}, V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance		Ciss	—	740	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance		Coss	—	370	—	pF	$V_{GS} = 0$
Reverse transfer capacitance		Crss	—	130	—	pF	f = 1MHz
Turn-on delay time		$t_{d(on)}$	—	13	—	ns	$V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$
Rise time		t_r	—	55	—	ns	$V_{DD} \cong 30 \text{ V}$
Turn-off delay time		$t_{d(off)}$	—	140	—	ns	
Fall time		t_f	—	95	—	ns	
Body–drain diode forward voltage		V_{DF}	—	0.82	1.07	V	$I_F = 7 \text{ A}, V_{GS} = 0$ ^{Note4}
Body–drain diode reverse recovery time		t_{rr}	—	45	—	ns	$I_F = 7 \text{ A}, V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Note: 4. Pulse test

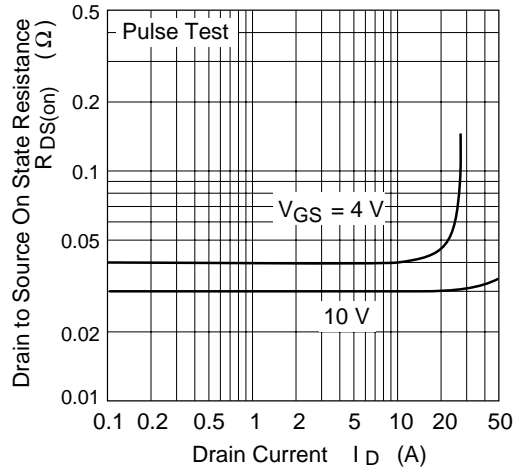
Main Characteristics



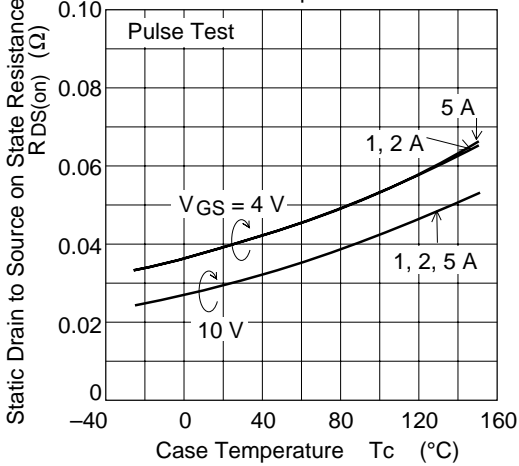
Drain to Source Saturation Voltage vs. Gate to Source Voltage



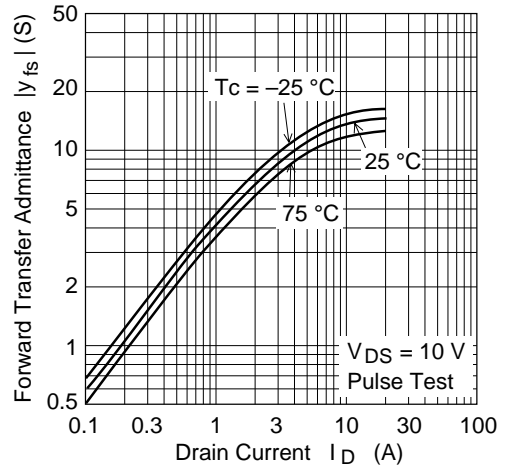
Static Drain to Source on State Resistance vs. Drain Current

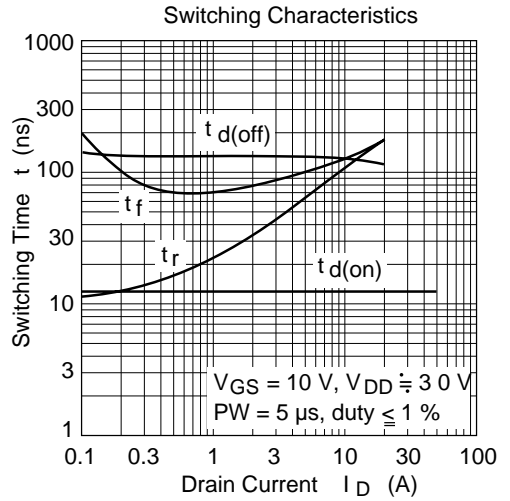
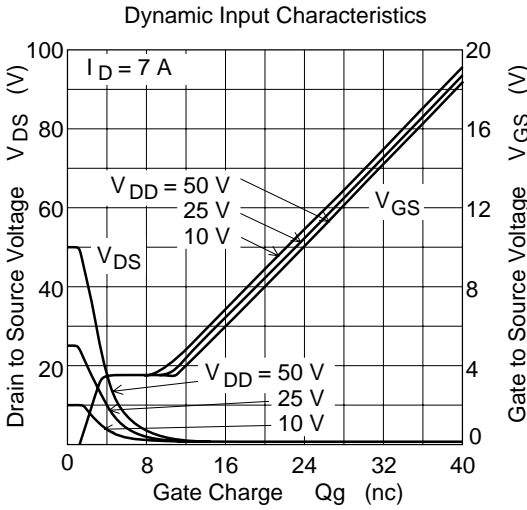
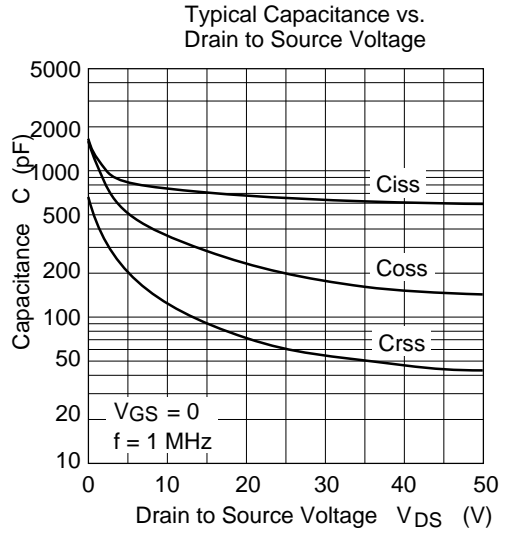
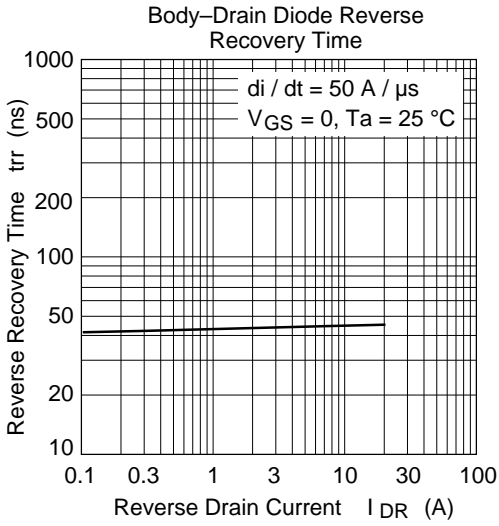


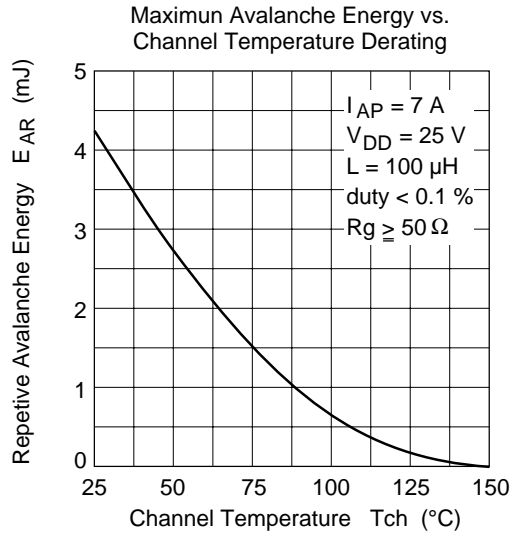
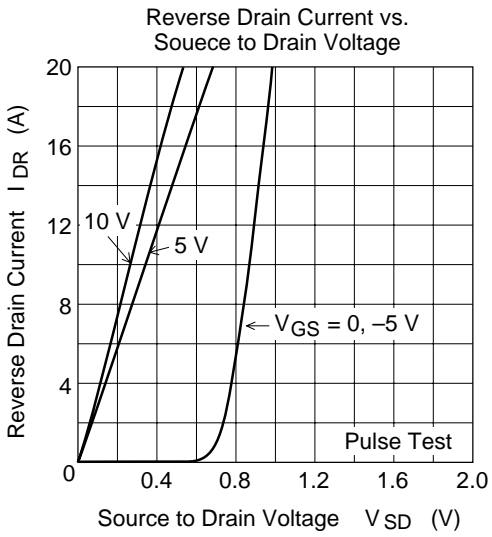
Static Drain to Source on State Resistance vs. Temperature



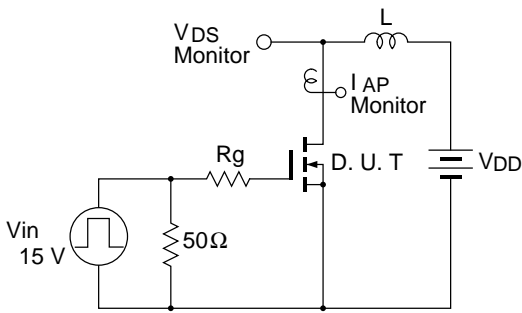
Forward Transfer Admittance vs. Drain Current





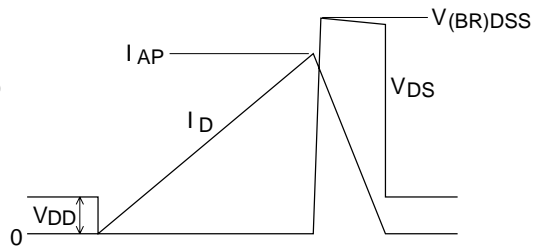


Avalanche Test Circuit

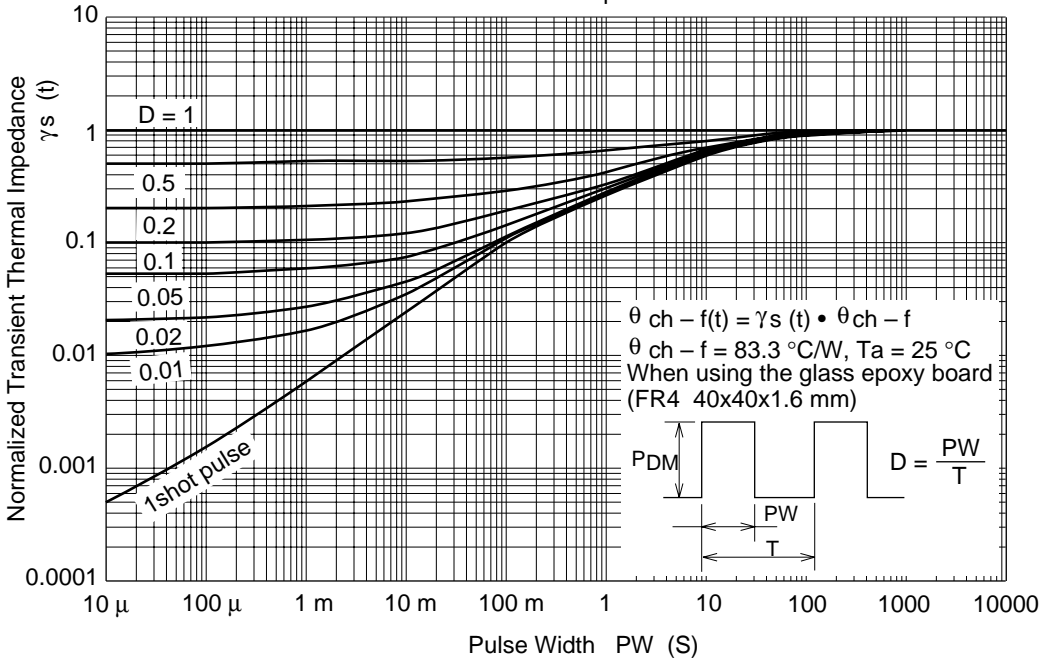


Avalanche Waveform

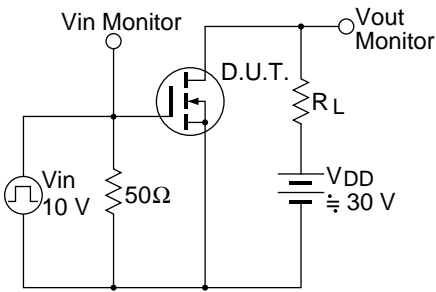
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



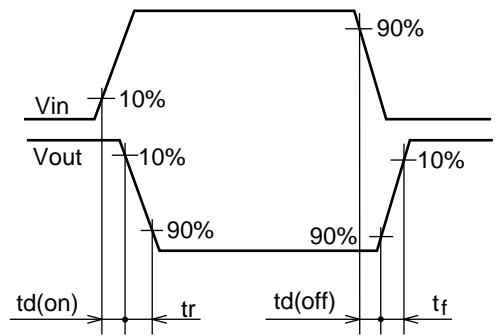
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

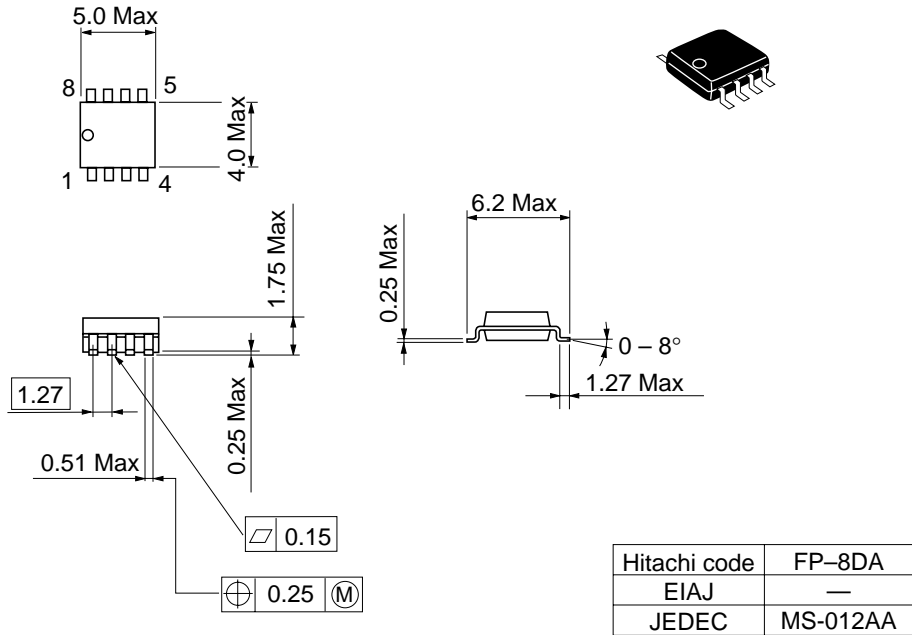


Switching Time Waveform



Package Dimensions

Unit: mm



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