Silicon Bipolar RFIC
900 MHz Vector Modulator

Technical Data

HPMX-2003

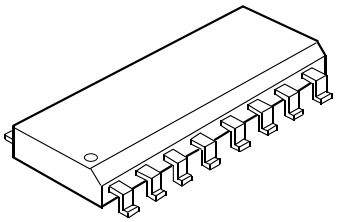
Features

- **800–1000 MHz Output Frequency Range**
- **+6 dBm Peak P_{out}**
- **Unbalanced 50 Ω Output**
- **Internal 90° Phase Shifter**
- **5 Volt, 36 mA Bias**
- **SO-16 Surface Mount Package**

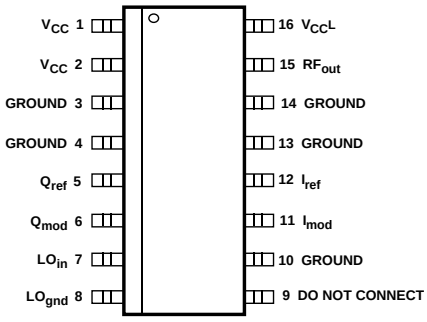
Applications

- **Direct Modulator for 900 MHz Cellular Telephone Handsets, Including GSM, JDC, and NADC**
- **Direct Modulator for 900 MHz ISM Band Spread-Spectrum Transmitters and LANs**

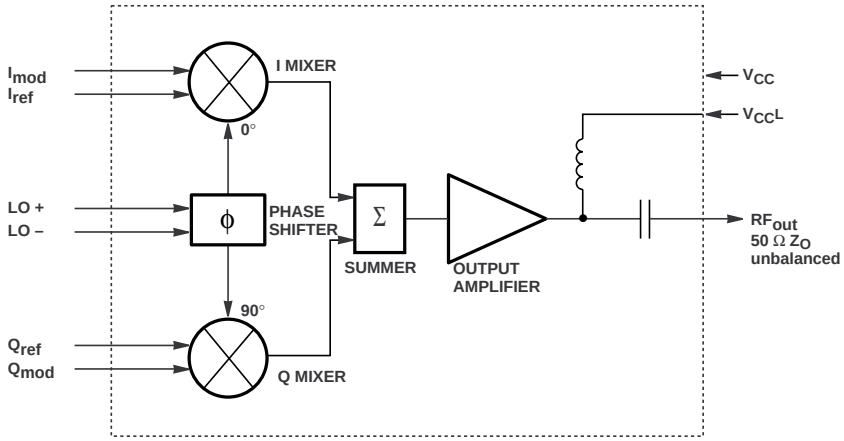
Plastic SO-16 Package



Pin Configuration



Functional Block Diagram



Description

Hewlett Packard's HPMX-2003 is a Silicon RFIC direct conversion vector modulator designed for use at output frequencies between 800 MHz and 1 GHz. Housed in a SO-16 surface mount plastic package, the IC contains two matched Gilbert cell mixers, an RC phase shifter, a summer, and an output amplifier complete with 50 Ω impedance match and DC block.

This device is suitable for use in direct and offset-loop modulated portable and mobile telephone handsets for cellular systems such as GSM, North American Digital Cellular and Japan Digital Cellular. It can also be used in digital transmitters operating in the 900 MHz ISM (Industrial-Scientific-Medical) band, including use in Local Area Networks (LANs).

The HPMX-2003 is fabricated with Hewlett-Packard's 25 GHz ISOSAT-II process, which combines stepper lithography, ion-implantation, self-alignment techniques, and gold metallization to produce RFICs with superior performance, uniformity and reliability.

HPMX-2003 Absolute Maximum Ratings, T_A = 25°C

Symbol	Parameter	Units	Absolute Maximum[1]
P_{diss}	Power Dissipation[2,3]	mW	500
LO_{in}	LO Input Power	dBm	15
V_{CC}	Supply Voltage	V	10
ΔV_{Imod}, ΔV_{Qmod}	Swing of V_{Imod} about V_{Iref}[4] or V_{Qmod} about V_{Qref}	V_{p-p}	5[4]
V_{Iref}, V_{Qref}	Reference Input Levels[4]	V	5[4]
T_{STG}	Storage Temperature	°C	-65 to +150
T_j	Junction Temperature	°C	150

Thermal Resistance[2]:
θ_{jc} = 125°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_C = 25°C (T_C is defined to be the temperature at the end of pin 3 where it contacts the circuit board).
3. Derate at 8 mW/°C for T_C > 88°C.
4. Do not exceed V_{CC} by more than 0.8 V.

HPMX-2003 Guaranteed Electrical Specifications, T_A = 25°C, Z_O = 50 Ω

V_{CC} = 5 V, LO= -12 dBm at 900 MHz (Unbalanced Input), V_{Iref} = V_{Qref} = 2.5 V (Unless Otherwise Noted).

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_d	Device Current	mA		36	44
P_{out}	Output Power $V_{Imod} = V_{Qmod} = 3.75$ V	dBm	+4.0	+6	
LO_{leak}	P_{out} - LO at Output $V_{Imod} = V_{Qmod} = 2.5$ V	dBc	+30	+37	
ε_{mod}	Average Modulation Error $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2} = 1.25$ V	%		4	7

HPMX-2003 Summary Characterization Information, T_A = 25°C, Z_O = 50 Ω

V_{CC} = 5 V, LO = -12 dBm at 900 MHz (Unbalanced Input), V_{Iref} = V_{Qref} = 2.5 V (Unless Otherwise Noted).

Symbol	Parameters and Test Conditions	Units	Typ.
R_{in}	Input Resistance (I_{mod} to I_{ref} or Q_{mod} to Q_{ref})	Ω	10 k
R_{in-gnd}	Input Resistance to Ground (Any I, Q Pin to Ground)	Ω	10 k
$VSWR_{LO}$	LO VSWR (50 Ω) GSM: 890-915 MHz Bandwidth NADC: 824-850 MHz Bandwidth JDC: 940-960 MHz Bandwidth		1.5:1 1.5:1 1.5:1
$VSWR_O$	Output VSWR (50 Ω) (Tuned by Placement of V_{ccL} Capacitor – See Figures 22, 32, and 42) GSM: 890-915 MHz Bandwidth NADC: 824-850 MHz Bandwidth JDC: 940-960 MHz Bandwidth		1.2:1 1.1:1 1.2:1
	Output Noise Floor $V_{Imod} = V_{Qmod} = 3.75$ V	dBm/Hz	-134
IM_3	DSB Third Order Intermodulation Products	dBc	+34
A_i	RMS Amplitude Error	dB	0.3
P_i	RMS Phase Error	degrees	2

HPMX-2003 Pin Description

V_{CC} (pins 1,2)

These two pins provide DC power to the mixers in the RFIC, and are connected together internal to the package. They should be connected to a 5 V supply, with appropriate AC bypassing (1000 pF typ.) used near the pins, as shown in figures 1 and 2. **The voltage on these pins should always be kept *at least 0.8 V more positive* than the DC level on any of pins 5, 6, 11, or 12.** Failure to do so may result in the modulator drawing sufficient current through the data or reference inputs to damage the IC.

Ground (pins 3, 4, 10, 13 & 14)

These pins should connect with minimal inductance to a solid ground plane (usually the backside of the PC board). Recommended assembly employs multiple plated through via holes where these leads contact the PC board.

I_{ref} (pin 12) and Q_{ref} (pin 5), I (pin 11) and Q (pin 6) Inputs

The I and Q inputs are designed for unbalanced operation but can be driven differentially with similar performance. The recommended level of unbalanced I and Q signals is 2.5 V_{p-p} with an average level of 2.5 V above ground. The reference pins should be DC biased to this average data signal level (V_{CC}/2 or 2.5 V typ.). For single ended drive, pins 5 and 12 can be tied together. For balanced operation, 2.5 V_{p-p} signals may be applied across the I_{mod}/I_{ref} and the Q_{mod}/Q_{ref} pairs. The average level of all four signals should be about 2.5 V above ground. The impedance between any I or Q and ground is typically 10 K Ω and the impedance between I_{mod} and I_{ref} or Q_{mod} and Q_{ref} is typically 10 KΩ. The input bandwidth typically exceeds 40 MHz. It is possible to reduce LO leakage through the IC by applying slight DC imbalances between I_{mod} and I_{ref} and/or Q_{mod} and Q_{ref} (see section entitled "HPMX-2003 Using Offsets to Improve Lo Leakage"). All performance data shown on this data sheet was taken with unbalanced I/Q inputs.

LO Input (pins 7 and 8)

The LO input of the HPMX-2003 is balanced and matched to 50 For drive from an unbalanced LO, pin 7 should be AC coupled to the LO using a 50 Ω transmission line and a blocking capacitor (1000 pF typ.), and pin 8 should be AC grounded (1000 pF capacitor typ.), as shown in figure 1. For drive from a balanced LO source, 50 Ω transmission lines and blocking capacitors (1000 pF typ.) are used on both pins 7 and 8, as shown in figure 2. The internal phase shifter allows operation from 800 - 1000 MHz. The recommended LO input level is -12 dBm. All performance data shown on this data sheet was taken with unbalanced LO operation.

RF Output (pin15)

The RF output of the HPMX-2003 is configured for unbalanced operation. The output is internally DC blocked and matched to 50 Ω, so a simple 50 Ω microstrip line is all that is required to connect the modulator to other circuits.

V_{CCL} (pin 16)

Pin 16 is the V_{CC} input for the output stage of the IC. It is **not** internally connected to the other V_{CC} pins. The external connection allows the addition of a small inductor (0 - 6 nH) to tune the output for minimum VSWR, depending upon the operating frequency.

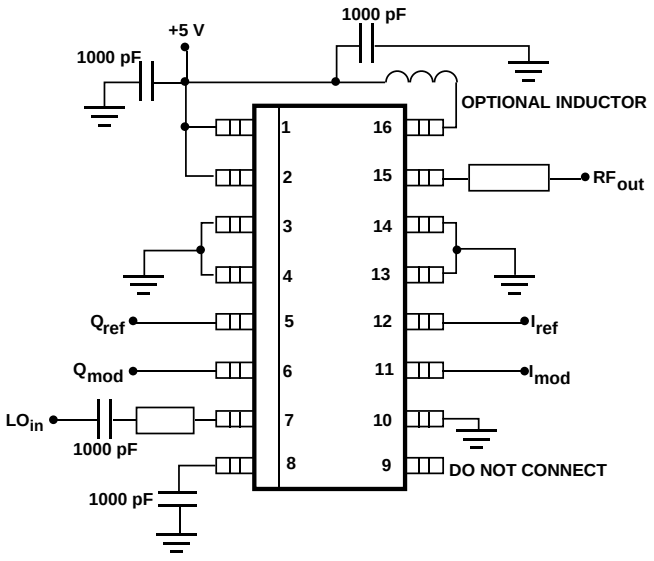


Figure 1. HPMX-2003 Connections Showing Unbalanced LO and I, Q Inputs.

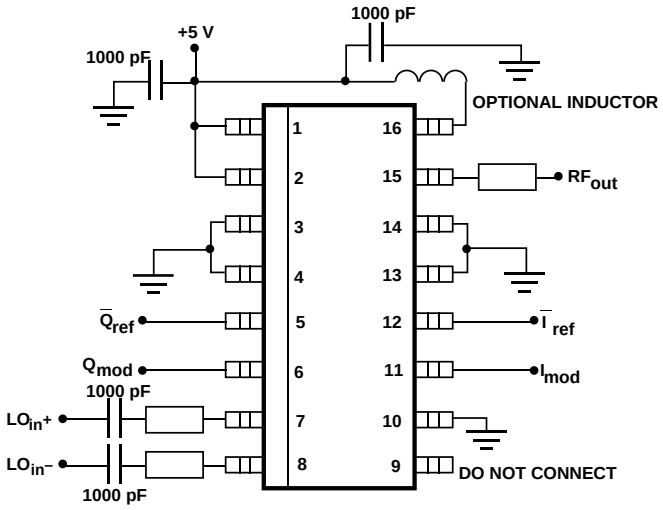


Figure 2. HPMX-2003 Connections Showing Balanced LO and I, Q Inputs.

HPMX-2003 Typical Data Measurement

Direct measurement of the amplitude and phase error at the output is an accurate way to evaluate modulator performance. By measuring the error directly, all the harmonics, LO leakage, etc. that show up in the output signal are accounted for. Figure 3, below, shows the test setup that was used to create the amplitude and phase error plots (figures 12 and 13).

Amplitude and phase error are measured by using the four channel power supply to simulate I and Q input signals. Real 2.5 V_{p-p} I and Q signals would swing 1.25 volts above and below an average 2.5 V level, therefore, a "high" level input is simulated by applying 3.75 V, and a "low" level by applying 1.25 V to the I and/or Q inputs.

Amplitude and phase are measured by setting the network analyzer for an S_{21} measurement at frequency of choice. Set the port 1 stimulus level to the LO level you intend to use in your circuit (-12 dBm for the data sheet). A 6-10 dB attenuator can be placed in the line to port 2 to prevent network analyzer overload, depending upon the network analyzer you are using.

By adjusting the V_{Imod} and V_{Qmod} settings you can step around the I, Q vector circle, reading magnitude and phase at each point. The relative values of phase and amplitude at the various points will indicate the accuracy of the modulator. Note: you must use very low ripple power supplies for the reference, V_{Imod}, and V_{Qmod} supplies. Ripple or noise of only a few millivolts will appear as wobbling phase readings on the network analyzer.

The same test setup shown below is used to measure input and output VSWR, reverse isolation, and power vs. frequency. V_{Imod} and V_{Qmod} are set to 3.75 V and the appropriate frequency ranges are swept. S_{11} provides input VSWR data, S_{22} provides output VSWR data. S_{21} provides power output (add source power to S_{21} derived gain).

LO leakage data shown in figures 18, and 19 is generated by setting $V_{Imod} = V_{Qmod} = V_{Iref} = V_{Qref} = 2.5\,V$ then performing an S_{21} sweep. Since phase is not important for these measurements, a scalar network analyzer or a signal generator and spectrum analyzer could be used.

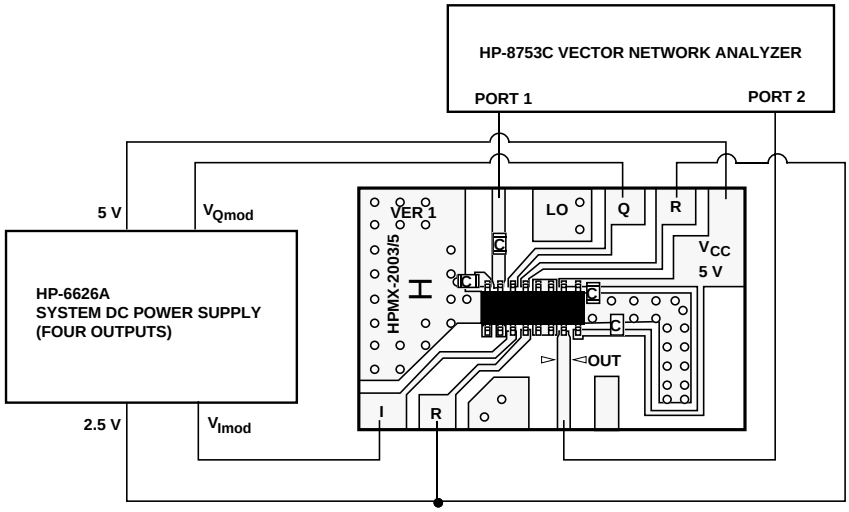


Figure 3. Test Setup for Measuring Amplitude and Phase Error, Input and Output VSWR, Power Output and LO Leakage of the Modulator.

HPMX-2003 Typical Performance

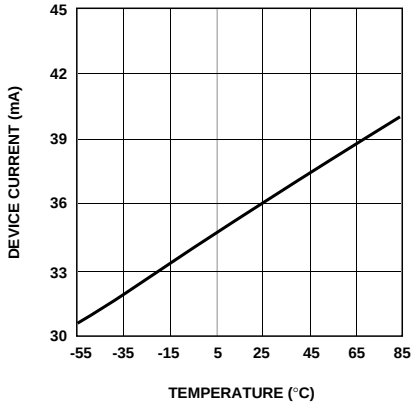


Figure 4. HPMX-2003 Device Current vs. Temperature, V_{CC} = 5 V.

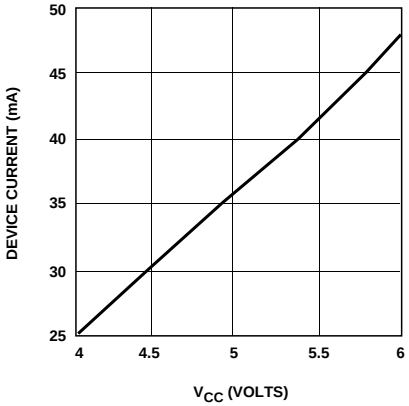


Figure 5. HPMX-2003 Device Current vs. V_{CC}, T_A = 25°C.

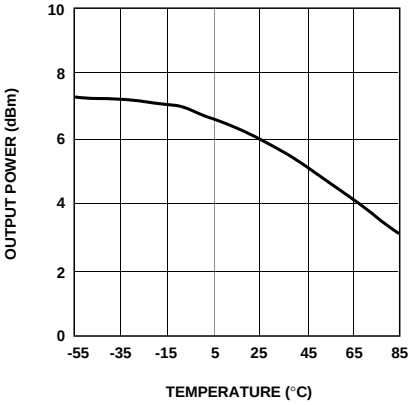


Figure 6. HPMX-2003 Power Output vs. Temperature at 900 MHz, LO = -12 dBm, $V_{Imod} = V_{Qmod} = 3.75$ V, $V_{Iref} = V_{Qref} = 2.5$ V, V_{CC} = 5 V.

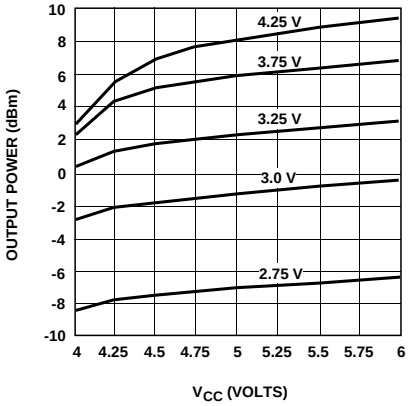


Figure 7. HPMX-2003 Power Output vs. V_{CC} and I, Q Level at 900 MHz, LO = -12 dBm, $V_{Imod} = V_{Qmod}$, T_A = 25°C.

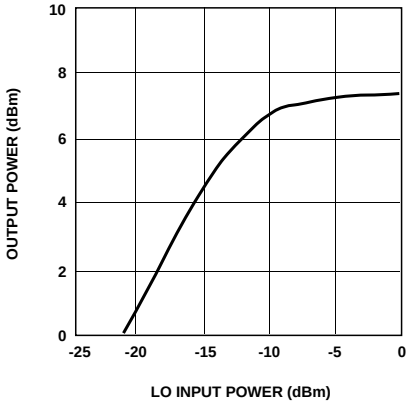


Figure 8. HPMX-2003 Power Output vs. LO Level at 900 MHz, V_{CC} = 5 V, $V_{Imod} = V_{Qmod} = 3.75$ V, T_A = 25°C.

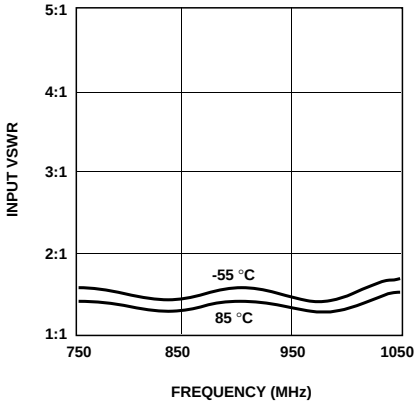


Figure 9. HPMX-2003 LO Input VSWR vs. Frequency and Temperature, V_{CC} = 5 V.

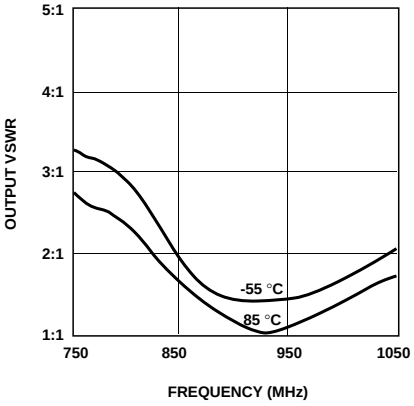


Figure 10. HPMX-2003 Output VSWR vs. Frequency and Temperature.

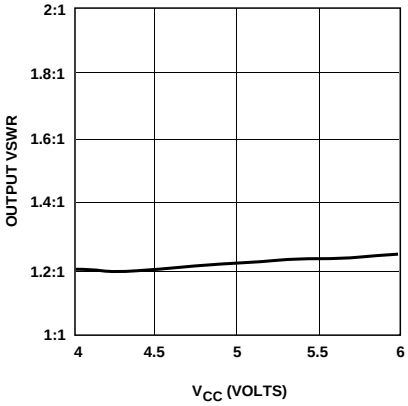


Figure 11. HPMX-2003 Output VSWR vs. V_{CC} at 900 MHz, T_A = 25°C.

HPMX-2003 Modulation Accuracy (Sample Part)

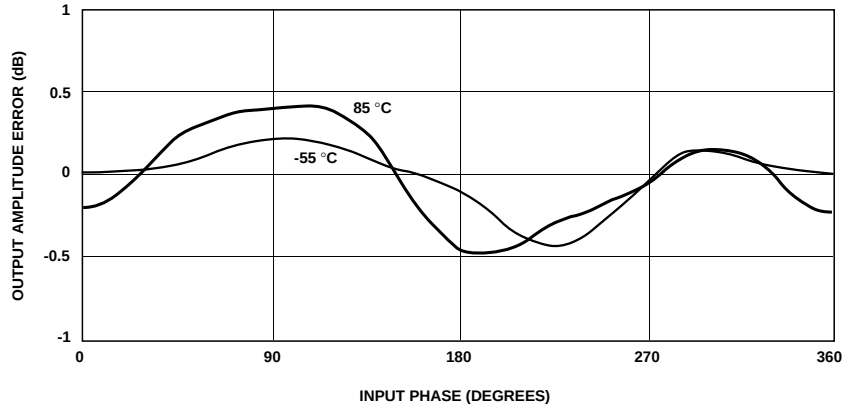


Figure 12. HPMX-2003 Amplitude Error vs. Input Phase at 900 MHz, V_{CC} = 5 V, $\sqrt{(V_{Imod}-2.5)^2 + (V_{Qmod}-2.5)^2}$ = 1.25 V, LO = -12 dBm. 25°C Curve Deleted for Clarit y.

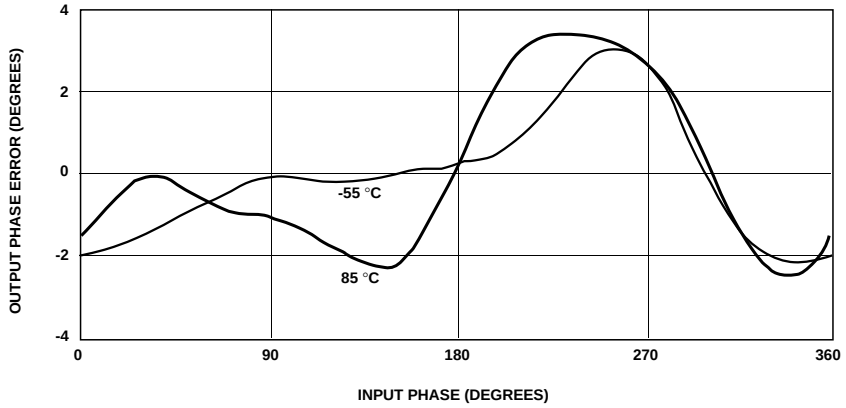


Figure 13. HPMX-2003 Output Phase Error vs. Input Phase at 900 MHz, V_{CC} = 5 V, $\sqrt{(V_{Imod}-2.5)^2 + (V_{Qmod}-2.5)^2}$ = 1.25 V, LO = -12 dBm. 25°C Curve Deleted for Clarity.

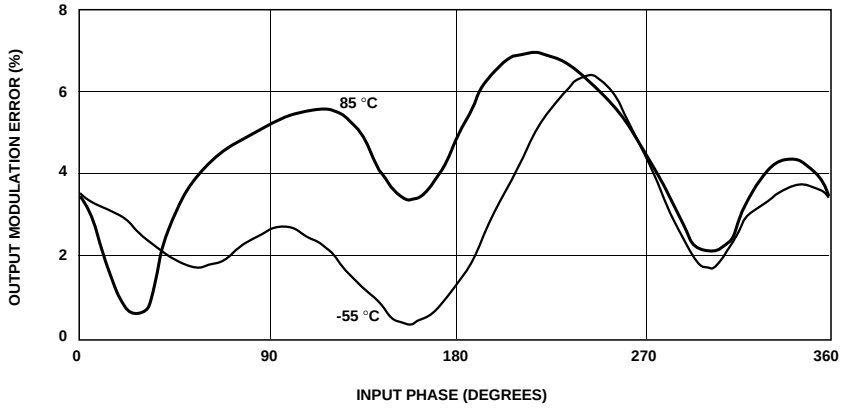


Figure 14. Modulation Error vs. Input Phase at 900 MHz, V_{CC} = 5 V, $\sqrt{(V_{Imod}-2.5)^2 + (V_{Qmod}-2.5)^2}$ = 1.25 V, LO = -12 dBm. Percent Modulation Error is Calculated from the Values of Amplitude and Phase Error.

HPMX-2003 Single and Double Sideband Performance

Single sideband (SSB) and double sideband (DSB) tests are sometimes used to evaluate modulator performance. Figure 17, below, shows the test equipment setup that was used to create the SSB and DSB output spectrum graphs (figures 15 and 16).

The phase shift provided by the I and Q signal generators must be very close to 90 degrees and the amplitude of the two signals must be matched within a few millivolts or results will not accurately reflect the performance of the modulator IC.

The I, Q signal generator must put out low distortion signals or the output spectrum will show high harmonic levels that reflect the performance of the signal generator, not the modulator.

HPMX-2003 Typical Sideband Performance Data

SSB: $V_{Iref} = V_{Qref} = 2.5\,V, V_{Imod} = V_{Iref} + 1.25\sin(2\pi f t), V_{Qmod} = V_{Qref} + 1.25\cos(2\pi f t), f = 25\,kHz$
DSB: $V_{Iref} = V_{Qref} = 2.5\,V, V_{Imod} = V_{Iref} + 1.25\cos(2\pi f t), V_{Qmod} = V_{Qref} + 1.25\cos(2\pi f t), f = 25\,kHz$

Symbol	Parameters and Test Conditions	Units	SSB	DSB
P_{LSB}	Lower Sideband Power Output	dBm	+3	0
LO_{leak}	LO Suppression	dBc	34	31
P_{USB}	Upper Sideband Power Output	dBm	-32	0
IM_3	Third Order Intermodulation Products	dBm	NA	-34

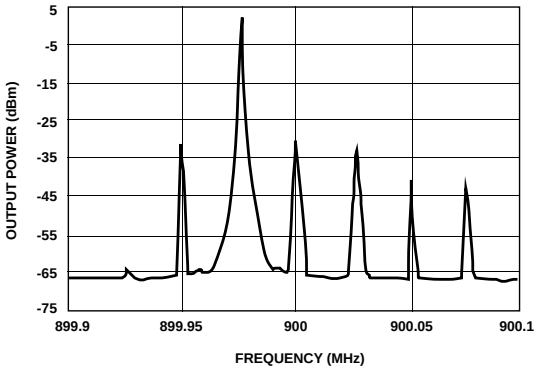


Figure 15. Single Sideband Output Spectrum. LO = -12 dBm at 900 MHz. The Test Setup is Shown in Figure 1 7.

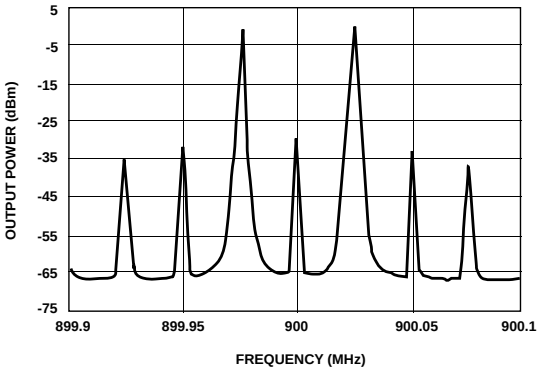


Figure 16. Double Sideband Output Spectrum. LO = -12 dBm at 900 MHz. The Test Setup is Shown in Figure 1 7.

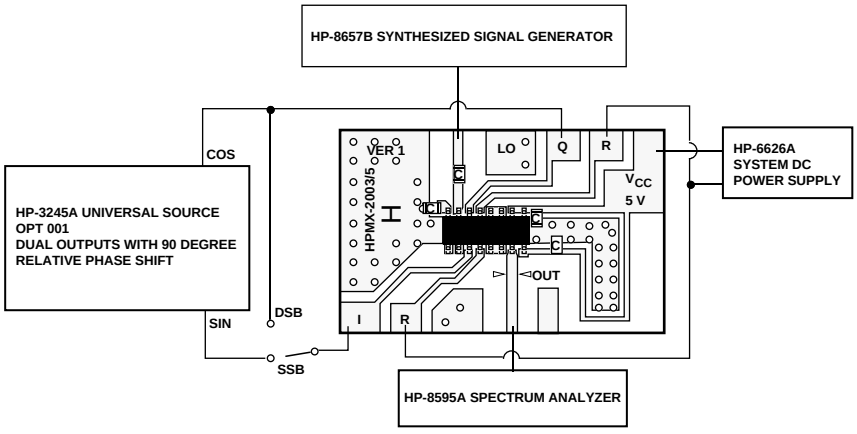


Figure 17. HPMX-2003 Single/Double Sideband Test Setup.

HPMX-2003 Using Offsets to Improve LO Leakage

It is possible to improve on the excellent performance of the HPMX-2003 for applications that are particularly sensitive to LO leakage. The nature of the improvement is best understood by examining figures 18 and 19, below.

LO leakage results when normal variations in the wafer fabrication process cause small shifts in the values of the modulator IC's internal components. These random variations create an effect equivalent to slight DC imbalances at the input of each (I and Q) mixer. The DC imbalances at the mixer inputs are multiplied by ± 1 at the LO frequency and show up at the output of the IC as LO leakage.

It is possible to externally apply small DC signals to the I and Q inputs and exactly cancel the internally generated DC offsets. This will result in sharply decreased LO leakage at precisely the frequency and temperature where the offsets were applied (see figure 18).

This improvement is not very useful if it doesn't hold up over frequency and temperature changes. The lower curve in figure 18 shows how the offset-adjusted LO leakage varies versus frequency. Note that it remains below -45 dBm over most of the frequency range shown. In the 20 MHz range centered at 900 MHz, the level is closer to -55 dBm.

Figure 19 shows the performance of the offset adjusted LO leakage over temperature. Note that the adjusted curve is at a level below -50 dBm over most of the temperature range.

The net result of using externally applied offsets with the HPMX-2003 is that an LO leakage level below -40 dBm can typically be achieved over both frequency and temperature.

The magnitude of the required external offset varies randomly from part to part and between the I and Q mixers on any given IC. Offsets can range from -56 mV to +56 mV. External offsets may be applied either by varying the average level of the I and Q modulating signals, or by varying the voltages at the I_{ref} and Q_{ref} pins of the modulator.

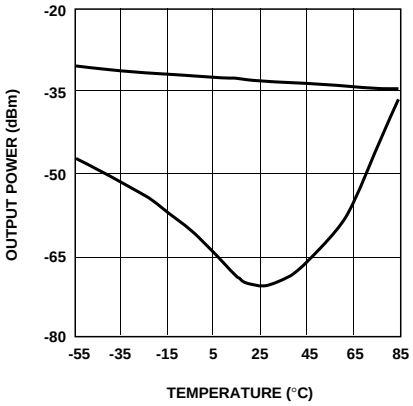


Figure 18. LO Leakage vs. Frequency Without DC Offsets (Upper Curve) and LO Leakage vs. Frequency With DC Offsets (Adjusted for Minimum LO Leakage at 900 MHz). T_A = 25°C, V_{CC} = 5 V, V_{Iref} = V_{Qref} = 2.5 V, LO = -12 dBm.

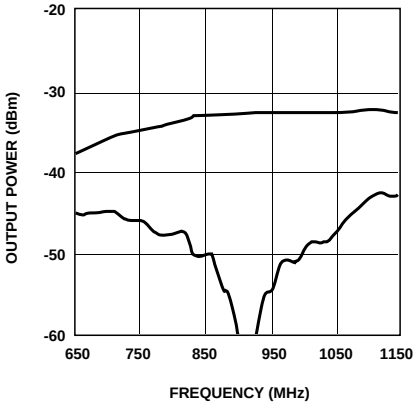


Figure 19. LO Leakage With No DC Offsets vs. Temperature (Upper Curve) and LO Leakage With DC Offsets (Adjusted for Minimum Leakage at 25°C) vs. Temperature (Lower Curve). Frequency = 900 MHz, V_{CC} = 5 V, V_{Iref} = V_{Qref} = 2.5 V, LO = -12 dBm.

HPMX-2003 Modulation Spectrum Diagrams

Figure 20, below, shows the test setup that was used to generate the modulation spectrum diagrams that appear on the GSM, JDC and NADC applications pages of this data sheet. The major differences between the tests are summarized in the table below.

The modulation spectra are created by setting the function generator to the appropriate bit-clock frequency. The pattern generator is set to produce a pseudorandom serial bit stream (n = 20) that is NRZ coded. The pseudorandom bit stream which simulates the serial data in a digital phone is fed to the base-band processor that splits it into a two bit parallel stream (I and Q) and then filters each according to the requirements of the digital telephone system being simulated. The I and Q signals from the baseband filter are then DC offset by 2.5 V using the op-amp circuit. The output of the modulator is monitored using a spectrum analyzer.

System	Bit Clock Frequency	Baseband Filter	Channel (LO) Frequency
GSM	270 kHz	0.3 GMSK (HP 8657B)	900 MHz
JDC	42 kHz	$\alpha = 0.5$ $\pi/4$ DQPSK (HP 8657D)	950 MHz
NADC	48.6 kHz	$\alpha = 0.35$ $\pi/4$ DQPSK (HP 8657D)	835 MHz

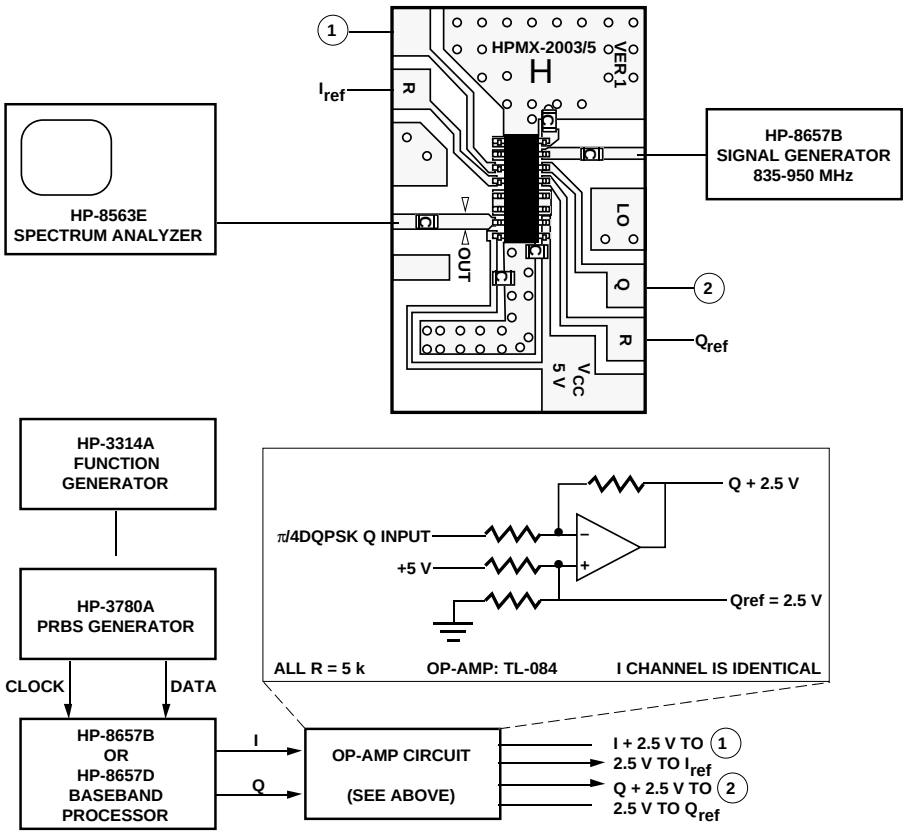


Figure 20. Test Equipment Setup for Modulation Spectrum Diagrams.

HPMX-2003 GSM Applications

The GSM System

GSM (Group Speciale Mobile) commonly refers to the European digital cellular telephone system standard. Digital cellular phones for the European market must conform to this standard. The GSM system is characterized by 200 kHz channel spacing and mobile to base transmit frequencies of 890 - 915 MHz. The primary modulation characteristics include 0.3 GMSK filtering of the I and Q signals and 270 kbps transmission rate.

Critical Performance Parameters

GSM standards require that the telephone exhibit RMS phase error ≤ 5° and peak phase error <20°. The modulated output spectrum of the phone must lie within a "spectral mask" which defines maximum allowable radiation levels into adjacent and alternate channels. Specifically, 200 kHz from the channel center frequency (f_0), the output of the phone must be at least 30 dB below the peak output at f_0. 400 kHz from f_0 the output must be 50-60 dB below the peak output at f_0 depending upon the class of radio. Refer to the GSM900 specifi-cations for more detailed information.

HPMX-2003 Performance

Typical RMS phase error level of 2° and typical peak levels of 8° makes the HPMX-2003 an excellent choice for GSM applications. The output spectrum falls easily within the GSM spectral mask, and the high power and simple output configuration mean lower components count, reduced size and higher system efficiency.

Particulars of Use

Many of the GSM application performance graphs shown in this data sheet were created using the test board shown in figure 21, below.

The only external components required by this IC are four chip capacitors. One capacitor is used as a DC block on the input transmission line. The second capacitor (at pin 8) provides an AC ground to one side of the differential LO input. The third and fourth capacitors (at pins 1 and 16) are for V_{CC} bypass.

The circuit board includes an inductive trace that can optionally be used to minimize output VSWR by placing a bypass capacitor at various points along the inductive line. Minimum VSWR for GSM applications is achieved by placing the capacitor as shown in the circle (inductance ≈2 nH).

The IC has an internal blocking capacitor so the output is a simple 50 Ω transmission line. An enlarged scale layout of the test board can be found on the last page of this data sheet.

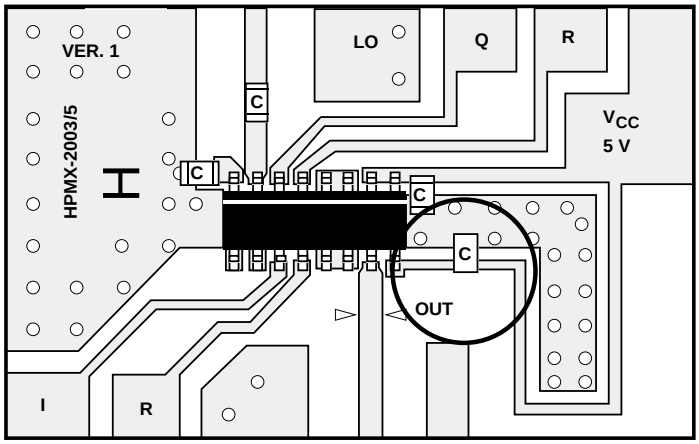


Figure 21. HPMX-2003 GSM Test Board.

HPMX-2003 Typical Performance Data

GSM Applications

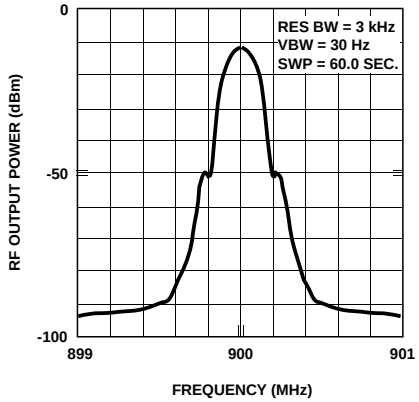


Figure 22. HPMX-2003 GSM Modulation Spectrum at -40°C.

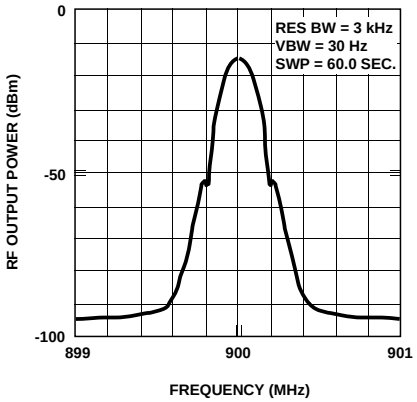


Figure 23. HPMX-2003 GSM Modulation Spectrum at 25°C.

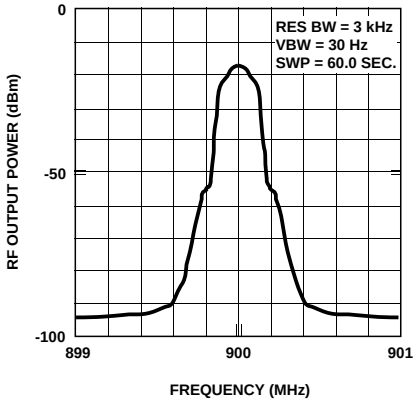


Figure 24. HPMX-2003 GSM Modulation Spectrum at 85°C.

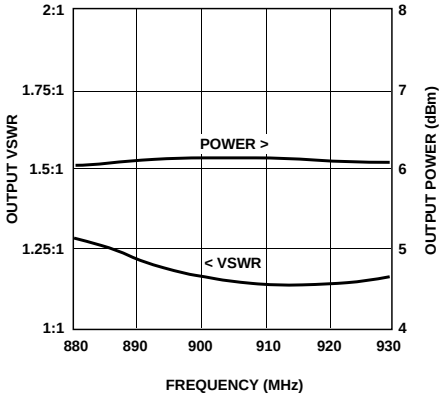


Figure 25. HPMX-2003 Output VSWR and Power vs. Frequency, V_{CC} = 5 V, LO = -12 dBm, V_{Imod} = V_{Qmod} = 3.75 V, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

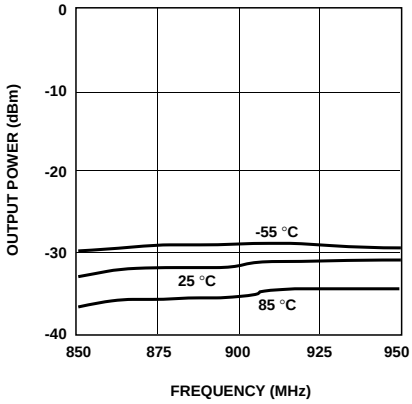


Figure 26. HPMX-2003 LO Leakage vs. Frequency and Temperature (Without Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, V_{Imod} = V_{Qmod} = V_{Iref} = V_{Qref} = 2.5 V.

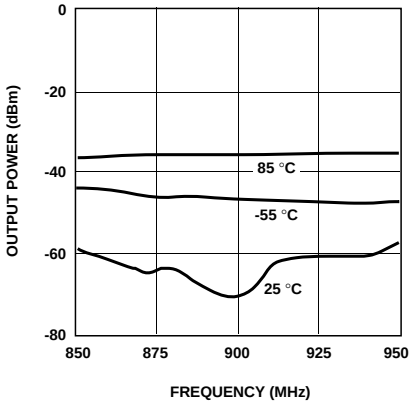


Figure 27. LO leakage vs. Frequency and Temperature (With 25°C Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V.

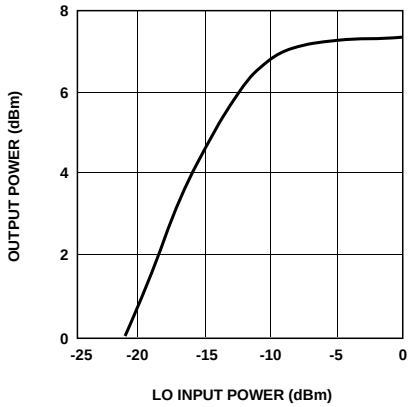


Figure 28. HPMX-2003 Power Output vs. LO Input Power at 900 MHz, V_{CC} = 5 V, V_{Imod} = V_{Qmod} = 3.75 V, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

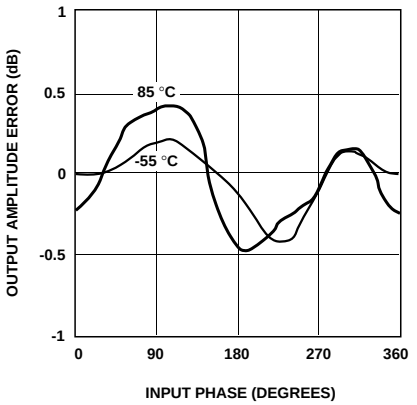


Figure 29. HPMX-2003 Vector Amplitude Error vs. Input Phase and Temperature at 900 MHz, V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V.

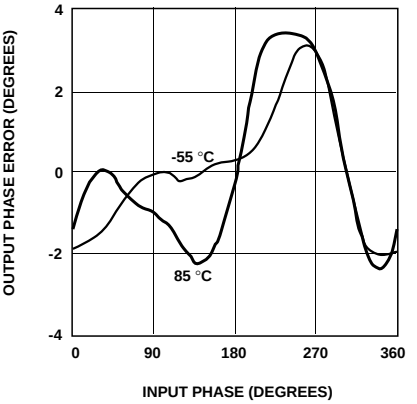


Figure 30. HPMX-2003 Vector Phase Error vs. Input Phase and Temperature at 900 MHz, V_{CC} = 5 V, LO = -12 dBm, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V.

Note: Modulation spectrum test conditions as follows: V_{CC} = 5 V, LO = -12 dBm at 900 MHz, V_{Imod} = V_{Qmod} = 2.5 V_{p-p}, unbalanced, average level = 2.5 V, V_{Iref} = V_{Qref} = 2.5 V, bit clock rate: 270 kHz, baseband filter: α = 0.3 GMSK.

HPMX-2003 NADC Applications

The NADC System

NADC (North American Digital Cellular) commonly refers to the digital sections of the IS-55 cellular telephone system standard. Dual mode (FM/TDMA) cellular phones for the North American market must conform to this standard. The NADC system is characterized by 30 kHz channel spacing and mobile to base transmit frequencies of 824 - 849 MHz. The primary modulation characteristics include π/4 DQPSK filtering of the I and Q signals and 48.6 kbps transmission rate.

Critical Performance Parameters

System specifications require that the telephone exhibit RMS modulation error under 12% in the digital mode. The modulated output spectrum of the phone must lie within a "spectral mask" which defines maximum allowable radiation levels into adjacent and alternate channels. Specifically, total power radiated into the either adjacent channel must be at least 26 dB below the mean output power. Total power radiated into either alternate channel must be at least 45 dB below the mean output power. Refer to the IS-55 specifications for more detailed information.

HPMX-2003 Performance

The typical RMS modulation error level of 4% makes the HPMX-2003 an excellent choice for NADC applications. The output falls easily within the NADC spectral requirements, and the high power and simple output configuration mean lower components count, reduced size and higher system efficiency.

Particulars of Use

Many of the NADC application performance graphs shown in this data sheet were created using the test board shown in figure 31, below.

The only external components required by this IC are four chip capacitors. One capacitor is used as a DC block on the input transmission line. The second capacitor (at pin 8) provides an AC ground to one side of the differential LO input. The third and fourth capacitors (at pins 1 and 16) are for V_{CC} bypass.

The circuit board includes an inductive trace that can optionally be used to minimize output VSWR by placing a bypass capacitor at various points along the inductive line. Minimum VSWR for NADC applications is achieved by placing the capacitor as shown in the circle (inductance ≈ 6 nH).

The IC has an internal blocking capacitor so the output is a simple 50 Ω transmission line. An enlarged scale layout of the test board can be found on the last page of this data sheet.

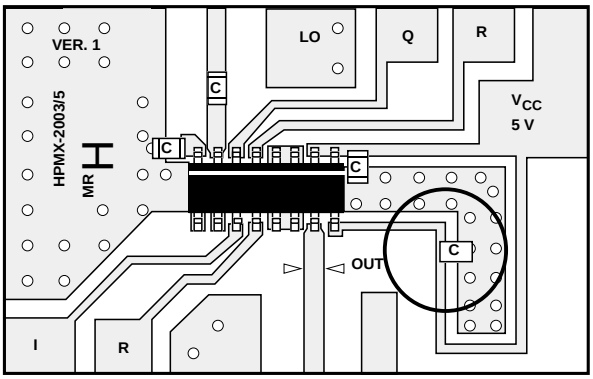


Figure 31. HPMX-2003 NADC Test Board.

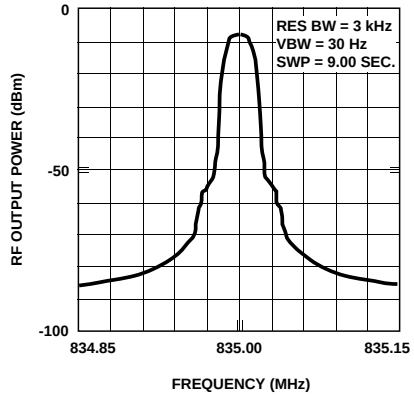


Figure 32. HPMX-2003 NADC Modulation Spectrum at -40°C.

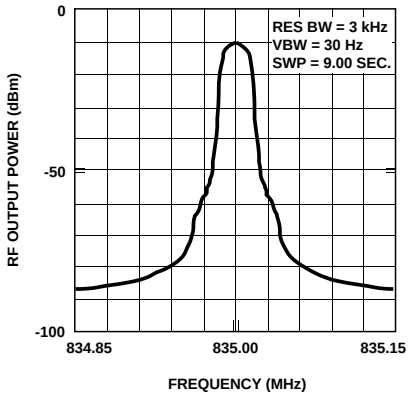


Figure 33. HPMX-2003 NADC Modulation Spectrum at 25°C.

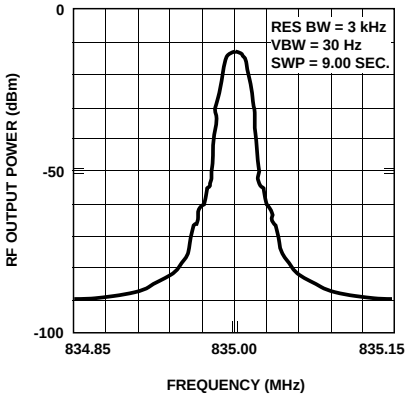


Figure 34. HPMX-2003 NADC Modulation Spectrum at 85°C.

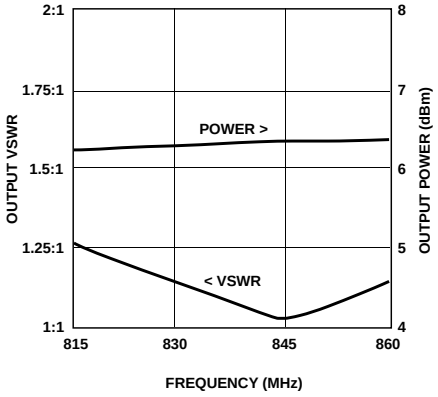


Figure 35. HPMX-2003 Output VSWR and Power vs. Frequency, V_{CC} = 5 V, LO = -12 dBm, $V_{Imod} = V_{Qmod}$ = 3.75 V, Unbalanced, $V_{Iref} = V_{Qref}$ = 2.5 V, T_A = 25°C.

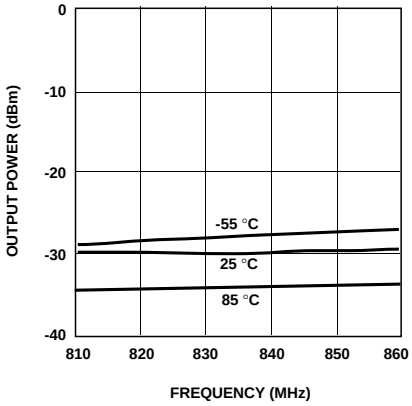


Figure 36. HPMX-2003 LO Leakage vs. Frequency and Temperature (Without Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, $V_{Imod} = V_{Qmod} = V_{Iref} = V_{Qref}$ = 2.5 V.

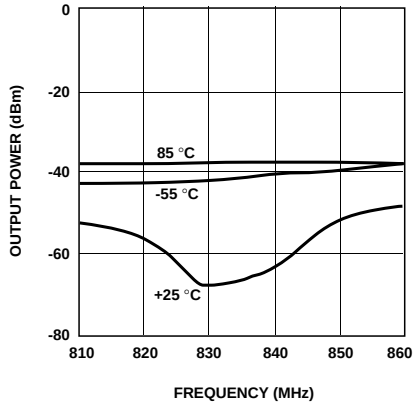


Figure 37. LO Leakage vs. Frequency and Temperature (With 25°C Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V.

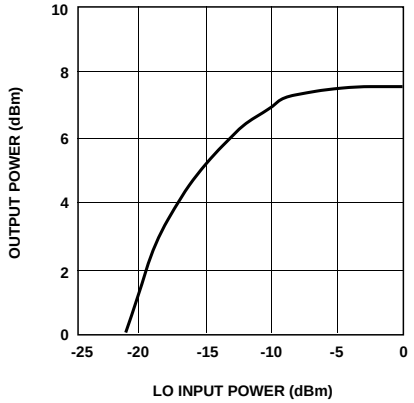


Figure 38. HPMX-2003 Power Output vs. LO Input Power at 900 MHz, V_{CC} = 5 V, LO = -12 dBm, $V_{Imod} = V_{Qmod}$ = 3.75 V, Unbalanced, $V_{Iref} = V_{Qref}$ = 2.5 V, T_A = 25°C.

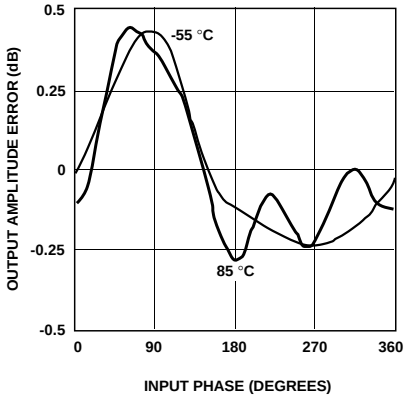


Figure 39. HPMX-2003 Vector Amplitude Error vs. Input Phase and Temperature at 900 MHz, V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V.

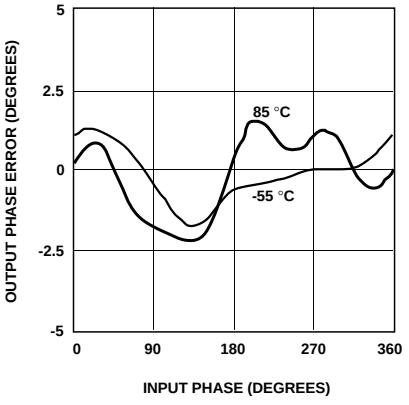


Figure 40. HPMX-2003 Vector Phase Error vs. Input Phase and Temperature at 900 MHz, V_{CC} = 5 V, LO = -12 dBm, Unbalanced, $V_{Iref} = V_{Qref}$ = 2.5 V.

Note: Modulation spectrum test conditions as follows: LO = -12 dBm at 835 MHz, $V_I = V_Q$ = 2.5 V_{p-p}, unbalanced, average level = 2.5 V, $V_{Iref} = V_{Qref}$ = 2.5 V, bit clock rate: 48.6 kHz, baseband filter: $\alpha = 0.35$, $\pi/4$ DQPSK, V_{CC} = 5 V.

HPMX-2003 JDC Applications

The JDC System

JDC (Japan Digital Cellular) commonly refers to the Japanese digital cellular telephone system standard. Digital cellular phones for the Japanese market must conform to this standard. The JDC system is characterized by 25 kHz channel spacing and mobile to base transmit frequencies of 940 – 960 MHz. The primary modulation characteristics include π/4 DQPSK filtering of the I and Q signals and 42 kbps transmission rate.

Critical Performance Parameters

JDC standards require that the telephone exhibit RMS modulation error ≤ 12.5%. The modulated output spectrum of the phone must lie within a "spectral mask" which defines maximum allowable radiation levels into adjacent and alternate channels. Specifically, 50 kHz from the channel center frequency (f_0), the output of the phone must be at least 45 dB below the peak output at f_0. 100 kHz from f_0, the output must be at least 60 dB below the peak output at f_0. Refer to the JDC specifications for more detailed information.

HPMX-2003 Performance

The typical RMS modulation error level of 4% makes the HPMX-2003 an excellent choice for JDC applications. The output spectrum falls easily within the JDC spectral mask, and the high power and simple output configuration mean lower components count, reduced size and higher system efficiency.

Particulars of Use

Many of the JDC application performance graphs shown in this data sheet were created using the test board shown in figure 41,below.

The only external components required by this IC are four chip capacitors. One capacitor is used as a DC block on the input transmission line. The second capacitor (at pin 8) provides an AC ground to one side of the differential LO input. The third and fourth capacitors (at pins 1 and 16) are for V_{CC} bypass.

The circuit board includes an inductive trace that can optionally be used to minimize output VSWR by placing a bypass capacitor at various points along the inductive line. Minimum VSWR for JDC applications is achieved by placing the capacitor as shown in the circle (inductance ≈ 0 nH).

The IC has an internal blocking capacitor so the output is a simple 50 Ω transmission line. An enlarged scale layout of this board can be found on the last page of this data sheet.

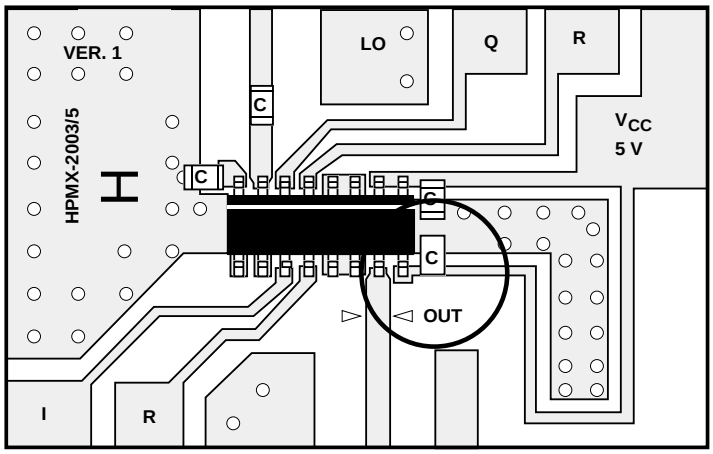


Figure 41. HPMX-2003 JDC Test Board.

HPMX-2003 Typical Performance Data

JDC Applications

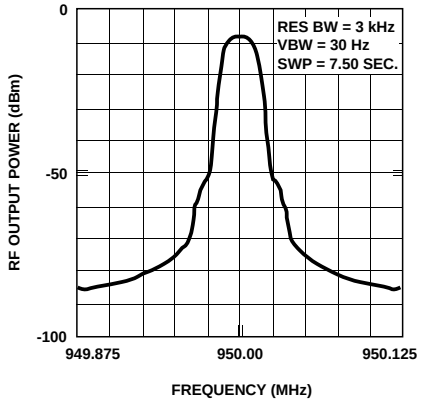


Figure 42. HPMX-2003 JDC Modulation Spectrum at -40°C.

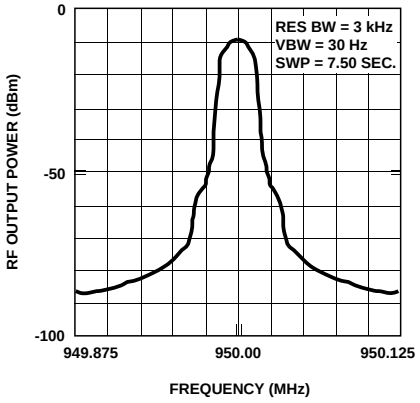


Figure 43. HPMX-2003 JDC Modulation Spectrum at 25°C.

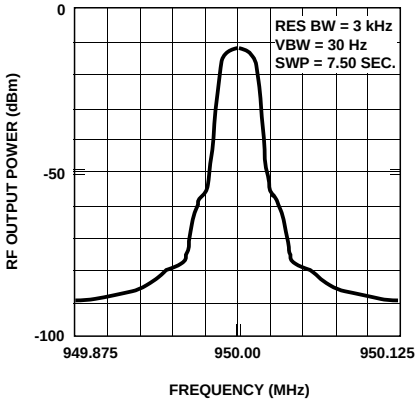


Figure 44. HPMX-2003 JDC Modulation Spectrum at 85°C.

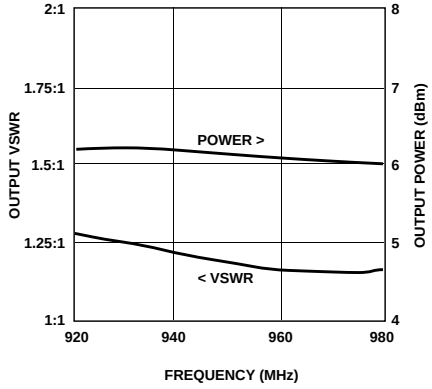


Figure 45. HPMX-2003 Output VSWR and Power vs. Frequency, V_{CC} = 5 V, LO = -12 dBm, $V_{Imod} = V_{Qmod}$ = 3.75 V, Unbalanced, $V_{Iref} = V_{Qref}$ = 2.5 V, T_A = 25 °C.

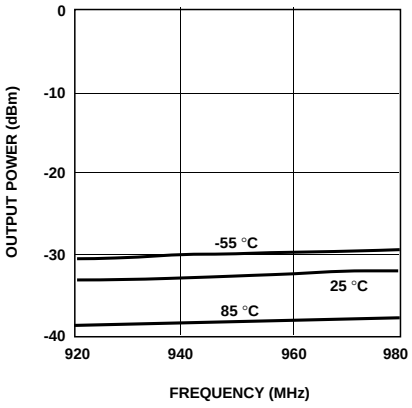


Figure 46. HPMX-2003 LO Leakage vs. Frequency and Temperature (Without Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, $V_{Imod} = V_{Qmod} = V_{Iref} = V_{Qref}$ = 2.5 V.

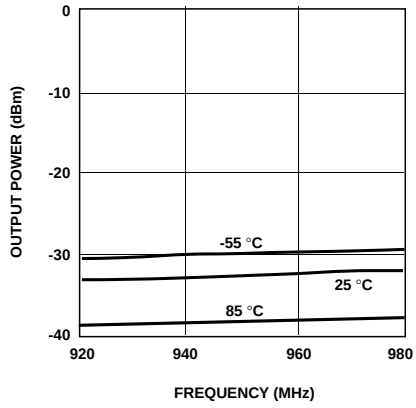


Figure 47. LO Leakage vs. Frequency and Temperature (With 25°C Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V.

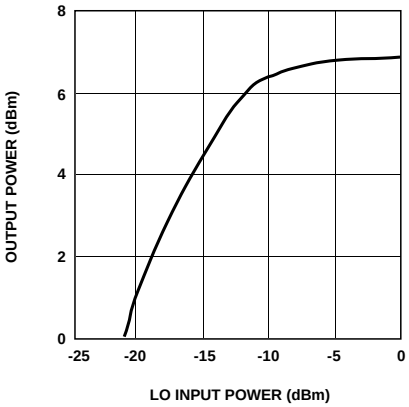


Figure 48. HPMX-2003 Power Output vs. LO Input Power at 950 MHz, V_{CC} = 5 V, $V_{Imod} = V_{Qmod}$ = 3.75 V, Unbalanced, $V_{Iref} = V_{Qref}$ = 2.5 V, T_A = 25°C.

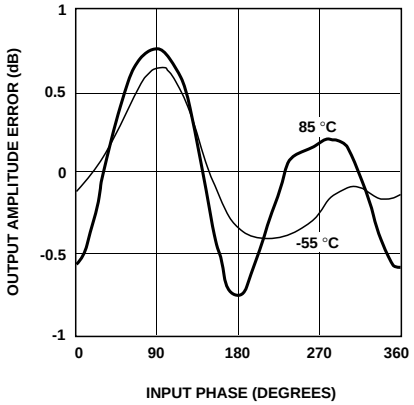


Figure 49. HPMX-2003 Vector Amplitude Error vs. Input Phase and Temperature at 950 MHz, V_{CC} = 5 V, LO = -12 dBm, Unbalanced, $V_{Iref} = V_{Qref}$ = 2.5 V.

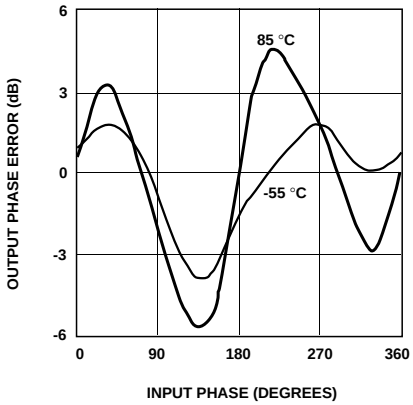


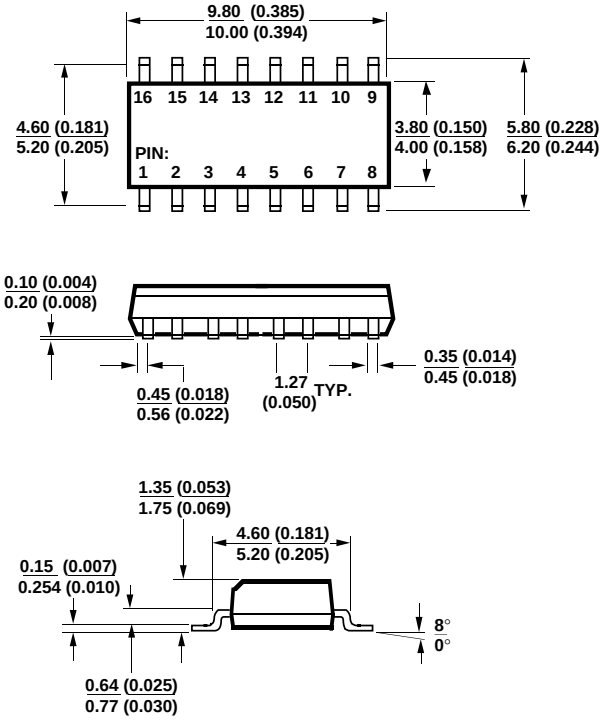
Figure 50. HPMX-2003 Vector Phase Error vs. Input Phase and Temperature at 950 MHz, V_{CC} = 5 V, LO = -12 dBm, Unbalanced, $V_{Iref} = V_{Qref}$ = 2.5 V.

Note: Modulation spectrum test conditions as follows: LO = -12 dBm at 950 MHz, $V_{Imod} = V_{Qmod}$ = 2.5 V_{p-p}, unbalanced, average level = 2.5 V, $V_{Iref} = V_{Qref}$ = 2.5 V, bit clock rate: 42 kHz, baseband filter: $\alpha = 0.5$, $\pi/4$ DQPSK, V_{CC} = 5 V.

HPMX-2003
Part Number Ordering Information

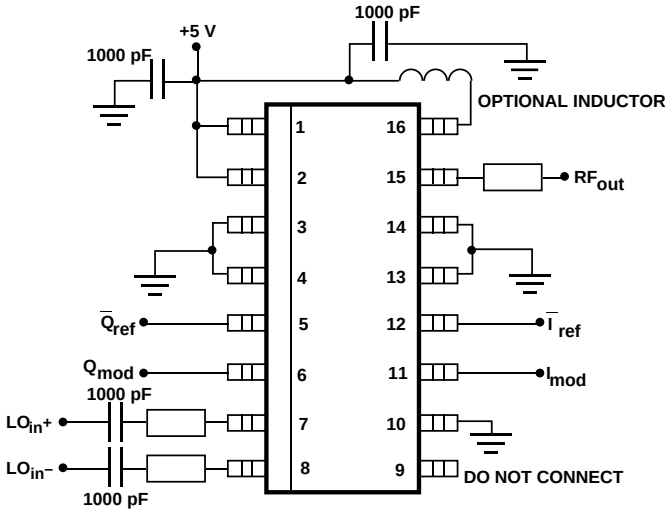
Part Number	Option	No. of Devices	Reel Size
HPMX-2003		25 min.	tube
HPMX-2003	T10	1000	7"

Package Dimensions
SO-16 Package



NOTE: DIMENSIONS ARE IN MILLIMETERS (INCHES).

HPMX-2003 Test Board Layout



Finished board size: 1.5" x 1" x 1/32" Material: 1/32" epoxy/fiberglass, 1 oz. copper, both sides, tin/lead coating, both sides.

Note: white "+" marks indicate drilling locations for plated-through via holes to the groundplane on the bottom side of the board.