

3.6A, 200V, 1.500 Ohm, P-Channel Power MOSFETs

These are advanced power MOSFETs designed, tested, and guaranteed to withstand a specific level of energy in the avalanche breakdown mode of operation. These are P-Channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17502.

Ordering Information

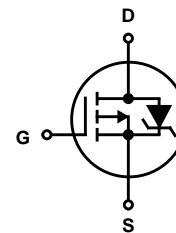
PART NUMBER	PACKAGE	BRAND
IRFR9220	TO-252AA	IF9220
IRFU9220	TO-251AA	IF9220

NOTE: When ordering use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, e.g., IRFR92209A.

Features

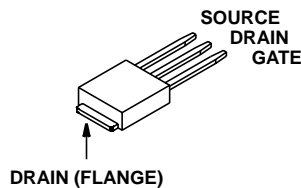
- 3.6A, 200V
- $r_{DS(ON)} = 1.500\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

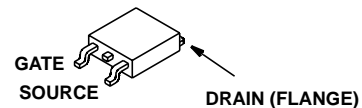


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



IRFR9220, IRFU9220

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	IRFR9220, IRFU9220	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	-200 V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	-200 V
Gate to Source Voltage	V_{GS}	± 20 V
Continuous Drain Current	I_D	3.6 A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve
Power Dissipation	P_D	42 W
Linear Derating Factor		0.33 $\text{W}/^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	-200	-	-	V	
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	-2.0	-	-4.0	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	-25	μA	
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	-250	μA	
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA	
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 2.2\text{A}, V_{GS} = -10\text{V}$ (Figure 9)	-	-	1.500	Ω	
Turn-On Time	t_{ON}	$V_{DD} = -100\text{V}, I_D = 3.9\text{A},$ $R_L = 24\Omega, V_{GS} = -10\text{V},$ $R_{GS} = 18\Omega$ (Figures 13, 16, 17)	-	-	50	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	8.8	-	ns	
Rise Time	t_r		-	27	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	7.3	-	ns	
Fall Time	t_f		-	19	-	ns	
Turn-Off Time	t_{OFF}	-	-	-	50	ns	
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0$ to -10V	$V_{DD} = -160\text{V},$ $I_D = 3.9\text{A},$ $R_L = 41\Omega$ $I_{G(REF)} = 1.45\text{mA}$	-	20	-	nC
Gate to Drain Charge	Q_{gd}			-	11	-	nC
Gate to Source Charge	Q_{gs}			-	3.3	-	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ (Figure 12)	-	550	-	pF	
Output Capacitance	C_{OSS}		-	110	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	33	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	3.00	$^\circ\text{C}/\text{W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	100	$^\circ\text{C}/\text{W}$	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = -3.6\text{A}$	-	-	-6.3	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = -3.6\text{A}, dI_{SD}/dt = -100\text{A}/\mu\text{s}$	-	150	300	ns
Reverse Recovery Charge	Q_{RR}			0.97	2.0	μC

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

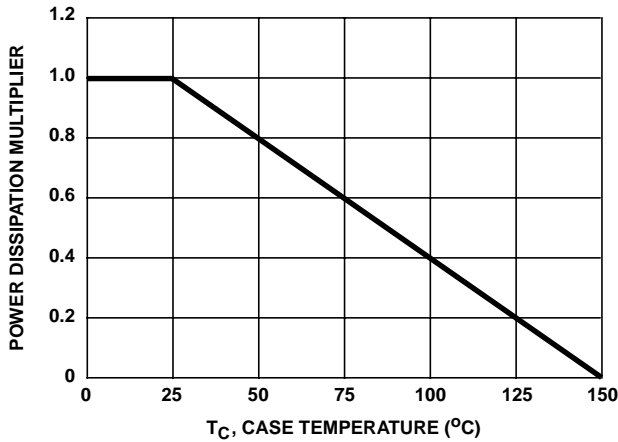


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

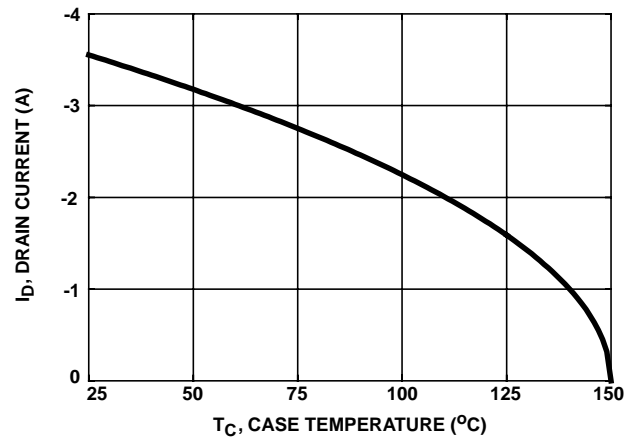


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

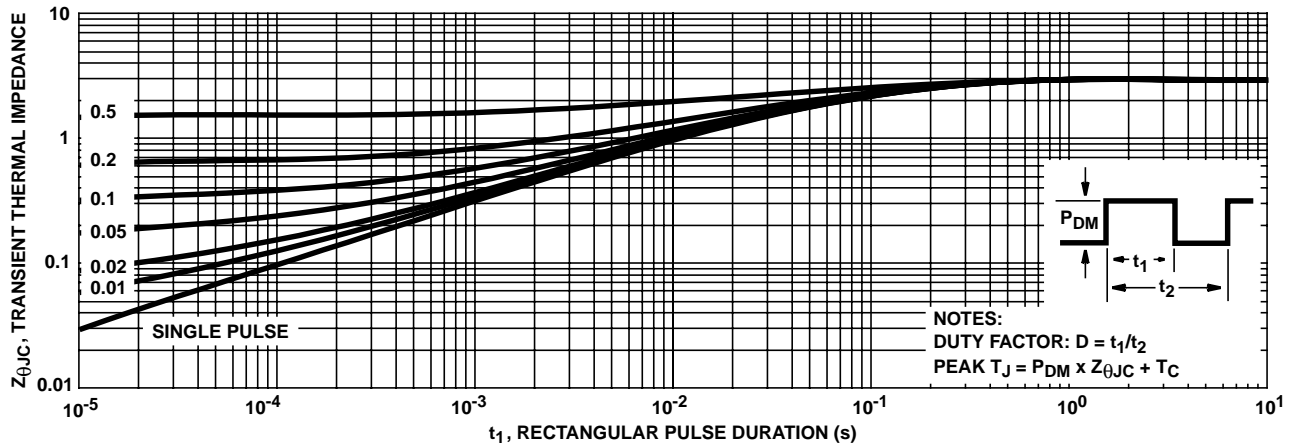


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

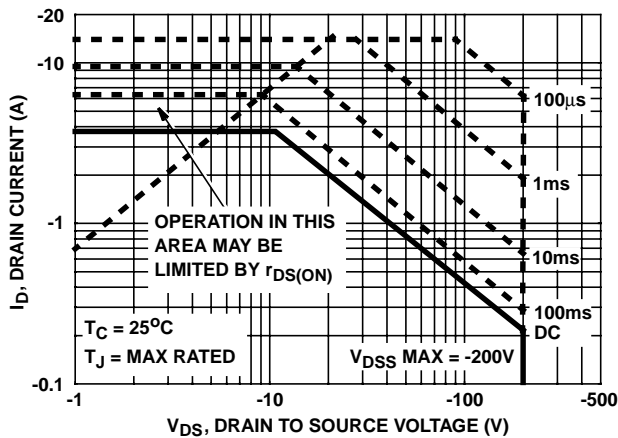


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

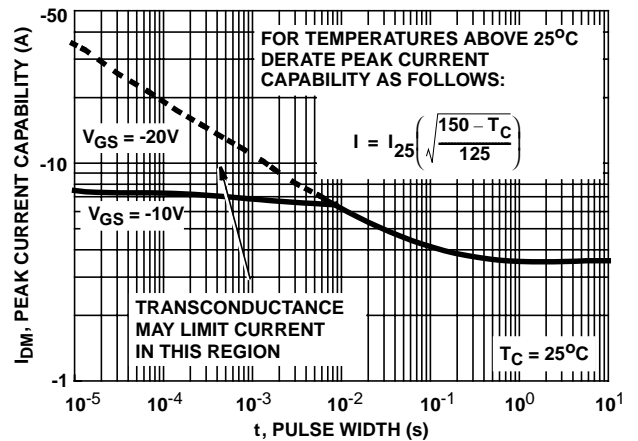


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)

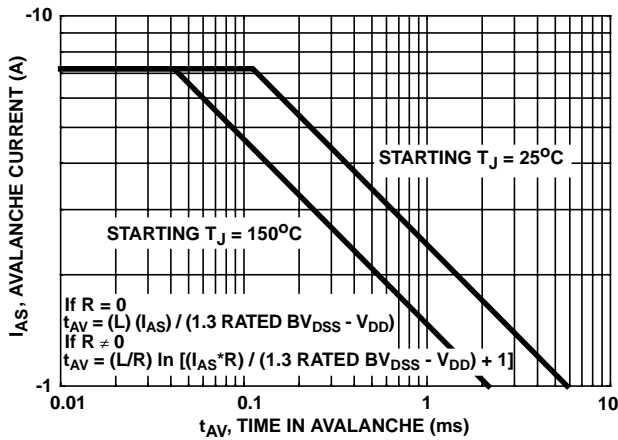


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

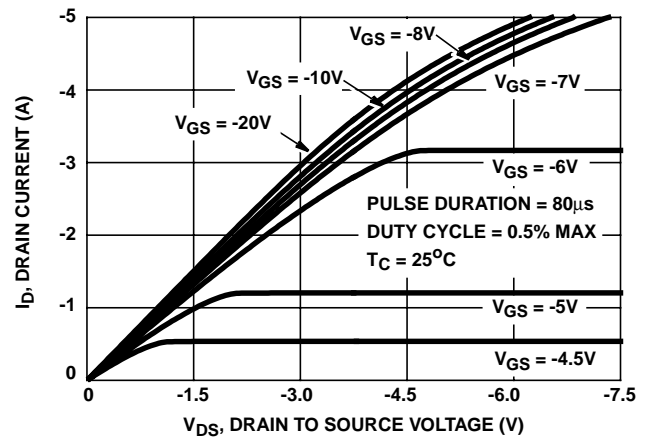


FIGURE 7. SATURATION CHARACTERISTICS

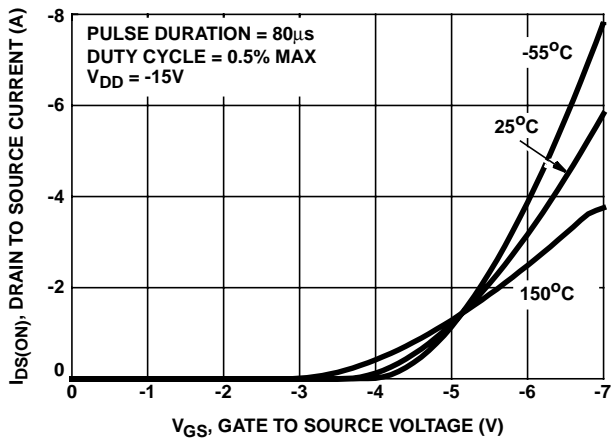


FIGURE 8. TRANSFER CHARACTERISTICS

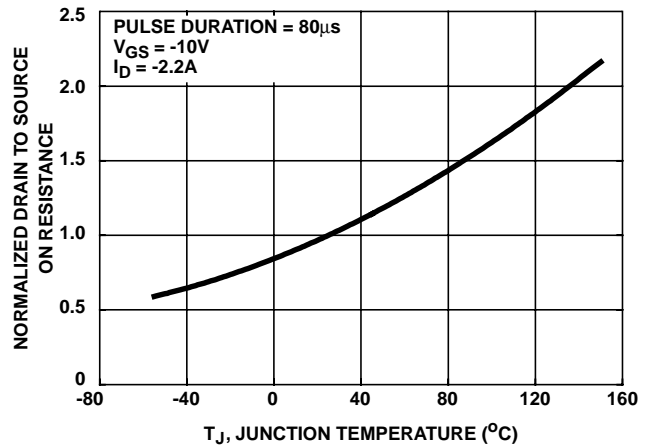


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

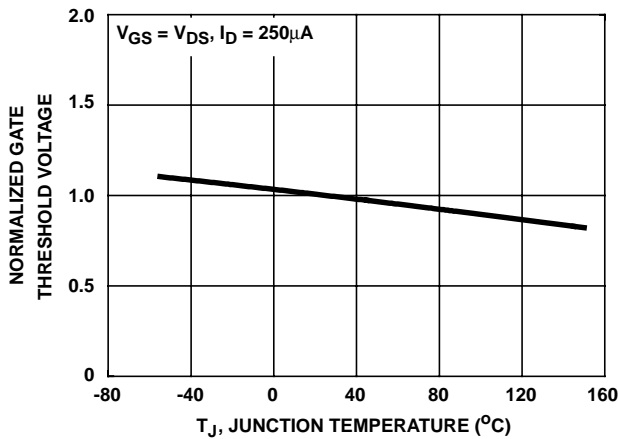


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

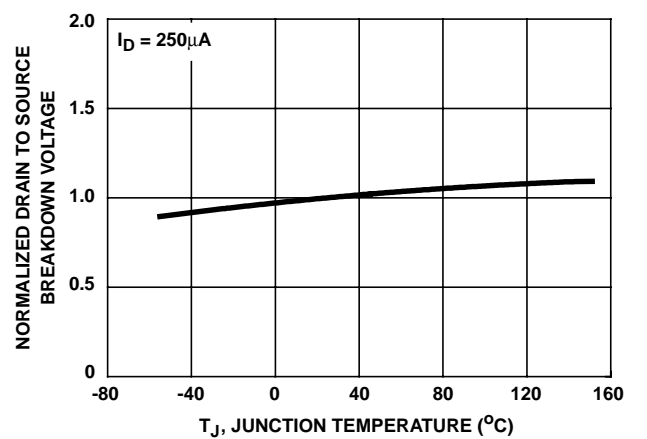


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

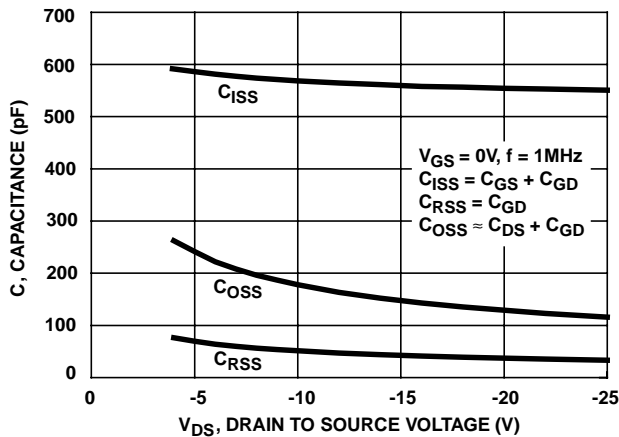
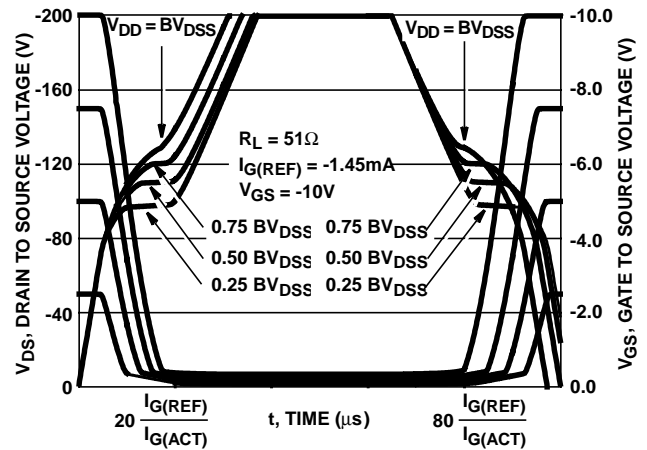


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

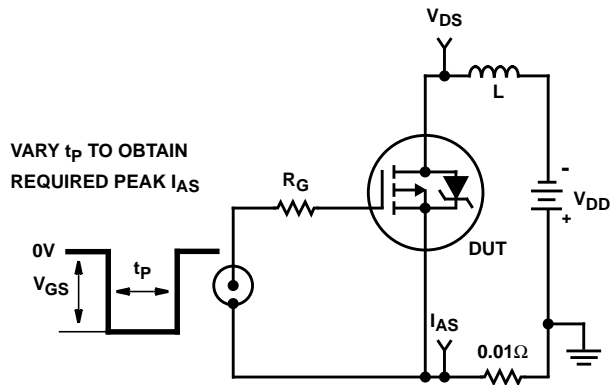


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

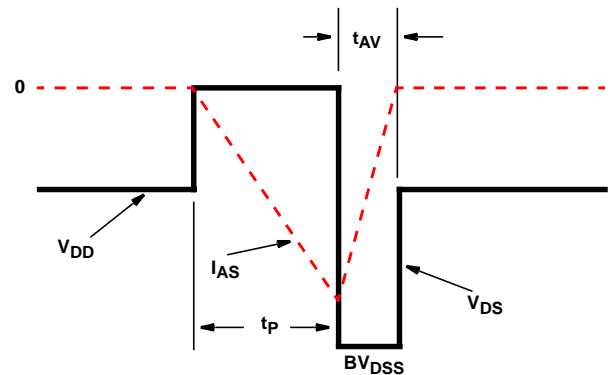


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

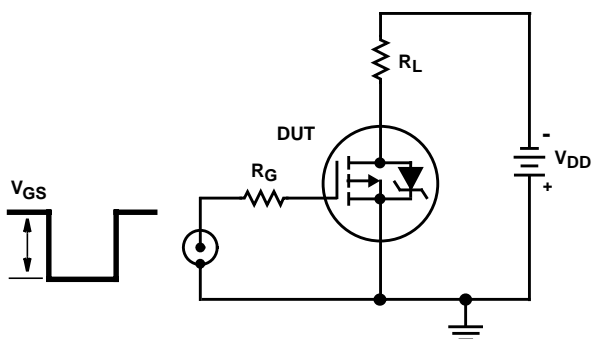


FIGURE 16. SWITCHING TIME TEST CIRCUIT

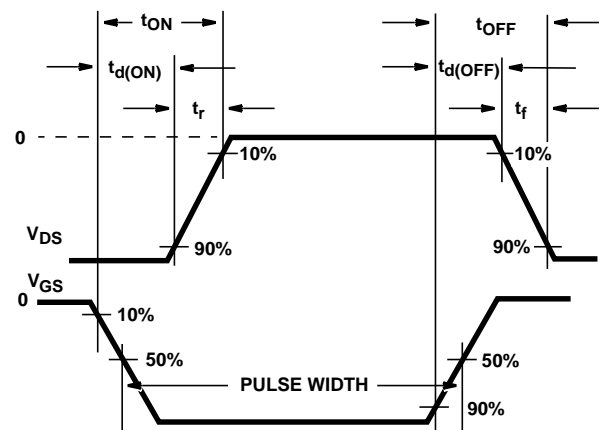


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

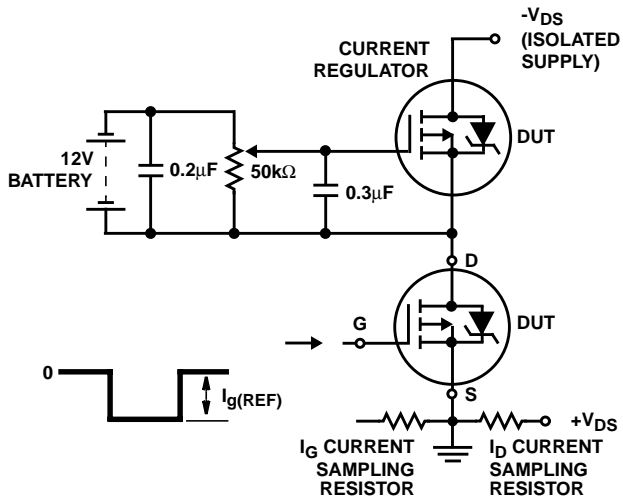


FIGURE 18. GATE CHARGE TEST CIRCUIT

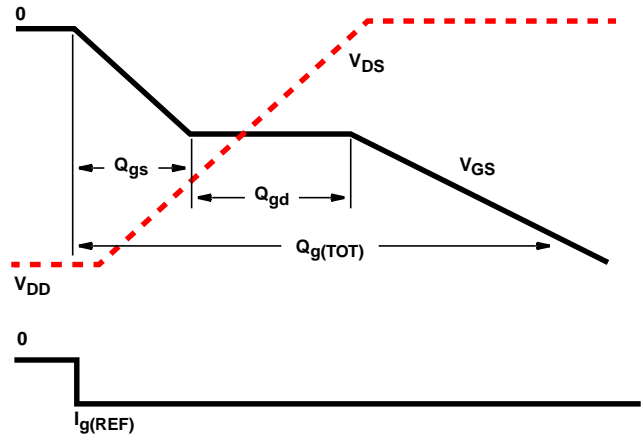


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

.SUBCKT IRFU9220 2 1 3 REV 9/6/94

CA 12 8 723e-12
 CB 15 14 733e-12
 CIN 6 8 517e-12

DBODY 5 7 DBDMOD
 DBREAK 5 11 DBKMOD
 DPLCAP 10 6 DPLCAPMOD

EBREAK 7 11 17 18 -244.4
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 5 10 8 6 1
 EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
 LGATE 1 9 2.609e-9
 LSOURCE 3 7 2.609e-9

MOS1 16 6 8 8 MOSMOD M=0.99
 MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
 RDRAIN 50 16 RDSMOD 1.194
 RGATE 9 20 2.17
 RIN 6 8 1e9
 RLDRAIN 2 5 10
 RLGATE 1 9 26.09
 RLSOURCE 3 7 26.09
 RSCL1 5 51 RSCLMOD 1e-6
 RSCL2 5 50 1e3
 RSOURCE 8 7 RDSMOD 90.1e-3
 RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

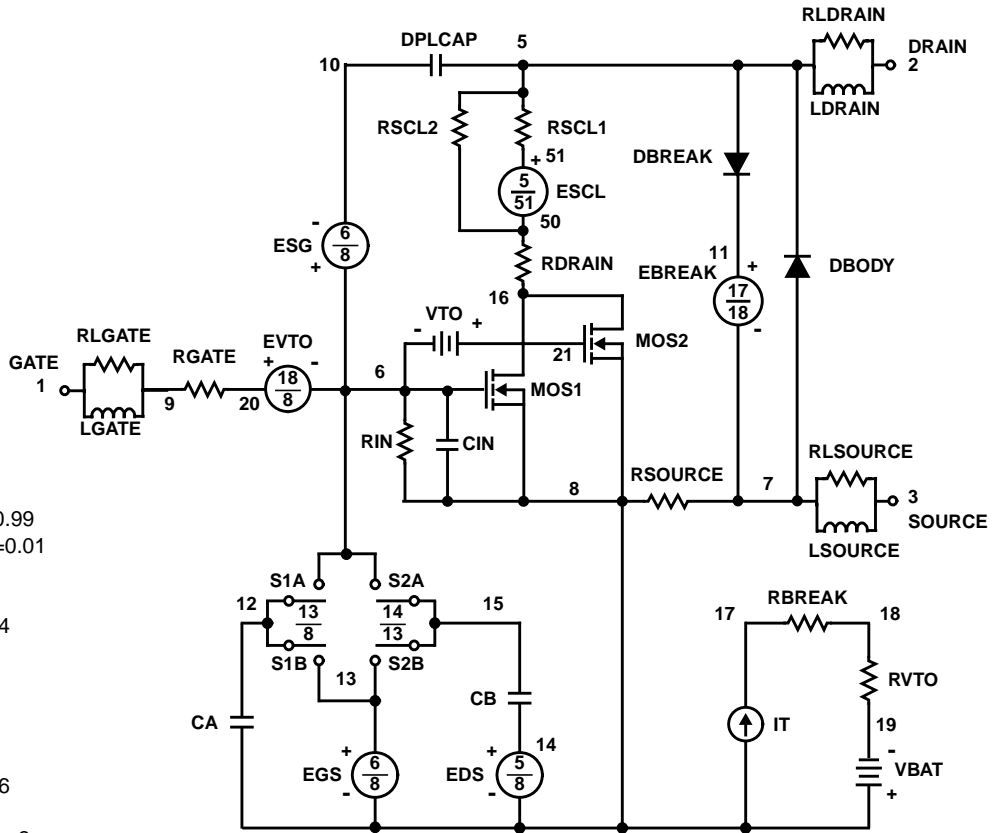
VBAT 8 19 DC 1
 VTO 21 6 -0.77

ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51))*1e6/4.6,6)}

.MODEL DBDMOD D (IS=2.56e-14 RS=8.09e-2 TRS1=-2.45e-3 TRS2=-1.33e-5 CJO=4.21e-10 TT=1.17e-7)
 .MODEL DBKMOD D (RS=5.07 TRS1=-1.05e-3 TRS2=1.28e-5)
 .MODEL DPLCAPMOD D (CJO=170e-12 IS=1e-30 N=10)
 .MODEL MOSMOD PMOS (VTO=-3.58 KP=1.38 IS=1e-30 N=10 TOX=1 L=1u W=1u)
 .MODEL RBKMOD RES (TC1=1.1e-3 TC2=-2.73e-6)
 .MODEL RDSMOD RES (TC1=6.95e-3 TC2=2.23e-5)
 .MODEL RSCLMOD RES (TC1=2.40e-3 TC2=-1.5e-5)
 .MODEL RVTOMOD RES (TC1=-3.27e-3 TC2=-1.33e-6)
 .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=5.29 VOFF=3.29)
 .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.29 VOFF=5.29)
 .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.1 VOFF=-4.9)
 .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.9 VOFF=0.1)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.



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