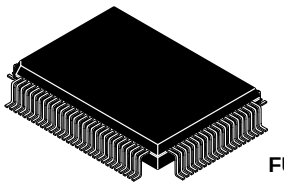
MC143421

Advance Information

PCI Bus Interface

The MC143421 PCI Bus Interface chip is a low cost and highly integrated PCI interface solution that includes Advanced Configuration Power Interface (ACPI) features. It is designed to enable the addition of a PCI interface to PC peripherals such as DSP–based analog modems.

The Peripheral Interface Bus (PIB) that interfaces this device to the PC peripheral function provides four address lines, byte–wide data, and eight programmable lines that can be used for chip selects, interrupts, and power–down enable.



FU SUFFIX
QFP
CASE 842D

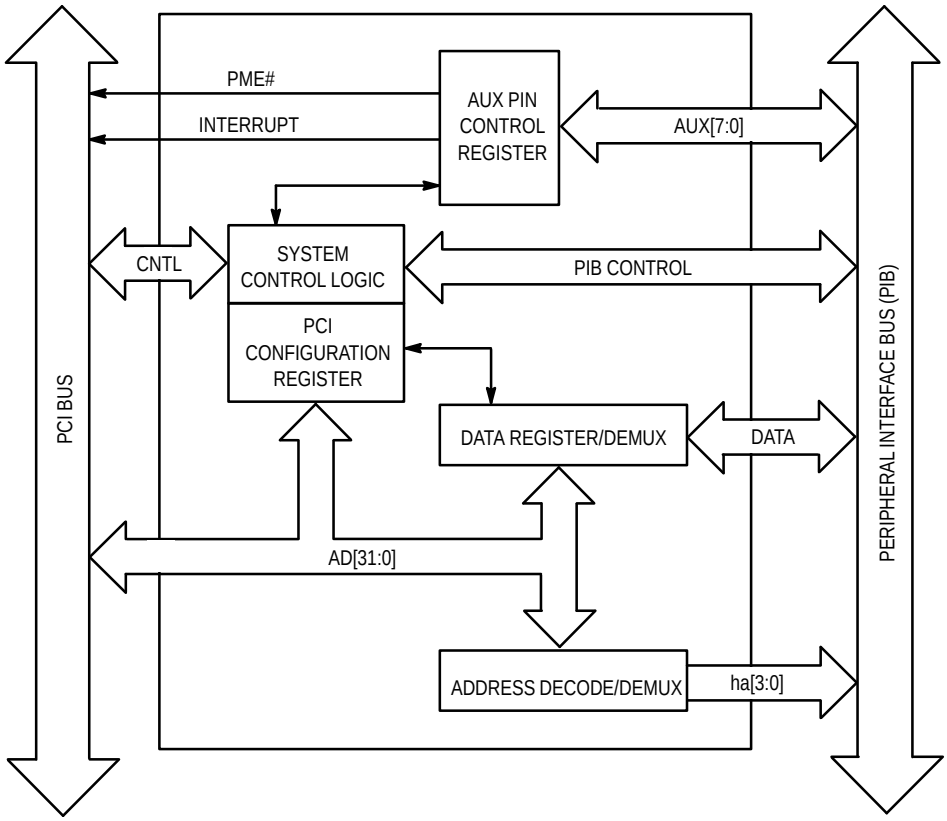
ORDERING INFORMATION

MC143421FU QFP

Features

- Fully Compliant 32–Bit PCI 2.1 Interface
- Four Address Lines and Byte–Wide Data
- Eight General Purpose I/O Lines
- ACPI Power Management and OnNow™ Support
- Single Digital 100–Pin QFP VLSI Implementation

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 0
2/98 TN98022400

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_A	Operating Temperature Range	– 25 to 75	°C
V	Voltage Range on Any Pin	– 0.5 to 5.5	V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Operating Temperature Range	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V

DC CHARACTERISTICS (Over the Recommended Operating Conditions)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	High Level Input Voltage	2.5	—	5.25	V	TTL Level
V_{IL}	Low Level Input Voltage	– 0.5	—	0.8	V	TTL Level
V_{CH}	CLK High Level Input	3.7	—	5.25	V	CMOS Level
V_{CL}	CLK Low Level Input	– 0.5	—	0.8	V	CMOS Level
V_{OH}	High Level Output Voltage	3.0	—	—	V	I_{OH} = 1 mA
V_{OL}	Low Level Output Voltage	—	—	0.45	V	I_{OL} = 4 mA
I_{LI}	Input Leakage Current	—	—	15	µA	
I_{IO}	Output Leakage Current	—	—	15	µA	
C_{in}	Input Capacitance	—	—	10	pF	fc = 1 MHz
C_{out}	Output Capacitance	—	—	15	pF	fc = 1 MHz
C_{CLK}	Clock Capacitance	—	—	20	pF	fc = 1 MHz

Table 1. Pin Descriptions

Pin No.	Signal Name	I/O Type	Function
1	C/BE[3]#	I	PCI Bus Command and Byte Enable
2	IDSEL	I	PCI Initialization Device Select; Chip Select for Configuration Read and Write Cycles
3	GND		Ground
4	V_{CC}		Power 5 V
5	AD[23]	I/O	PCI Bus Multiplexed Address and Data
6	AD[22]	I/O	PCI Bus Multiplexed Address and Data
7	AD[21]	I/O	PCI Bus Multiplexed Address and Data
8	AD[20]	I/O	PCI Bus Multiplexed Address and Data
9	GND		Ground
10	AD[19]	I/O	PCI Bus Multiplexed Address and Data
11	AD[18]	I/O	PCI Bus Multiplexed Address and Data
12	AD[17]	I/O	PCI Bus Multiplexed Address and Data
13	AD[16]	I/O	PCI Bus Multiplexed Address and Data
14	V_{CC}		Power 5 V
15	GND		Ground
16	C/BE[2]#	I	PCI Bus Command and Byte Enable
17	FRAME#	I	PCI Cycle Frame; Indicates the Beginning and Duration of a Bus Access
18	IRDY#	I	PCI Initiator Ready; Indicates the Bus Master's Ability to Complete the Current Data Phase of the Transaction
19	GND		Ground
20	TRDY#	O	PCI Target Ready; Indicates the Target Agent's Ability to Complete the Current Data Phase of the Transaction
21	DEVSEL#	O	PCI Device Select for Configuration Read and Write Cycles
22	STOP#	O	PCI Stop; Indicates the Current Target Request for Transceiver Termination
23	PAR	O	Indicates Even Parity Across AD[31:0] and C/BE[3:0]#
24	GND		Ground
25	V_{CC}		Power 5 V
26	C/BE[1]#	I	PCI Bus Command and Byte Enable
27	AD[15]	I/O	PCI Bus Multiplexed Address and Data
28	AD[14]	I/O	PCI Bus Multiplexed Address and Data
29	AD[13]	I/O	PCI Bus Multiplexed Address and Data
30	GND		Ground
31	AD[12]	I/O	PCI Bus Multiplexed Address and Data
32	AD[11]	I/O	PCI Bus Multiplexed Address and Data
33	AD[10]	I/O	PCI Bus Multiplexed Address and Data
34	AD[9]	I/O	PCI Bus Multiplexed Address and Data
35	GND		Ground
36	AD[8]	I/O	PCI Bus Multiplexed Address and Data
37	C/BE[0]#	I	PCI Bus Command and Byte Enable
38	AD[7]	I/O	PCI Bus Multiplexed Address and Data
39	AD[6]	I/O	PCI Bus Multiplexed Address and Data
40	GND		Ground
41	V_{CC}		Power 5 V
42	AD[5]	I/O	PCI Bus Multiplexed Address and Data

Table 1. Pin Descriptions (continued)

43	AD[4]	I/O	PCI Bus Multiplexed Address and Data
44	AD[3]	I/O	PCI Bus Multiplexed Address and Data
45	AD[2]	I/O	PCI Bus Multiplexed Address and Data
46	GND		Ground
47	AD[1]	I/O	PCI Bus Multiplexed Address and Data
48	AD[0]	I/O	PCI Bus Multiplexed Address and Data
49	$\overline{\text{READ}}$	O	PIB Read Strobe
50	$\overline{\text{WRITE}}$	O	PIB Write Strobe
51	$\overline{\text{RESET}}$	O	PIB Reset — Generated by PCI Reset
52	GND		Ground
53	V_{CC}		Power 5 V
54	ha[3]	O	PIB Address — Subsystem ID (Sampled at Reset)
55	ha[2]	O	PIB Address — Subsystem ID (Sampled at Reset)
56	ha[1]	O	PIB Address — Subsystem ID (Sampled at Reset)
57	ha[0]	O	PIB Address — Subsystem ID (Sampled at Reset)
58	GND		Ground
59	hd[7]	I/O	PIB Data — Subvender ID (Sampled at Reset)
60	hd[6]	I/O	PIB Data — Subvender ID (Sampled at Reset)
61	hd[5]	I/O	PIB Data — Subvender ID (Sampled at Reset)
62	hd[4]	I/O	PIB Data — Subvender ID (Sampled at Reset)
63	hd[3]	I/O	PIB Data — Subvender ID (Sampled at Reset)
64	hd[2]	I/O	PIB Data — Subvender ID (Sampled at Reset)
65	V_{CC}		Power 5 V
66	GND		Ground
67	hd[1]	I/O	PIB Data — Subvender ID (Sampled at Reset)
68	hd[0]	I/O	PIB Data — Subvender ID (Sampled at Reset)
69	aux[7]	I/O	PIB Programmable General Purpose I/O (See Figure 1)
70	aux[6]	I/O	PIB Programmable General Purpose I/O (See Figure 1)
71	aux[5]	I/O	PIB Programmable General Purpose I/O (See Figure 1)
72	aux[4]	I/O	PIB Programmable General Purpose I/O (See Figure 1)
73	GND		Ground
74	PME#	OC	PCI Power Management Event
75	NC		No Connect
76	NC		No Connect
77	NC		No Connect (Or 10 k Resistor Pull–Down — See Device Class Section)
78	NC		No Connect (Or 10 k Resistor Pull–Down — See Device Class Section)
79	V_{CC}		Power 5 V
80	aux[3]	I/O	PIB Programmable General Purpose I/O (See Figure 1)
81	aux[2]	I/O	PIB Programmable General Purpose I/O (See Figure 1)
82	aux[1]	I/O	PIB Programmable General Purpose I/O (See Figure 1)
83	aux[0]	I/O	PIB Programmable General Purpose I/O (See Figure 1)
84	GND		Ground
85	INTA#	O	PCI Interrupt
86	RST#	I	PCI Device Reset

Table 1. Pin Descriptions (continued)

87	CLK	I	PCI Bus Clock
88	NC		No Connect
89	NC		No Connect
90	GND		Ground
91	V_{CC}		Power 5 V
92	AD[31]	I/O	PCI Bus Multiplexed Address and Data
93	AD[30]	I/O	PCI Bus Multiplexed Address and Data
94	AD[29]	I/O	PCI Bus Multiplexed Address and Data
95	AD[28]	I/O	PCI Bus Multiplexed Address and Data
96	GND		Ground
97	AD[27]	I/O	PCI Bus Multiplexed Address and Data
98	AD[26]	I/O	PCI Bus Multiplexed Address and Data
99	AD[25]	I/O	PCI Bus Multiplexed Address and Data
100	AD[24]	I/O	PCI Bus Multiplexed Address and Data

NOTE: A # symbol at the end of a signal name indicates that it is active low and connects to the PCI Bus (per PCI specification conventions). An overbar symbol also indicates the pin is active low and connects to the Peripheral Interface Bus (per Motorola specification conventions).

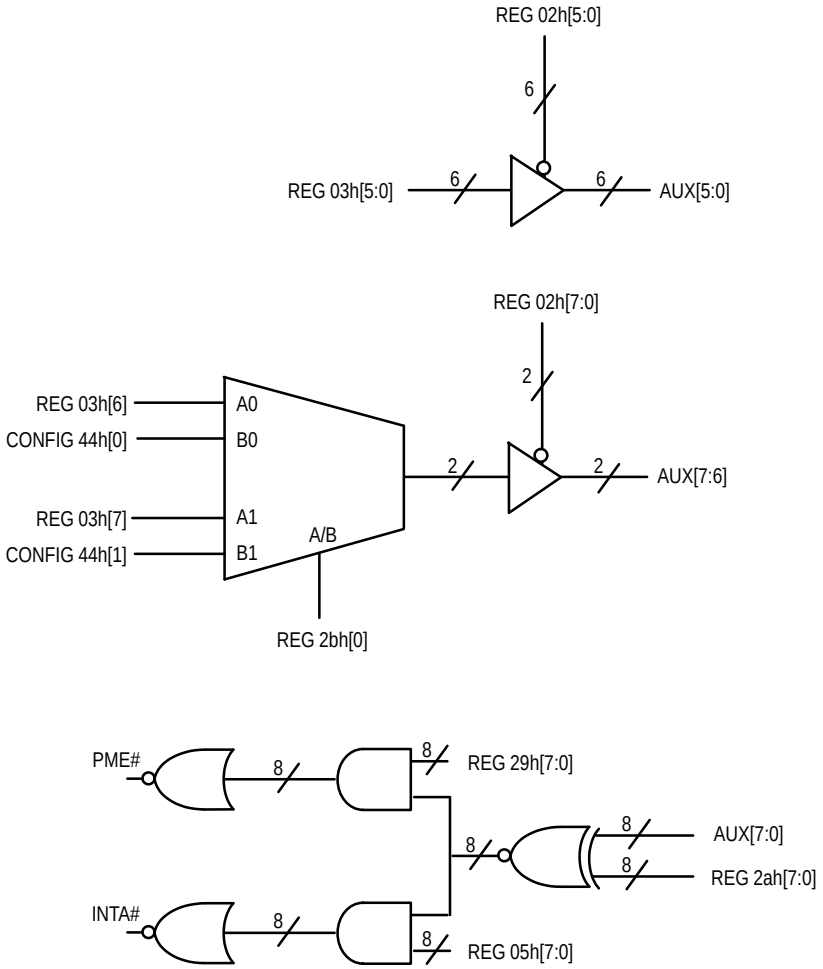


Figure 1. Logical Equivalence of AUX Pin Control Register

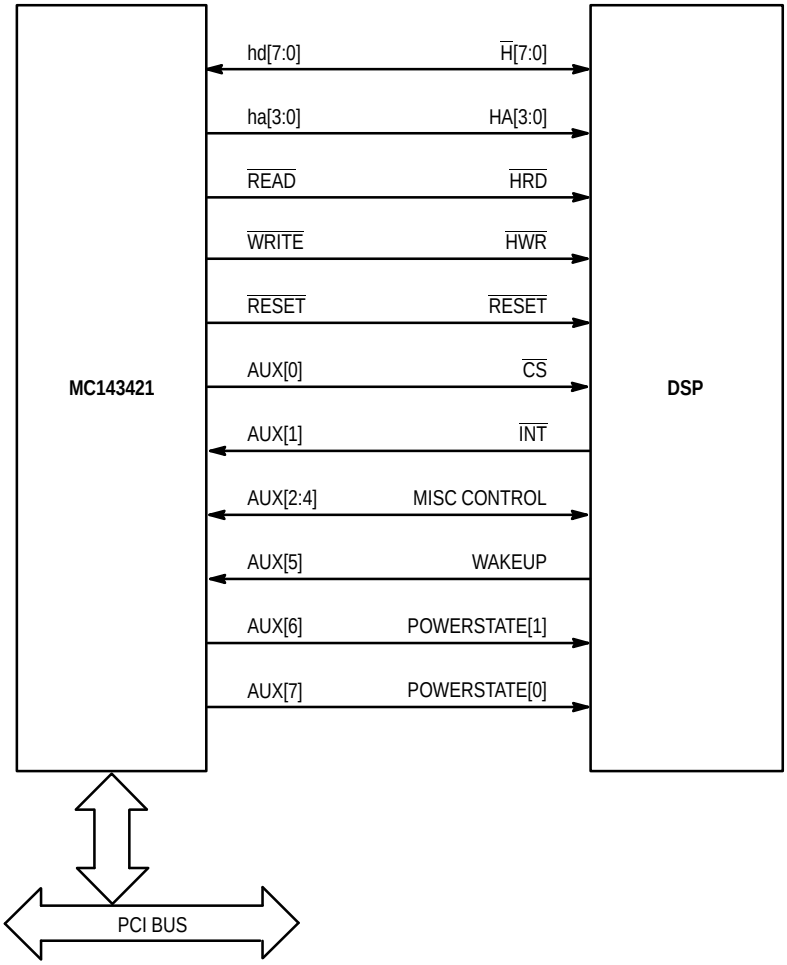


Figure 2. Typical Implementation

Table 2. PCI Configuration Space Description

Please reference PCI Specification 2.1 and “Addition of PME# Signal to Connector” ECN.

Offset	Bits	Type	Description	Value
00h	15:0	RO	Vendor ID	1057h
02h	31:16	RO	Device ID	3421h
04h	29	RO	Master Abort	
	28	RO	Target Abort	
	26:25	RO	Medium Device	2100000h
	20	RO	New Capabilities (ACPI)	
	2	RO	Master Enable	
	1	RW	Memory Enable	
	0	RW	I/O Enable	
08h	31:8	RO	PCI Multimedia Device	048000h
	7:0	RO	Revision ID	00h
0ch	23:16	RO	Header Type	0h
	15:8	RO	Latency Timer	
10h	31:8	RW	256–Byte I/O Space	
	7:1	RO	I/O Size	0h
	0	RO	I/O Space Indicator	1b
14h	31:12	RW	4K Memory Space	
	11:1	RO	Memory Size	0h
	0	RO	Memory Space Indicator	0b
2ch	31:20	RO	Subsystem ID	0h
	19:16	RO	Subsystem ID	From ha[3:0] During Reset
	15:8	RO	Subvendor ID	0h
	7:0	RO	Subvendor ID	From hd[7:0] During Reset
34h	7:0	RO	Cap_Ptr (ACPI)	40h
3ch	15:11	RO	Interrupt Pin	0h
	10:8	RO	INTA#	1b
	7:0	RW	Interrupt Line	
40h	31:0	RO	PMC (ACPI)	6c210001h
44h	15	RW	PEN_status — This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the function to stop asserting a PME# (if enabled). Writing a 0 has no effect.	
	8	RW	PEN_EN — A 1 enables the function to assert PME#. When 0, PME# assertion is disabled.	
	1:0	RW	PowerState — This two–bit field is used both to determine the current power state of the function and to set the function into a new power state. The definition of the field values is given below: 00b D0 01b D1 10b D2 11b $D3_{hot}$	

NOTES:
1. RO: Read Only Register
2. RW: Read and Write Register
3. All other registers not shown in the table will return 0s.

PERIPHERAL INTERFACE BUS

Pin Description

Pin	Signal Type	Description
$\overline{\text{RESET}}$	Output	Reset Signal, Active Low
$\overline{\text{READ}}$	Output	Read Command Pulse Signal, Active Low
$\overline{\text{WRITE}}$	Output	Write Command Pulse Signal, Active Low
ha[3:0]	Output	4–Bit Address Bus
hd[7:0]	In/Out	8–Bit Data Bus

Address Mapping

A31:A8	A7	A6	A5	A4	A3	A2	A1	A0
PCI A31 to A8 equal to config register 10h	1	1	ha [3]	ha [2]	ha [1]	ha [0]	X	X

A31 to A8 from the PCI bus are compared to the value in configuration register 10h, when a match occurs and both A7 and A6 are equal to 1, the lower eight bits are mapped as follows:

A5 mapped to ha[3]
A4 mapped to ha[2]
A3 mapped to ha[1]
A2 mapped to ha[0]
A0 and A1 are ignored

PCI Read Operation

The MC143421 will translate the PCI I/O cycle to the ISA–like Peripheral Interface Bus (PIB) that connects to the peripheral function. In the event of a PCI I/O read operation, and if the address is qualified for the address mapping of the PIB, the $\overline{\text{READ}}$ control signal on the PIB will be activated for at least three PCI cycles.

The input data, from the eight–bit data port on the PIB, will be latched on the rising edge of the $\overline{\text{READ}}$ signal and transferred to the PCI bus. The PCI address bus is driven by the MC143421 one cycle prior to the falling edge of the $\overline{\text{READ}}$ pulse and at least one cycle after the rising edge or the $\overline{\text{READ}}$ pulse. The setup and hold time for the MC143421 to successfully latch the data from the PIB is 3 ns.

PCI Write Operation

The write operation is complementary to the read with the same timing, the data and address information on the PIB is valid one cycle prior to the falling edge of the PIB $\overline{\text{WRITE}}$ pulse. The data will remain valid until one cycle after the rising edge of the PIB $\overline{\text{WRITE}}$ pulse. The address valid time is the same as the read operation.

Subsystem ID and Subvendor ID

When the MC143421 is reset, the states of the hd[7:0] and ha[3:0] pins are read into the subsystem ID and subvendor ID registers. The inputs are matched to register 2Ch as shown in Table 3.

Pins hd[0] and ha[0] are internally lightly pulled up, and hd[7:1] and ha[3:1] are internally lightly down. If these pins are left floating on reset, the resulting subsystem and subvendor IDs will be 1. External pullups and pulldowns are required for unique subvendor and subsystem IDs.

Device Class

The MC143421 is classified as a PCI Multimedia Device. Pins 77 and 78 are internally lightly pulled down, and can be left as no connects, or externally pulled down. If either of these pins are pulled up, it will result in an invalid vendor and device ID.

Table 3. Register 2Ch

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	ha3	ha2	ha1	ha0
Subsystem ID															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	hd7	hd6	hd5	hd4	hd3	hd2	hd1	hd0
Subvendor ID															

INTERNAL REGISTER DESCRIPTION

Offset	Bits	Description
00h	0	External reset, controlling pin $\overline{\text{ERESET}}$ on the PIB
	1	Reserved
	2	Reserved
	3	Reserved
	5:4	00: PIB three–cycle operation 01: PIB five–cycle operation 1–: PIB twelve–cycle operation
	6	Reserved
	7	Reserved
01h	7:0	Reserved
02h	7:0	AUX pin control register. The corresponding AUX pin is an output when set to 1.
03h	7:0	AUX pin data register. When AUX pin is set as an output, the output state will be controlled by this register.
04h	7:0	Reserved
05h	7:0	Interrupt 1 mask register. Selects the AUX input that will generate the interrupt.
06h	7:0	Reserved
07h	7:0	AUX pin status register. Reads the status of the AUX pin.
29h	7:0	ACPI mask register. Set to 1 to select the AUX input to be used to enable PME# output. Enables an external event (such as a ring) to switch on the computer.
2ah	7:0	AUX pin data polarity control register. Set to 1 to invert the polarity of data.
2bh	0	AUX pin data select register. Bit 0 set to 1, AUX[6:7] becomes power state bit (reference PCI config register 44h[1:0]).
C0 to FF	7:0	Peripheral Interface Bus Addressing

Access Procedures

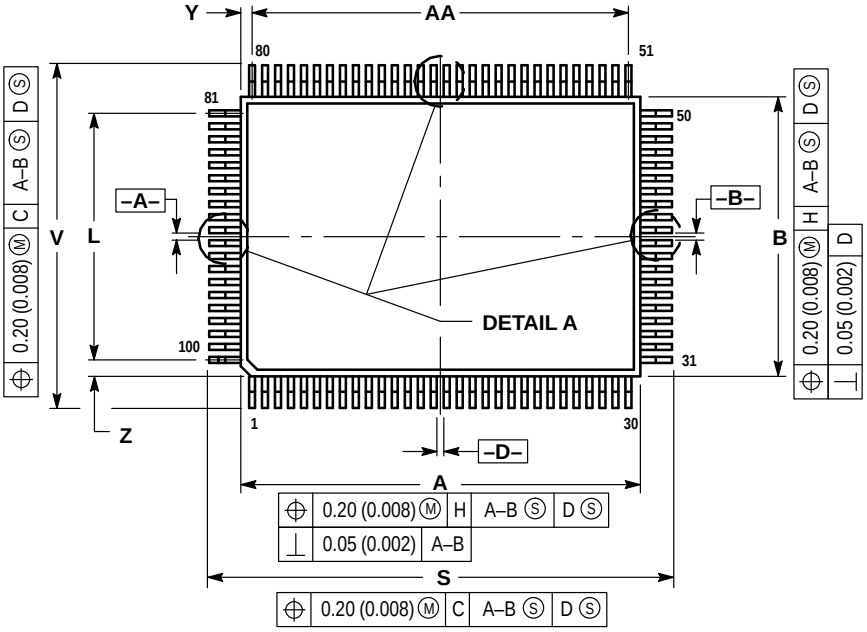
All the internal registers are IO/MEM mapped. They can be accessed with either I/O or memory read/write command from the PCI bus.

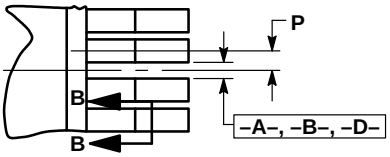
For I/O access, the host needs to send the address with bits A31 to A8 to match the data in configuration register 10h bits 31 to 8. Also, the address bits 7 and 6 need to be set to 0.

For memory access, the address bits A31 to A12 need to match the value in configuration register 14h bits 31 to 12 and the address bits 11 to 6 need to all be 0. The internal registers are byte addressable.

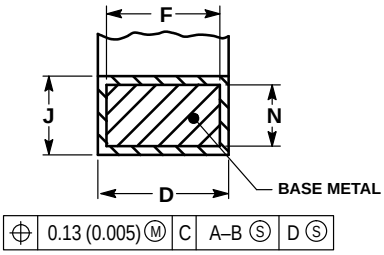
PACKAGE DIMENSIONS

FU SUFFIX
QFP (Quad Flat Package)
CASE 842D–03

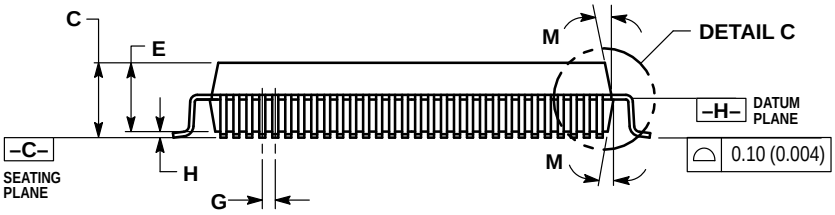


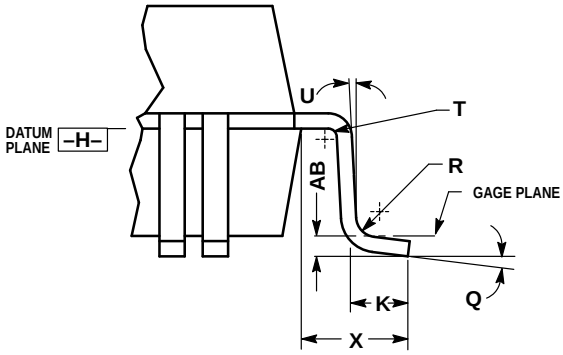


DETAIL A



SECTION BB
ROTATED 90° CLOCKWISE





DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46 (0.018). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.90	20.10	0.783	0.791
B	13.90	14.10	0.547	0.555
C	—	3.30	—	0.130
D	0.22	0.38	0.009	0.015
E	2.55	3.05	0.100	0.120
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	0.10	0.36	0.004	0.014
J	0.11	0.23	0.004	0.009
K	0.73	1.03	0.028	0.040
L	12.35 REF		0.486 REF	
M	5°	16°	5°	16°
N	0.11	0.17	0.004	0.007
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.25	0.35	0.010	0.014
S	23.65	24.15	0.931	0.951
T	0.13	—	0.005	—
U	0°	—	0°	—
V	17.65	18.15	0.695	0.715
X	1.95 REF		0.077 REF	
Y	0.58 REF		0.023 REF	
Z	0.83 REF		0.033 REF	
AA	18.85 REF		0.742 REF	
AB	0.25 BSC		0.010 BSC	

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ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

CUSTOMER FOCUS CENTER: 1–800–521–6274