P/Active™ IEEE 1284 ECP/EPP Termination Network

Features

- 28-pin QSOP package
- 17 filtering lines in a single package
- In-system ESD protection to 30kV contact discharge per IEC 61000-4-2

Application

- Low cost Parallel Port Terminations and Filters for PCs and peripherals
- Set-Top-Boxes for Internet Access

Product Description

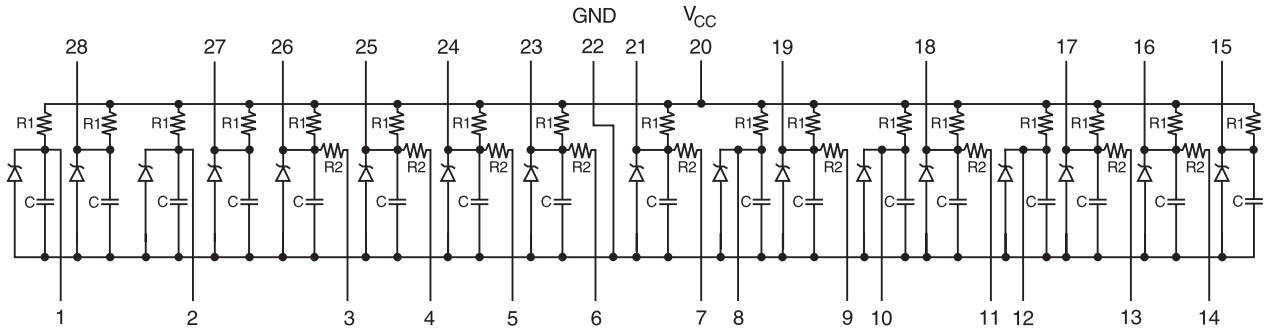
California Micro Devices' filtering/ESD network provides an integrated parallel port solution in a single QSOP package.

Enhanced high-speed parallel ports are used to provide communications between PC's, workstations, and external devices such as tape back-up drives, ZIP drives, printers, parallel port SCSI adapters, external LAN adapters, scanners, video capture, and other PC peripherals. These ports support bi-directional transfers to 2MB/sec. In addition, government EMC limits impose filtering requirements on the parallel port. The device provides a complete parallel port termination solution. It integrates the equivalent of 60 discrete components and is ideal for space critical applications. The pins of the device which connect to the parallel port are protected to 30kV contact discharge, well beyond Level 4 of the IEC 61000-4-2 specification. All other pins are ESD protected for contact discharges up to 8kV per IEC 61000-4-2.

There are two available values for the pull-up resistor R1. The PACSZ1284-01 has R1 = 1kΩ, and the PACSZ1284-02 has R1 = 2.2kΩ.

California Micro Devices' technology provides high reliability and low cost through manufacturing efficiency. California Micro Devices' solution is silicon-based and has the same reliability characteristics as today's integrated circuits.

SCHEMATIC CONFIGURATION



	STANDARD PART ORDERING INFORMATION			
	Package		Ordering Part Number	
RC Code	Pins	Style	Part Number	Part Marking
01	28	QSOP	PACSZ128401Q	PACSZ128401Q
02	28	QSOP	PACSZ128402Q	PACSZ128402Q

When placing an order please specify desired shipping: Tube or Tape and Reel.

C0970500

ABSOLUTE MAXIMUM RATINGS		
Parameter	**Rating**	**Unit**
V_{CC} Voltage	5.5	V
Input Voltage range, no clamping	–0.4 to 5.5	V
Temperature Storage:	–40 to 150	°C
Operating Ambient	0 to +70	
Operating Junction	0 to +125	
Power Dissipation per resistor	0.1	W
Package Power Dissipation	1.0	W

OPERATING CONDITIONS (unless specified otherwise)		
Parameter	**Rating**	**Unit**
V_{CC} Voltage	5.0	V
Ambient Temperature	0 to +70	°C

ELECTRICAL OPERATING CHARACTERISTICS (over operating conditions unless specified otherwise)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
R1, R2	Resistance tolerance	Measured at 25°C	–20		20	%
C	Capacitor tolerance	Measured at 1MHz, 2.5V DC	–20		20	%
I_{LEAK}	Leagage current to ground	Measured at 5.5V, 25°C		1	10	µA
V_{ESDi}	ESD protection, input pins	Pins 3-7,9, 11, 13, 14, 2 IEC61000-4-2 specification	±8			kV
V_{ESD}	ESD protection, connector pins	Pins 1, 2, 3, 8, 10, 12, 15-19, 21, 23-28, IEC61000-4-2 specification	±30			kV
V_{CLAMP}	Clamping voltage under ESD discharge	(ESD applied to connector pin, measured at corresponding input pin) 8kV discharge, Human body model -8kV discharge, Human body model		8.3 –2.7		V V

Note 1: Pins 3-7, 9, 11, 13, and 14 typically connect to the I/O pins of the Super I/O chip.

Note 2: Pins 1, 2, 8, 10, 12, 15, 16, 17, 18, 19, 21, and 23-28 typically connect to the Parallel Port Connector.

Note 3: ESD voltage is applied between Input/Connector Pins and ground, one pin at a time (guaranteed by design and characterization).

STANDARD VALUES			
R1 (Ω)	**R2 (Ω)**	**C (pf)**	**RC Code**
1.0k	33	150	01
2.2k	33	150	02

Application Information

The IEEE 1284 specification requires both termination and EMI filtering on a total of 17 lines. Basic filtering is provided through the presence of a capacitor on all signal lines. The filter capacitor is the junction capacitance of an ESD diode. The typical capacitance at a reverse voltage of 2.5V is 150pF. This diode capacitance is somewhat voltage dependent. See Figure 1.

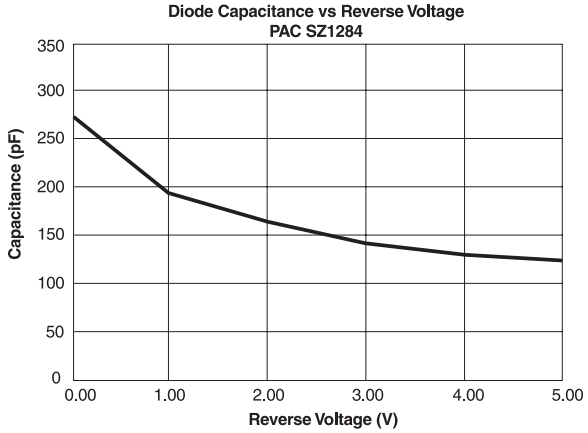


Figure 1

The higher speed Data and Strobe lines (9 in total) require an additional series resistor termination for proper operation while the eight (8) Status lines do not. See Table 1.

Signal Name	Series Termination
Data 1— Data 8	Yes
Strobe	Yes
Init	Not Required
AutoFeedXT	Not Required
Selection	Not Required
Ack	Not Required
Busy	Not Required
Paper Empty	Not Required
Select	Not Required
Fault	Not Required

Table 1

Figure 2 shows the typical Insertion Loss graphs of the PACSZ1284 for Data and Strobe signals. The curves are dependent on the physical location of the filter elements with respect to the ground terminal of this device. These graphs are measured in a 50 Ohm environment on a Hewlett Packard HP 8753C Analyzer. The signal source is introduced at the resistor input and the output is measured at the corresponding protection diode. The actual pins measured are labeled in the graph.
See Figure 2.

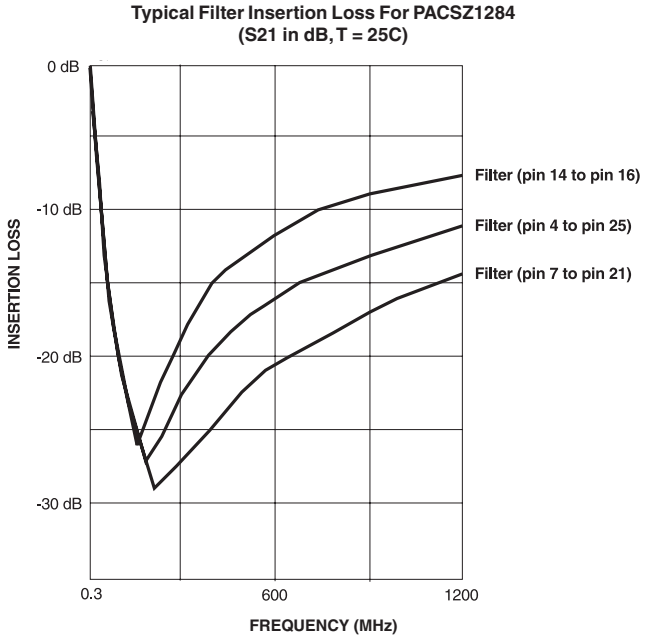


Figure 2