ULTRA-COMPACT REAL-TIME CLOCK IC

RS5C313

APPLICATION MANUAL

RICOH

ELECTRONIC DEVICES DIVISION

NO.EA-034-9908

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June 1995

RS5C313

APPLICATION MANUAL

CONTENTS

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OUTLINE

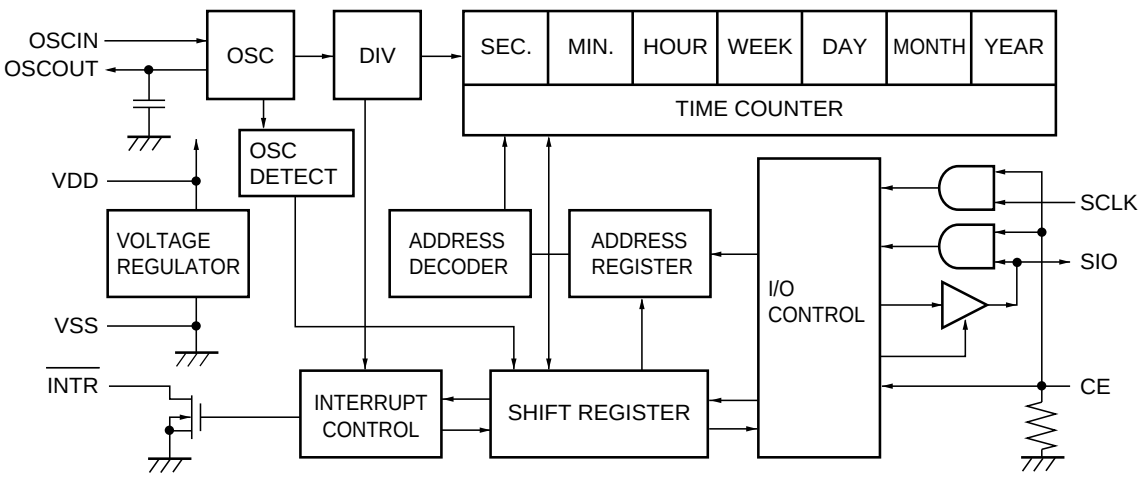
The RS5C313 is a CMOS type real-time clock which is connected to the CPU via three signal lines and capable of serial transmission of clock and calendar data to the CPU. The RS5C313 can generate various interrupt clock pulses lasting for long periods (one month). Driving an oscillation circuit at constant voltage, the circuit undergoes few voltage fluctuations and consequently realizes low current consumption (TYP. 0.7µA at 3 V). It also provides an oscillator halt sensing function for application to data validity at power-on and other occasions. Integrated into an ultra-compact and ultra-thin 8pin SSOP (0.65mm pitch), the RS5C313 is the optimum choice for equipment requiring small size and low power consumption.

There is RS5C314 reversing the logic of serial clock for series goods.

FEATURES

- Time Keeping Supply Voltage: 1.6 to 6.0 V
- Operating Supply Voltage: 2.7 to 6.0 V
- Low Current Consumption: TYP. 0.7µA (MAX. of 1.5µA) at 3V
- Connection to the CPU via only three pins: CE, SCLK, and SIO (for addressing and data read and write operations)
- A clock counter (counting hours, minutes, and seconds) and a calendar counter (counting leap years, years, months, days, and days of the week) in binary-coded decimal (BCD) code
- Generation of interrupt pulses to the CPU with cycles ranging from 1 month to 1/1024 Hz, interrupt flags, and interrupt halt
- Software-based alarming through clock-interlocked interrupt operation
- Oscillator halt sensing to judge internal data validity
- Second digit adjustment by ±30 seconds
- 12-hour or 24-hour time display selectable
- Automatic leap year recognition up to the year 2099
- CMOS logic
- Package: 8pin SSOP (0.65mm pitch)

BLOCK DIAGRAM

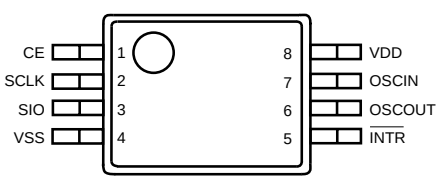


APPLICATIONS

- Communication equipment (Multi-function telephone, portable telephone, PHS, Pager)
- Office automation (Facsimile, portable facsimile)
- Personal computer (Desk top type, notebook type, word proccesor, PDA, electronic notebook, TV games)
- Audio visual equipment (Portable audio equipment, video camera, camera, digital camera, remote control equipment)
- Home use (Rice cooker, microwave range)

PIN CONFIGURATION

• 8pin SSOP



PIN DESCRIPTIONS

Pin No.	Symbol	Name	Description
1	CE	Chip enable input	The CE pin is used to interface with the CPU and is accessible when held at the high level. This pin incorporates a pull-down resistor. It should be switched to the low level or opened when not accessed or when powering off the system. Holding the CE pin at the high level for more than 2.5 seconds forces 1Hz interrupt pulses to be output from the $\overline{\text{INTR}}$ pin for oscillation frequency measurement . (No pulse is output for less than 1.5 seconds.)
2	SCLK	Shift clock input	The SCLK pin is used to input shift clock pulses to synchronize data input to, and output from, the SIO pin.
3	SIO	Serial input and output	The SIO pin inputs and outputs written or read data in synchronization with and output shift clock pulses from the SCLK pin. The SIO pin causes high impedance when the CE pin is held at the low level. After the CE pin is switched to the high level and the control bits and the address bits are input from the SIO, the SIO pin performs serial input and output operations
5	$\overline{\text{INTR}}$	Interrupt output	The $\overline{\text{INTR}}$ pin outputs cyclic interrupt pulses to the CPU. This pin functions as an Nch open drain output even when the CE pin is held at the low level.
7 6	OSCIN OSCOUT	Oscillation circuit input and output	These pins configure an oscillation circuit by connecting a 32.768 kHz crystal oscillator between the OSCIN and OSCOUT pins and by connecting a capacitor between the OSCIN and V_{SS} pins. (Any other oscillation circuit components are built into the RS5C313.)
8 4	V_{DD} V_{SS}	Positive power supply input Negative power supply input	The VDD pin is connected to a power supply and the V_{SS} pin is connected to the ground.

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Symbol	Item	Conditions	Ratings	Unit
V_{DD}	Supply voltage		–0.3 to +7.0	V
V_I	Input voltage		–0.3 to +V_{DD}+0.3	V
V_{O1}	Output voltage1	SIO	–0.3 to +V_{DD}+0.3	V
V_{O2}	Output voltage2	$\overline{INTR}$	–0.3 to +12	V
P_D	Maximum power consumption	Topt=25˚C	300	mW
Topt	Ambient operating temperature		–30 to +80	˚C
Tstg	Storage temperature		–40 to +125	˚C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Topt=–30 to +80°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD}	Operating supply voltage		2.7	5.0	6.0	V
V_{CLK}	Time Keeping supply voltage		1.6		6.0	V
f_{XT}	Oscillation frequency			32.768		kHz
C_G	External oscillator capacitance	C_L value of crystal=6 to 8pF	5	10	24	pF
V_{PUP}	Applied voltage at OFF	$\overline{INTR}$			10	V

DC CHARACTERISTICS

Unless otherwise specified:V_{SS}=0V, V_{DD}=5V±10%, Topt=–30 to +80°C, oscillation frequency=32.768kHz (C_L=6pF, R_1=30kΩ), C_G=10pF

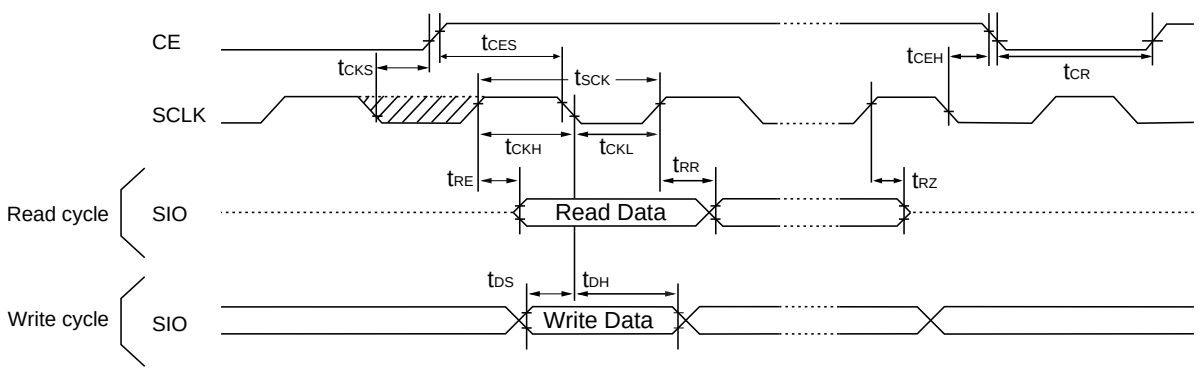
Symbol	Item	Pin name	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH}	"H" input voltage	CE, SCLK, SIO		0.8V_{DD}		V_{DD}	V
V_{IL}	"L" input voltage	CE, SCLK, SIO		0		0.2V_{DD}	V
I_{OH}	"H" output current	SIO	V_{OH}=V_{DD}–0.5V			–1	mA
I_{OL1}	"L" output current	SIO	V_{OL1}=0.5V	1			mA
I_{OL2}		$\overline{INTR}$	V_{OL2}=0.4V	2			
R_{DN}	Pull-down resistance	CE		45	130	450	kΩ
I_{ILK}	Input leakage current	SCLK	V_I =V_{DD} or V_{SS}	–1		1	µA
I_{OZ1}	Output off-state leakage current	SIO	V_O=V_{DD} or V_{SS}	–2		2	µA
I_{OZ2}		$\overline{INTR}$	V_O=10V	–5		5	
I_{DD1}	Power consumption 1	V_{DD}	V_{DD}=3V I/O=OPEN		0.7	1.5	µA
I_{DD2}	Power consumption 2	V_{DD}	V_{DD}=5.5V I/O=OPEN			2	µA
C_D	Internal oscillator capacitance	OSCOUT			10		pF

AC CHARACTERISTICS

(V_{SS}=0V, Topt=–30 to +80°C, C_L=50pF)

Symbol	Item	V_{DD}=5V±10%		V_{DD}=3V±10%		V_{DD}=5V±20%		Unit
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{CES}	CE set-up time	175		300		200		ns
t_{CEH}	CE hold time	175		300		200		ns
t_{CR}	CE recovery time	350		600		400		ns
t_{SCK}	SCLK clock cycle	350		600		400		ns
t_{CKH}	SCLK “H” clock time	175		300		200		ns
t_{CKL}	SCLK “L” clock time	175		300		200		ns
t_{CKS}	SCLK clock set-up time	60		100		80		ns
t_{RE}	Data output start time (from ↑ of SCLK)		120		200		135	ns
t_{RR}	Data output delay time (from ↑ of SCLK)		120		200		135	ns
t_{RZ}	Output floating time		120		200		135	ns
t_{DS}	Input data set-up time	50		80		60		ns
t_{DH}	Input data hold time	50		50		50		ns

TIMING CHART



Input/output conditions

V_{IH} = 0.8 × V_{DD}
V_{IL} = 0.2 × V_{DD}
V_{OH} = 0.8 × V_{DD}
V_{OL} = 0.2 × V_{DD}

*) The ability that is fair in “H” or “L” slanted line department

FUNCTIONAL DESCRIPTIONS

1. Addressing

	Address				Description	Data*1			
	A3	A2	A1	A0		D3	D2	D1	D0
0	0	0	0	0	1-second counter	S_8	S_4	S_2	S_1
1	0	0	0	1	10-second counter	—*2	S_{40}	S_{20}	S_{10}
2	0	0	1	0	1-minute counter	M_8	M_4	M_2	M_1
3	0	0	1	1	10-minute counter	—	M_{40}	M_{20}	M_{10}
4	0	1	0	0	1-hour counter	H_8	H_4	H_2	H_1
5	0	1	0	1	10-hour counter	—	—	$P/\overline{A}$ or H_{20}	H_{10}
6	0	1	1	0	Day-of-the-week counter	—	W_4	W_2	W_1
7	0	1	1	1	Interrupt cycle register	CT_3	CT_2	CT_1	CT_0
8	1	0	0	0	1-day counter	D_8	D_4	D_2	D_1
9	1	0	0	1	10-day counter	—	—	D_{20}	D_{10}
A	1	0	1	0	1-month counter	MO_8	MO_4	MO_2	MO_1
B	1	0	1	1	10-month counter	—	—	—	MO_{10}
C	1	1	0	0	1-year counter	Y_8	Y_4	Y_2	Y_1
D	1	1	0	1	10-year counter	Y_{80}	Y_{40}	Y_{20}	Y_{10}
E	1	1	1	0	Control register	CTFG	$\overline{12}/24$	WTEN/XSTP*3	ADJ/BSY*4
F	1	1	1	1	Test register	—	—	—	$\overline{TEST}$

*1) All the listed data can be read and written .
*2) The "—" mark indicates data which can be read only and set to "0" when read .
*3) The WTEN/XSTP bit of the control register is set to WTEN for write operation and XSTP for read operation.
*4) The ADJ/BSY bit of the control register is set to ADJ for write operation and BSY for read operation.

2. Register

2.1 Control Register (at Eh)

D3	D2	D1	D0	
CTFG	$\overline{12}$/24	WTEN	ADJ	(For write operation)
CTFG	$\overline{12}$/24	XSTP	BSY	(For read operation)

±30-second Adjustment Bit

ADJ	Description
0	Ordinary operation
1	Second digit adjustment

Clock/Calendar Counter Busy-state Indication Bit

BSY	Description
0	Ordinary operation
1	Second digit carry or adjustment

Clock Counter Enable/Disable Setting Bit

WTEN	Description
0	Disabling of 1-second digit carry for clock counter
1	Enabling of 1-second digit carry for clock counter

Oscillator Halt Sensing Bit

XSTP	Description
0	Ordinary oscillation
1	Oscillator halt sensing

12/24-hour Time Display System Selection Bit

$\overline{12}$/24	Description
0	12-hour time display system (separate for mornings and afternoons)
1	24-hour time display system

Interrupt Flag Bit

CTFG	Description
0	$\overline{INTR}$=H (Nch Open Drain). Enabling of write operation when the CT3 bit is set to 1.
1	$\overline{INTR}$=L (Nch Open Drain). Enabling of write operation when the CT3 bit is set to 1.

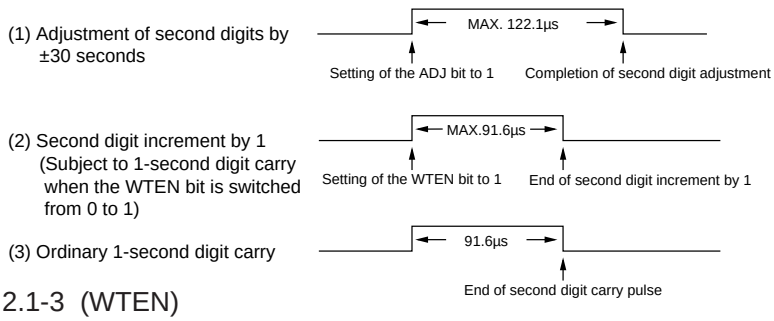
2.1-1 (ADJ)

When the ADJ bit is set to 1: (If the WTEN bit is 0, adjustment of second digits is started after the WTEN bit is set to 1.)

1) For second digits ranging from 00 to 29 seconds: Time counts smaller than seconds are reset to set second digits to “00”.
2) For second digits ranging from 30 to 59 seconds: Time counts smaller than seconds are reset to set second digits to “00” and increment minute digits by 1. After the ADJ bit is set to 1, the BSY bit is set to 1 for the maximum duration of 122.1µs.

2.1-2 (BSY)

When the BSY bit is 1, the clock and calendar counters are being updated. Consequently, write operation should be performed for the counters when the BSY bit is 0. Meanwhile, read operation is normally performed for the counters when the BSY bit is 0, but can be performed without checking the BSY bit as long as appropriate software is provided for preventing read errors(Refer to the item 11.3 Read Operation from Clock and Calendar Counters). The BSY bit is set to 1 in the following three cases:



2.1-3 (WTEN)

The WTEN bit should be set to 0 to check that the BSY bit is 0 when performing read and write operations for the clock and calendar counters. For read operation, the WTEN bit may be left as 1 without checking the BSY bit as long as appropriate measures such as read repetition are provided for preventing read errors(Refer to the item 11.3 Read Operation from Clock and Calendar Counters). The WTEN bit should be set to 1 after completing read and write operations, or will automatically be set to 1 by switching the CE pin to the low level. If 1-second digit carry occurs when the WTEN bit is 0, a second digit increment by 1 occurs when the WTEN bit is set to 1.

Note

If the WTEN bit is 0 for 1/1024 second and more, second digit increment by 1 may not occur. (Refer to the item 11.3 Read Operation from Clock and Calendar Counters).

2.1-4 (XSTP)

The XSTP bit senses the ocilllator halt. When the CE pin is held at the low level, the XSTP bit is set to 1 once the crystal oscillator is stopped after initial power-on or supply voltage drop and left to be 1 after it is restarted. When the CE pin is held at the high level, the XSTP bit is left as it was when the CE pin was held at the low level without checking oscillation stop. As such, the XSTP bit can be used to validate clock and calendar count data after power-on or supply voltage drop. The XSTP bit is set to 0 when write operation is performed for the control register (at Eh) (during normal oscillation).

2.1-5 ($\overline{12}$/24)

The 12/24 bit specifies time digit display in BCD code.

24-hour time display system	12-hour time display system	24-hour time display system	12-hour time display system
00	12(AM12)	12	32(PM12)
01	01(AM 1)	13	21(PM 1)
02	02(AM 2)	14	22(PM 2)
03	03(AM 3)	15	23(PM 3)
04	04(AM 4)	16	24(PM 4)
05	05(AM 5)	17	25(PM 5)
06	06(AM 6)	18	26(PM 6)
07	07(AM 7)	19	27(PM 7)
08	08(AM 8)	20	28(PM 8)
09	09(AM 9)	21	29(PM 9)
10	10(AM10)	22	30(PM10)
11	11(AM11)	23	31(PM11)

Either the 12-hour or 24-hour time display system should be selected before time setting (e.g. during initialization after power-on).

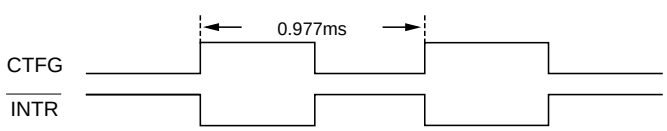
2.1-6 (CTFG)

The CTFG bit is set to 1 when interrupt pulses are output from the $\overline{\text{INTR}}$ pin held at the low level.
There are two interrupt modes selectable: the pulse mode (when the CT_3 bit is set to 0) and the level mode (when the CT_3 bit is set to 1).
The CTFG bit can be set only when the CT_3 is set to 1. Setting the CTFG bit to 1 switches the $\overline{\text{INTR}}$ pin to the low level while setting the CTFG bit to 0 turns off the $\overline{\text{INTR}}$ pin.

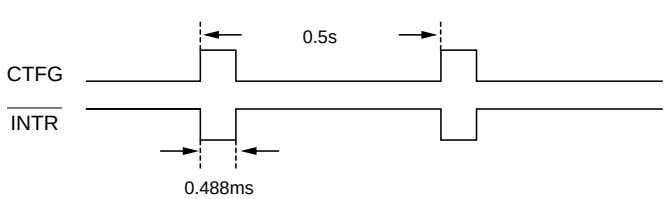
Interrupt cycle register				Outputs from $\overline{\text{INTR}}$ pin	Remarks
CT_3	CT_2	CT_1	CT_0		
0	*[*1]	0	0	OFF	Interrupt disabling
0	*	0	1	ON	Fixing $\overline{\text{INTR}}$ pin at low level
0	*	1	0	0.977ms	Cycle: 0.977 ms (1/1024 Hz), Duty: 50% *[2]
0	*	1	1	0.5s	Cycle: 0.5 s (1/2 Hz)*[3]
1	0	0	0	1 second	Every second*[4]
1	0	0	1	10 seconds	Every 10 seconds (For display of second digits: 00, 10, 20, 30, 40, and 50)*[4]
1	0	1	0	1 minute	Every minute (00 second)*[4]
1	0	1	1	10 minutes	Every 10 minutes (00 second) (For display of minute digits: 00, 10, 20, 30, 40, and 50)*[4]
1	1	0	0	1 hour	Every hour (00 minute and 00 second)*[4]
1	1	0	1	1 day	Every day (0 hour, 00 minute, and 00 second a.m.)*[4]
1	1	1	0	1 week	Every week (0 week, 0 hour, 00 minute, and 00 second a.m.)*[4]
1	1	1	1	1 month	Every month (1st day, 0 hour, 00 minute, and 00 second a.m.)*[4]

1) The symbol "" in the above table indicates 0 or 1.

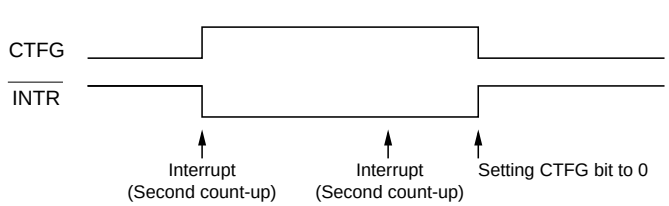
*2)



*3)



*4)



2.2 Interrupt Cycle Register (at 7h)

D3	D2	D1	D0	
CT_3	CT_2	CT_1	CT_0	(For write operation)
CT_3	CT_2	CT_1	CT_0	(For read operation)

Bits for selecting the interrupt cycle and output mode at the $\overline{INTR}$ pin*1

*1) (CT_3 to CT_0)
The CT_3 to CT_0 bits are used to select the interrupt cycle and output mode at the $\overline{INTR}$ pin. There are two interrupt modes selectable: the pulse mode (when the CT_3 bit is set to 0) and the level mode (when the CT_3 bit is set to 1).
The interrupt cycle and output mode at the $\overline{INTR}$ pin are shown in detail in the section on the CTFG bit in "2.1 Control Register (at Eh)".

2.3 Test Register (at Fh)

D3	D2	D1	D0	
*	*	*	$\overline{TEST}$	(For write operation)
0	0	0	0	(For read operation)*1

Bit For Testing*2

$\overline{TEST}$	Description
0	Testing mode
1	Ordinary operating mode

*1) The $\overline{TEST}$ bit is write-only and set to 0 when read.
*2) The $\overline{TEST}$ bit should be fixed at 1 for ordinary operation and will automatically be set to 1 when the CE pin is at the low level.

3. Counters

3.1 Clock Counter (at 0h to 5h)

D3	D2	D1	D0	
S_8	S_4	S_2	S_1	(read and write cycle) 1-second time digit (at 0h)
*	S_{40}	S_{20}	S_{10}	(read and write cycle) 10-second time digit (at 1h)
M_8	M_4	M_2	M_1	(read and write cycle) 1-minute time digit (at 2h)
*	M_{40}	M_{20}	M_{10}	(read and write cycle) 10-minute time digit (at 3h)
H_8	H_4	H_2	H_1	(read and write cycle) 1-hour time digit (at 4h)
*	*	P/$\overline{A}$ or H_{20}	H_{10}	(read and write cycle) 10-hour time digit (at 5h)

1) The "*" mark in the above table indicates data which are set to 0 for read cycle and not set for write cycle.
2) Any carry to 1-second digits from the second counter is disabled when the WTEN bit (of the control register) is set to 0.
3) Time digit display (BCD code):
   Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
   Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
   Hour digits: Range as shown in the section on the $\overline{12}$/24 bit and carried to day and day-of-the-week.
   digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.
4) Any registered imaginary time should be replaced with actual time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter to malfunction.

3.2 Day-of-the-week Counter (at 6h)

D3	D2	D1	D0	
*	W_4	W_2	W_1	(read and write cycle) Day-of-the-week counter

1) The "*" mark in the above table indicates data which are set to 0 for read cycle and not set for write cycle.
2) Day-of-the-week digits are incremented by 1 when carried to 1-day digits.
3) Day-of-the-week digit display (incremented in septimal notation):
   (W4W2W1)=(000)→ (001)→ - - - - - - → (110) → (000)
   The relation between days of the week and day-of-the-week digits is user changeable (e.g. Sunday=000).
4) The (W4W2W1) should not be set to (111).

3.3 Calendar Counter (at 8h to Dh)

D3	D2	D1	D0		
D_8	D_4	D_2	D_1	(read and write cycle) 1-day calendar digit	(at 8h)
*	*	D_{20}	D_{10}	(read and write cycle) 10-day calendar digit	(at 9h)
MO_8	MO_4	MO_2	MO_1	(read and write cycle) 1-month calendar digit	(at Ah)
*	*	*	MO_{10}	(read and write cycle) 10-month calendar digit	(at Bh)
Y_8	Y_4	Y_2	Y_1	(read and write cycle) 1-year calendar digit	(at Ch)
Y_{80}	Y_{40}	Y_{20}	Y_{10}	(read and write cycle) 10-year calendar digit	(at Dh)

1) The "*" mark in the above table indicates data which are set to 0 for read cycle and not set for write cycle.
2) The automatic calendar function provides the following calendar digit displays in BCD code:
   - Day digits: Range from 1 to 31 (for January, March, May, July, August, October, and December).
     Range from 1 to 30 (for April, June, September, and November).
     Range from 1 to 29 (for February in leap years).
     Range from 1 to 28 (for February in ordinary years).
     Carried to month digits when cycled to 1.
   - Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
   - Year digits: Range from 00 to 99 and counted as 00, 04, 08, - - - -- -, 92, and 96 in leap years.
3) Any registered imaginary time should be replaced with actual time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter to malfunction.

USAGES

1. Read Data

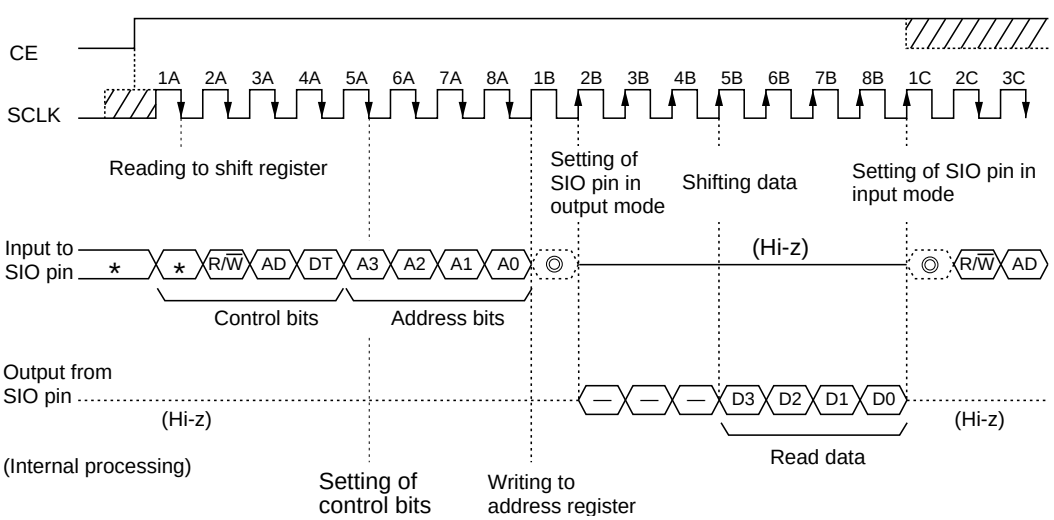
The real-time clock becomes accessible by switching the CE pin from the low level to high level to enable interfacing with the CPU and then inputting setting data (control bits and address bits) to the SIO pin in synchronization with shift clock pulses from the SCLK pin.

The input data are registered in synchronization with the falling edge of the SCLK. When the data is read, the read cycle shall be set by control bits.

- Control bits
  - R/$\overline{W}$: Establishes the read mode when set to 1, and the write mode when set to 0.
  - AD: Writes succeeding address bits (A3 to A0) to the address register when set to 1 with the DT bit set to 0 and performs no such write operation in any other case.
  - DT: Writes data bits (D3 to D0) to the counter or register specified by the address register which has written just before when set to 1 with the R/$\overline{W}$ and AD bits set equally to 0 and performs no such write operation in any other case.
- Address bits
  - A3 to A0: Inputs the bits MSB to LSB in the address table describing the functions.

1.1 Read Cycle Flow

1. The CE pin is switched from the low level to the high level.
2. Four control bits (with the first bit ignored) and four read address bits are input from the SIO pin. At this time, control bits R/$\overline{W}$ and AD are set equally to 1 while a control bit DT is set to 0.
3. The SIO pin enters the output mode at the rising edge of the shift clock pulse 2B from the SCLK pin while the four read bits (MSB→LSB) at designated addresses are output at the rising edge of the shift clock pulse 5B (see the figure below).
4. Then, the SIO pin returns to the input mode at the rising edge of the shift clock pulse 1C. Afterwards control bits and address bits are input at the shift clock pulses 1C in the same manner as at the shift clock pulse 1A.
5. At the end of read cycle, the CE pin is switched from the high level to the low level (after t_{CEH} from the falling edge of the eighth shift clock pulse from the SCLK pin). (Following on read cycle, write operation can be performed by setting control bits in the write mode at the shift clock pulse 1C and later with the CE pin held at the high level.)



) In the above figure, the ""mark indicates arbitrary data; the "—" mark indicates unknown data; the "◎" mark indicates data which are available when the SIO pin is held at the high, low, or Hiz level ; and the diagonaliy shaded area indicates high or low.

2. Write Data

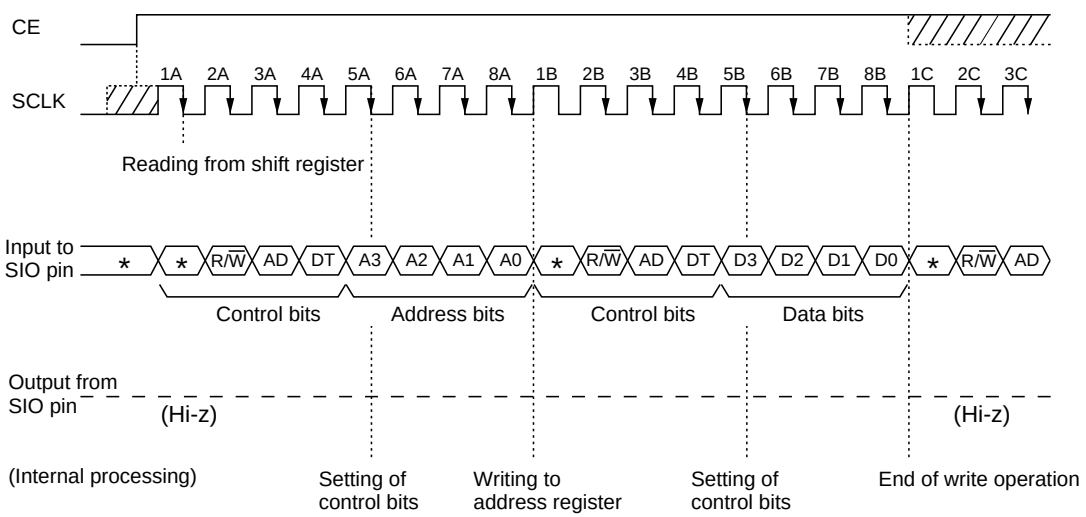
Writing data to the real-time clock requires inputting setting data (control bits and address bits) to the SIO pin and then establishing the write mode by using a control bit R/$\overline{W}$ in the same manner as in read operation.

*) Control bits and address bits are described in the previous section on read cycle.

- Data bits D3 to D0 : inputs writing data to the counter or the register describing the functions in order of MSB to LSB.

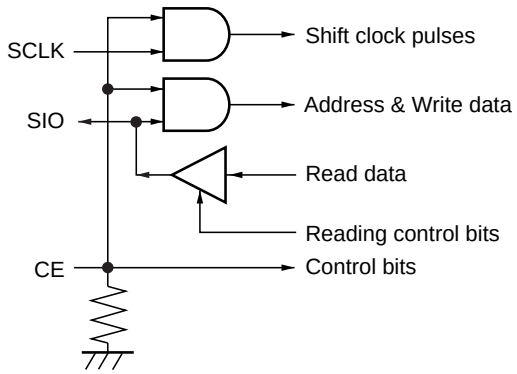
2.1 Write Cycle Flow

1. The CE pin is switched from the low level to the high level.
2. Four control bits (with the first bit ignored) and four write address bits are input from the SIO pin. At this time, control bits R/$\overline{W}$ and DT are set equally to 0 while a control bit AD is set to 1 (at the shift clock pulses 1A to 8A from the SCLK pin).
3. Four control bits and four bits of data to be written are input in the descending order of their significance. At this time, control bits R/$\overline{W}$ and AD are set equally to 0 while a control bit DT is set to 1 (at the shift clock pulses 1B to 8B from the SCLK pin).
4. When write cycle is continued, control bits and address bits are input at the shift clock pulse 1C and later in the same manner as at the shift clock pulse 1A.
5. At the end of write operation, control bits R/$\overline{W}$, AD, and DT are set equally to 0 (at the falling edge of the fifth shift clock pulse and later from the SCLK pin) or the CE pin is switched from the high level to the low level (after t_{CEH} from the falling edge of the eighth shift clock pulse from the SCLK pin).



) In the above figure, the "" mark indicates arbitrary data; and the diagonally shaded area indicates the high or low level.

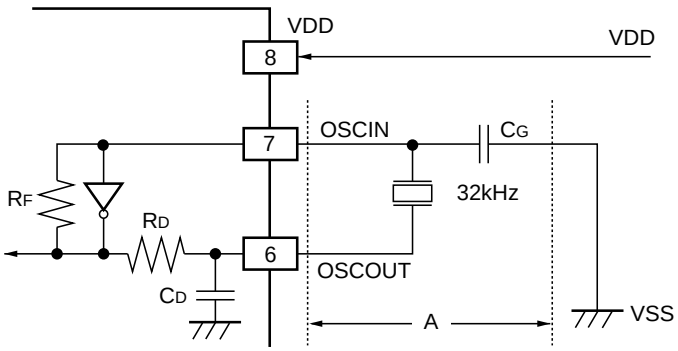
3. CE Pin



1) Switching the CE pin to the high level enables both the SCLK and SIO pins, allowing data to be serially read from and written to the SIO pin in synchronization with shift clock pulses input from the SCLK pin.
2) Switching the CE pin to the low level or opening it disables both the SCLK and SIO pins, causing high impedance and resetting the internal interfacing circuits such as the shift register.
3) The CE pin should be held at the low level or open state when no access is made to the RS5C313. The CE pin incorporates a pull-down resistor.
4) During system power-down (being back-up battery powered), the low-level input of the CE pin should be brought as close as possible to the VSS level to minimize the loss of charge in the battery.
5) Holding the CE pin at the high level for more than 2.5 seconds mainly forces 1Hz interrupt pulses to be output from the $\overline{\text{INTR}}$ pin for oscillation frequency measurement. When the CE pin is held at the high level for less than 1.5 seconds, no pulse is output.
6) The CE pin should be held at the low level in order to enable oscillator halt sensing. Holding the CE pin at the high level, therefore, disables oscillator halt sensing, retaining the value of the XSTP (oscillator halt sensing) bit which exists immediately before the CE pin is switched to the high level.

Considerations
When the power turns on from 0V, the CE pin should be set low or open once.

4. Configuration of Oscillating Circuit



Typical external device:
X'tal : 32.768kHz
(R_1=30kΩ)
(C_L=6pF to 8pF)
C_G=8pF to 20pF

Standard values of internal devices:
R_F=15MΩ (TYP.)
R_D=60kΩ (TYP.)
C_D=10pF (TYP.)

The oscillation circuit is driven at a constant voltage of about 1.5 V relative to the V_{SS} level. Consequently, it generates a waveform having a peak-to-peak amplitude of about 1.5 V on the positive side of the V_{SS} level.

Considerations in Mounting Components Surrounding Oscillating Circuit

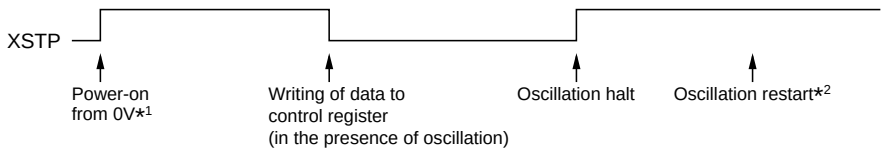
1) Mount the crystal oscillators and C_G in the closest possible position to the IC.
2) Avoid laying any signal or power line close to the oscillation circuit (particularly in the area marked with "←A →" in the above figure).
3) Apply the highest possible insulation resistance between the OSCIN or OSCOUT pin and the PCB.
4) Avoid using any long parallel line to wire the OSCIN or OSCOUT pin.
5) Take extreme care not to cause condensation, which leads to various problems such as oscillation halt.

Other Relevant Considerations

1) When applying an external input of clock pulses (32.768 kHz) to the OSCIN pin:
   DC coupling - - - - - Prohibited due to mismatching input levels.
   AC coupling - - - - - Permissible except that unpredictable results may occur in oscillator halt sensing due to possible sensing errors caused by noises, etc.
2) Avoid using the oscillator output of the RS5C313 (from the OSCOUT pin) to drive any other IC for the purpose of ensuring stable oscillation.

5. Oscillator Halt Sensing

Oscillation Halt can be sensed by setting the XSTP (oscillator halt sensing) bit to 0 (after writing data to the control register) and then monitoring the XSTP bit. Upon oscillator halt sensing, the XSTP bit is switched from 0 to 1. This function can be applied to judge clock data validity.



*1) While the CE pin is held at the low level the XSTP bit is set to 1 upon power-on from 0 V. Note that any instantaneous power disconnection may cause operational failure. When the CE pin is held at the high level oscillation halt is not sensed and the value of the XSTP bit when the CE pin is held at the low level is retained.

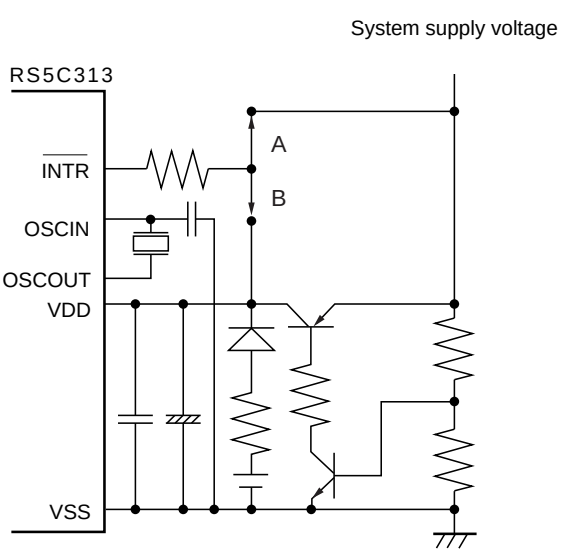
*2) Once oscillation halt has been sensed, the XSTP bit is held at 1 even if oscillation is restarted.

Considerations in Use of XSTP Bit

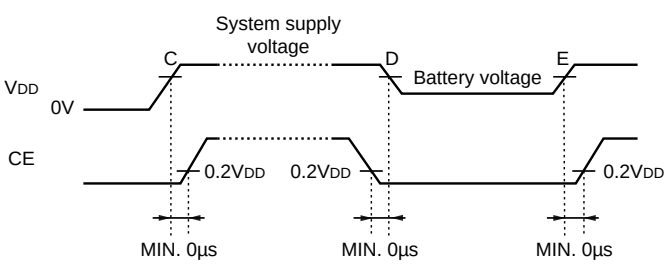
Ensure error-free oscillation halt sensing by preventing the following:

1) Instantaneous disconnection of V_{DD}
2) Condensation on the crystal oscillator
3) Generation of noise on the PCB in the crystal oscillator
4) Application of voltage exceeding prescribed maximum ratings to the individual pins of the IC

6. Typical Power Supply Circuit



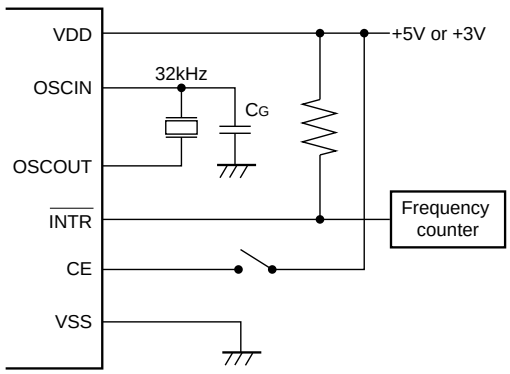
1) Connect the capacitance of the oscillation circuit to the VSS pin.
2) Mount the high- and low-frequency by-pass capacitors in parallel and very close to the RS5C313.
3) Connect the pull-up resistor of the $\overline{INTR}$ pin to two different positions depending on whether the resistor is in use during battery back-up.
   - When not in use during battery back-up
     ----- Position A in the left figure
   - When in use during battery back-up
     ----- Position B in the left figure
4) Timing of power supply on / off and CE terminal refer to lower part plan.



C,D,E : The lower limit voltage for CPU operation

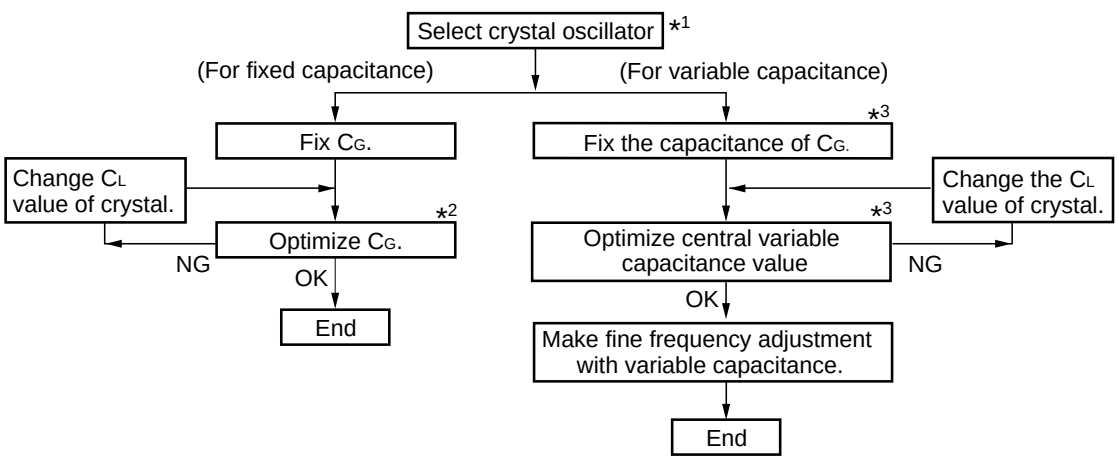
7. Oscillation Frequency Adjustment

7.1 Oscillation Frequency Measurement



1) When switch the CE pin to the high level after low level or open state, a 1-Hz interrupt pulse is output from the $\overline{INTR}$ pin about 2.5 seconds later. Measure this interrupt pulse by using a frequency counter
2) Ensure that the frequency counter has more than six digits (on the order of 1 ppm).
3) Place the C_G between the OSCIN pin and the V_{SS} level and pull up the $\overline{INTR}$ pin output to the V_{DD} .

7.2 Oscillation Frequency Adjustment



*1) To ensure that the crystal is matched to the IC, inquire its crystal supplier about its C_L (load capacitance) and R1 (equivalent series resistance) values. It is recommended that the crystal should have the C_L value range of 6 to 8pF and the typical R1 value of 30k ohms.

*2) To allow for the possible effects of floating capacitance, select the optimum capacitance of the C_G on the mounted PCB. The standard and recommendable capacitance values of the C_G range from 5 to 24pF and 8 to 20pF, respectively. When you need to change the frequency to get higher accuracy, change the C_L value of the crystal.

*3) Collate the central variable capacitance value of the C_G with its oscillation frequency by adjusting the angle of rotation of the variable capacitance of the C_G in such a manner that the actual variable capacitance value is slightly smaller than the central variable capacitance value. (It is recommended that the central variable capacitance value should be slightly less than one half of the actual variable capacitance value because the smaller is variable capacitance, the greater are fluctuations in oscillation frequency.) In the case of an excessive deviation of the oscillation frequency from its required value, change the C_L value of the crystal.

After adjustment, oscillation frequency is subject to fluctuations of an ambient temperature and supply voltage.
See "10. Typical Characteristic Measurements".

Note

Any rise or fall in ambient temperature from its reference value ranging from 20 to 25 degrees Celsius causes a time delay for a 32kHz crystal oscillator. It is recommendable, therefore, to set slightly high oscillation frequency at room temperature.

8. Interrupt Operation

The $\overline{\text{INTR}}$ pin output, the interrupt cycle register, and the CTFG bit can be used to interrupt the CPU in a certain cycle. (The $\overline{\text{INTR}}$ pin functions as an Nch open drain output.)

8.1 Selection of Interrupt Cycle

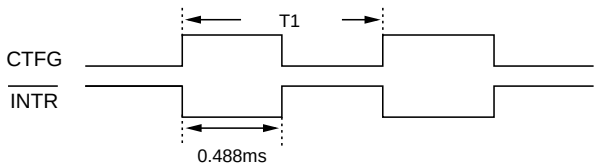
The interrupt cycle register can be used to select either one of two interrupt output modes: the pulse mode (when the CT_3 bit is set to 0) and the level mode (when the CT_3 bit is set to 1).

Interrupt cycle register				$\overline{\text{INTR}}$ pin output	Remarks
CT_3	CT_2	CT_1	CT_0		
0	*[*1]	0	0	OFF	Interrupt halt
0	*	0	1	ON	Fixing the $\overline{\text{INTR}}$ pin at the low level
0	*	1	0	0.977ms	Cycle: 0.977ms (1/1024Hz) Duty: 50%
0	*	1	1	0.5s	Cycle: 0.5s (1/2Hz)
1	0	0	0	1 second	Every second
1	0	0	1	10 seconds	Every 10 seconds (For display of second digits: 00, 10, 20, 30, 40, and 50)
1	0	1	0	1 minute	Every minute (00 second)
1	0	1	1	10 minutes	Every 10 minutes (00 second) (For display of minute digits: 00, 10, 20, 30, 40, and 50)
1	1	0	0	1 hour	Every hour (00 minute and 00 second)
1	1	0	1	1 day	Every day (0 hour, 00 minute, and 00 second a.m.)
1	1	1	0	1 week	Every week (0 week, 0 hour, 00 minute, and 00 second a.m.)
1	1	1	1	1 month	Every month (1st day, 0 hour, 00 minute, and 00 second a.m.)

1) The symbol "" in the above table indicates 0 or 1.

8.2 Pulse Mode Interrupt

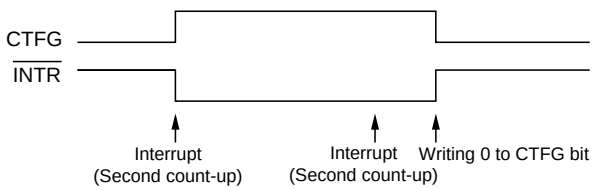
When the CT3 bit is set to 0 and provides four interrupt cycles, off, on, 1024 Hz, and 2 Hz can be selected. The CTFG bit cannot be set because it is used for output monitoring.



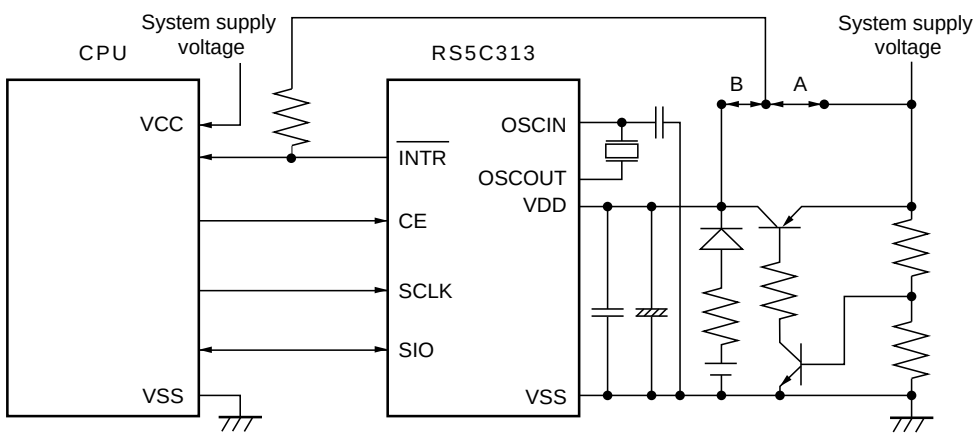
1024Hz : T1=0.977ms
2Hz : T1=500ms

8.3 Level Mode Interrupt

When the CT3 bit is set to 1, clock-interlocked cycles in increments of 1 second to 1 month can be selected. The CTFG bit can be written; writing the CTFG bit switches the $\overline{\text{INTR}}$ pin to the low level while writing 0 to the CTFG bit turns off the $\overline{\text{INTR}}$ pin.

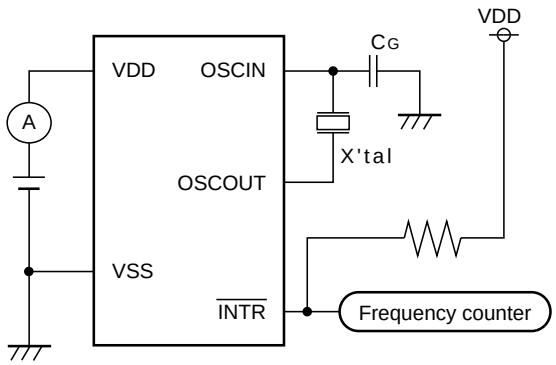


9. Typical Application



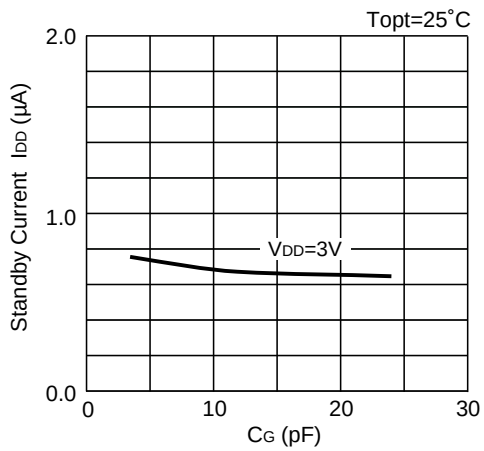
1) Connect the capacitance of the oscillation circuit to the VSS pin.
2) Mount the high- and low-frequency by-pass capacitors in parallel and very close to the RS5C313.
3) Connect the pull-up resistor of the $\overline{\text{INTR}}$ pin to two different positions depending on whether the resistor is in use during battery back-up.
   When not in use during battery back-up - - - - - Position A in the above figure
   When in use during battery back-up - - - - - -- Position B in the above figure

10. Typical Characteristic Measurements

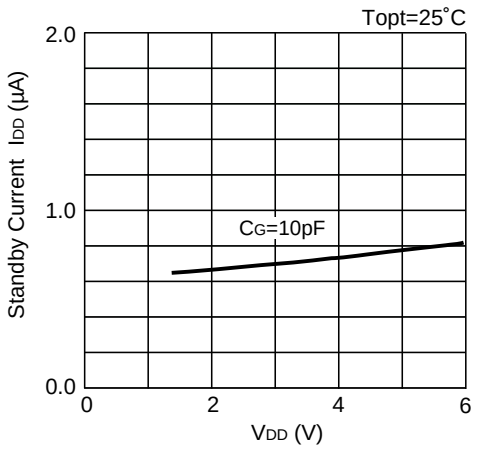


C_G=10pF
X'tal : R_1=30kΩ, C_L=6pF
T_{opt}=25˚C
Input pin : V_{DD} or V_{SS}
Output pin : Open

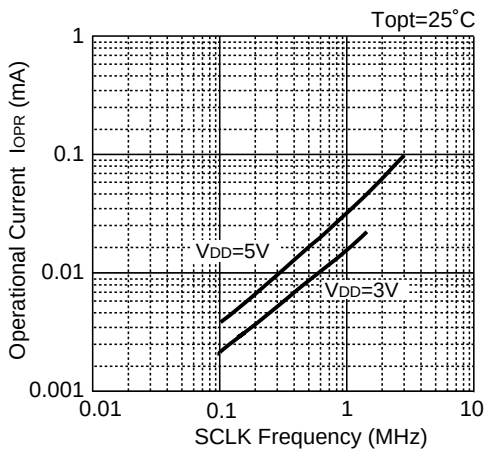
10.1 Standby Current vs. C_G (V_{DD}=3V)



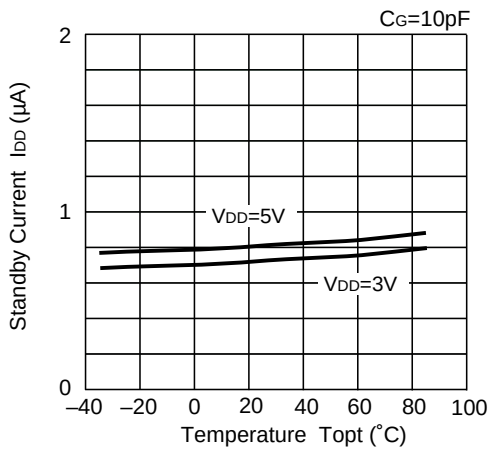
10.2 Standby Current vs. V_{DD}(C_G=10pF)



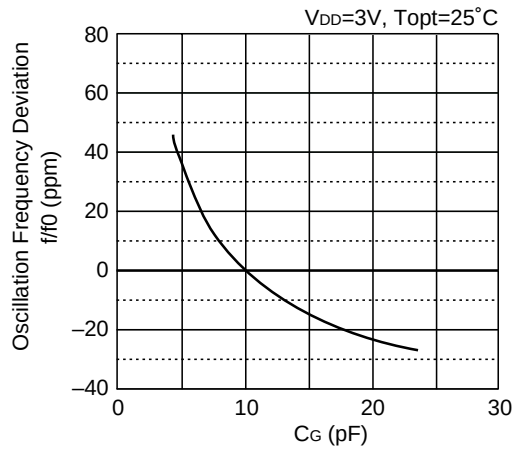
10.3 Operational Current vs. SCLK Frequency



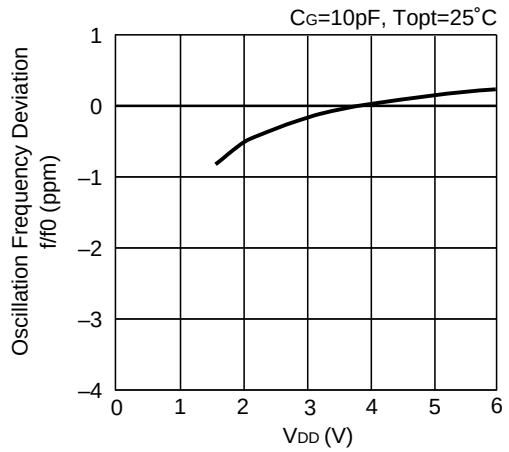
10.4 Standby Current vs. Temperature (V_{DD}=3V, 5V)



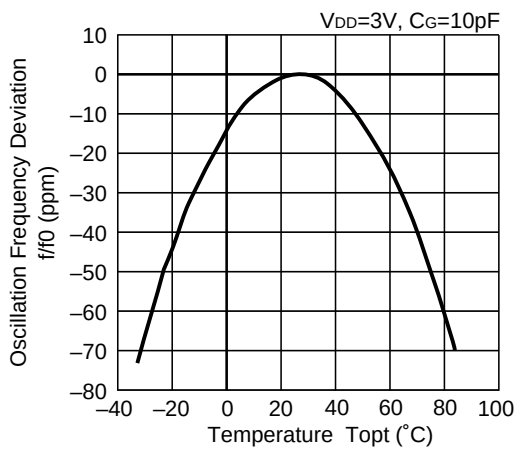
10.5 Oscillation Frequency Deviation vs. C_G (f0: C_G=10pF reference)



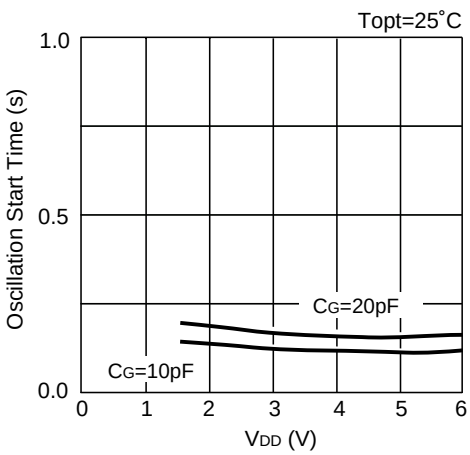
10.6 Oscillation Frequency Deviation vs. V_{DD} (f0: V_{DD}=4V reference)



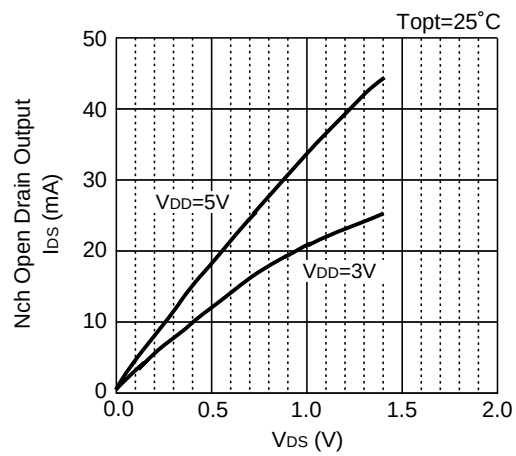
10.7 Oscillation Frequency Deviation vs. Temperature (f0: Topt=25˚C reference)



10.8 Oscillation Start Time vs. V_{DD}

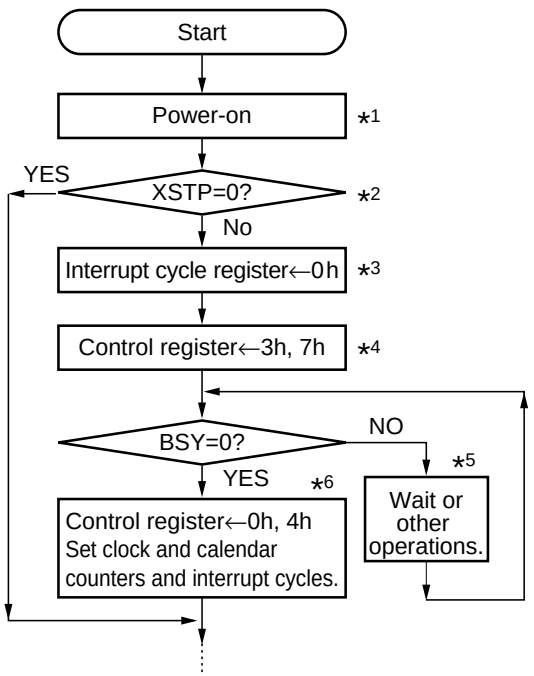


10.9 V_{DS} vs. I_{DS} for Nch Open Drain Output



11. Typical Software-based Operations

11.1 Initialization upon Power-on



*1) Switch the CE pin to the low level immediately after power-on.

*2) When not making oscillation halt sensing (data validity), the XSTP bit need not be checked.

*3) Turn off the $\overline{INTR}$ pin, whose output is uncertain at power-on.

*4) Write to control register 3h for 12-hour format or 7h for 24-hour format. Set the ADJ bit to 1 for checking oscillaiton.

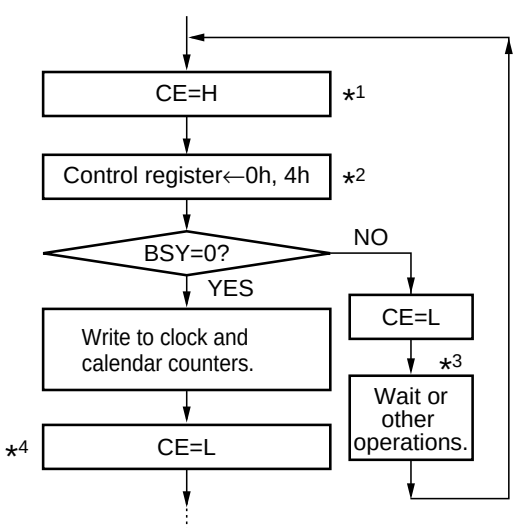
*5) It takes 0.1-2 seconds to be set the BSY bit to 0 from oscillation starting upon power-on from 0V. Provide an exit from an oscillation start loop to prepare for oscillation failure.

*6) Set the XSTP bit to 0 by writing data to the control register.
0h for the 12-hour time display system.
4h for the 24-hour time display system.

When using the XSTP bit

Ensure stable oscillation by preventing the following:
1) Condensation on the crystal oscillator
2) Instantaneous disconnection of power
3) Generation of clock noises, etc. in the crystal oscillator
4) Charge of voltage exceeding prescribed maximum ratings to the individual pins of the IC

11.2 Write Operation to Clock and Calendar Counters



*1) After switching the CE pin to the high level, hold it at the high level until any subsequent operation requires switching it to the low level. (Note that switching the CE pin to the low level sets the WTEN bit to 1.)

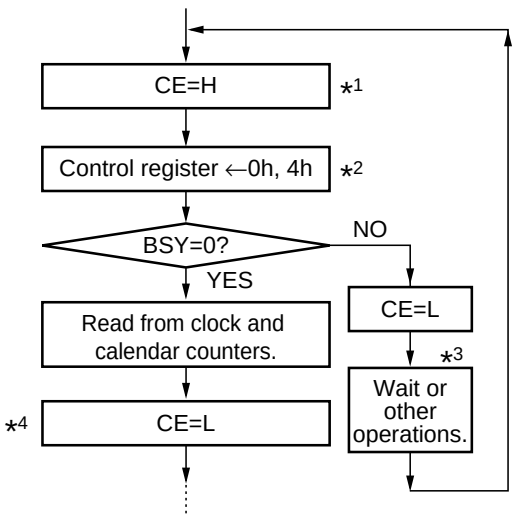
*2) Write 0h for the 12-hour format or 4h for the 24-hour time display system.

*3) The BSY bit is held at 1 for a maximum duration of 122.1 us.

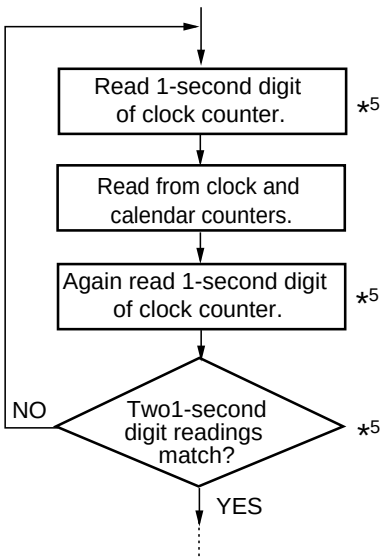
*4) Switch the CE pin to the low level to set the WTEN bit to 1.
During write operation to the clock and calendar counters, one 1-second digit carry causes a 1-second increment while two 1-second digit carries also cause only a 1-second increment, which, in turn, causes a time delay.

11.3 Read Operation from Clock and Calendar Counters

11.3-1



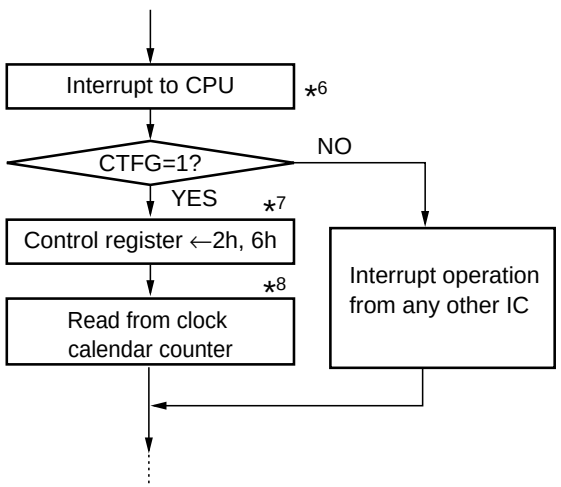
11.3-2



Note

Read data as described in 11.3-2 or 11.3-3 when it takes (1/1024) sec or more to set the WTEN bit from 0 to 1 (CE=L), the read operation described in 11.3-1 is prohibited as such a case.

11.3-3



*1) After switching the CE pin to the high level, hold it at the high level until any subsequent operation requires switching it to the low level. (Note that switching the CE pin to the low level sets the WTEN bit to 1.)

*2) Write 0h for the 12-hour format or 4h for the 24-hour time display system.

*3) The BSY bit is held at 1 for a maximum duration of 122.1 us.

*4) Switch the CE pin to the low level to set the WTEN bit to 1.
During write operation to the clock and calendar counters, one 1-second digit carry causes a 1-second increment while two 1-second digit carries also cause only a 1-second increment, which, in turn, causes a time delay.

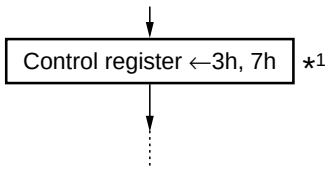
*5) When needing any higher-order digits than the minute digits, replace second digits with minute digits. (Reading LSD one of the required digits twice.)

*6) Select the level mode as an interrupt mode by setting the CT3 bit to 1.

*7) Write 2h for the 12-hour format or 6h for the 24-hour format.

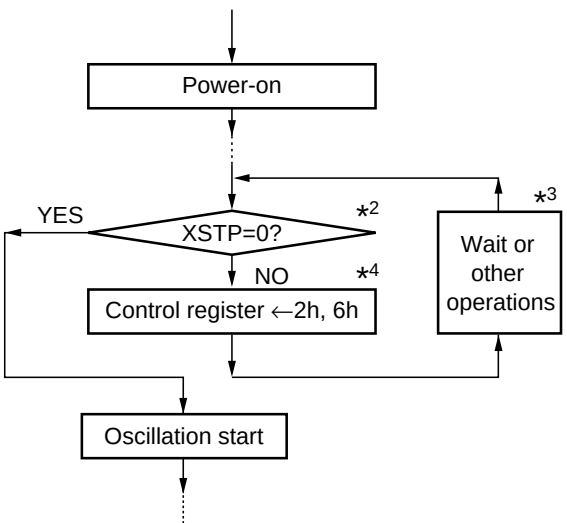
*8) Complete read operation within an interrupt cycle after interrupt generation (e.g. within 1 second).

11.4 Second-digit Adjustment by ±30 seconds



*1) Write 3h for the 12-hour format or 7h for the 24-hour format and then set the ADJ bit to 1. (The BSY bit is held at 1 for a maximum duration of 122.1µs after the ADJ bit is set to 1.)

11.5 Oscillation Start Judgment



*2) The XSTP bit is set to 1 upon power-on from 0V.

*3) It takes approximately 0.1 to 2 seconds to start oscillation.
Provide an exit from an oscillation start loop to prepare for oscillation failure.

*4) Write 2h for the 12-hour format or 6h for the 24-hour format.

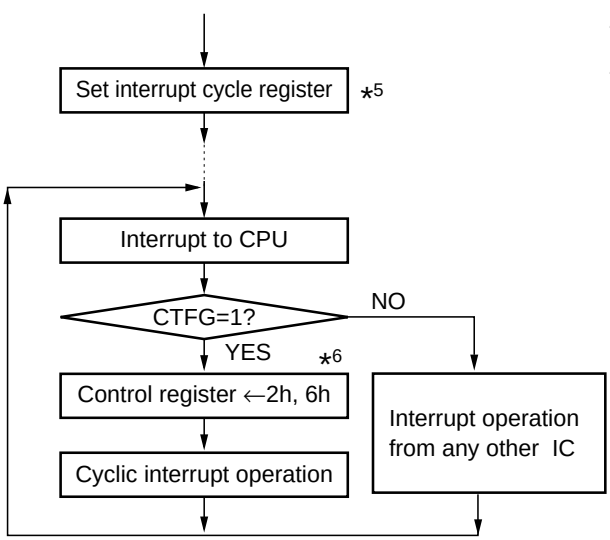
When using the XSTP bit

Ensure stable oscillation by preventing the following:

1) Condensation on the crystal oscillator
2) Instantaneous disconnection of power
3) Generation of clock noises, etc. in the crystal oscillator
4) Charge of voltage exceeding prescribed maximum ratings to the individual pins of the IC

11.6 Interrupt Operation

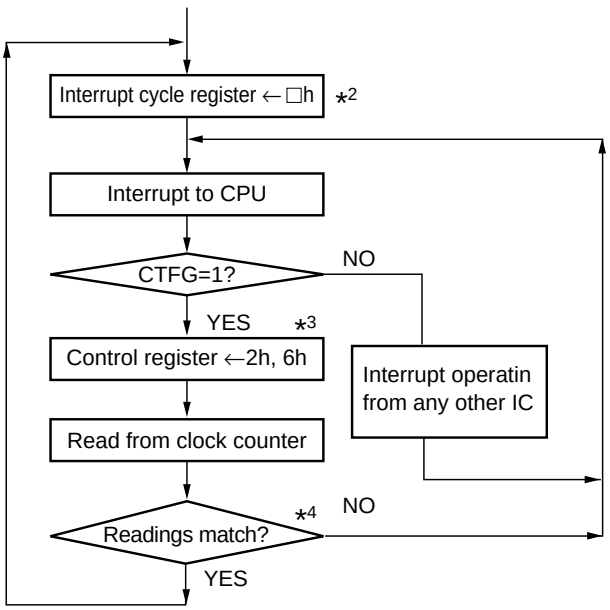
(a) Cyclic Interrupt Operation (Every 1 Second to 1 Month)



*5) Set the interrupt cycle register to the level mode by setting the CT3 bit to 1.

*6) Write 2h for the 12-hour format or 6h for the 24-hour format.

(b) Daily Time (Hour or Minute) Alarm Operation*1



*1) In this typical operation, alarm time is stored in the CPU and collated with clock time through interrupt operation.

*2) Initially set address □h to Ch (every 1 hour) and change it in the following sequence for every matching of clock counter readings in

Ch → Bh → Ah → (9h → 8h)
Every Every Every (Every Every)
1 hour 10 mins. 1 min. (10 secs. 1 sec.)

In this manner, change the settings of the interrupt cycle register.

*3) Write 2h for the 12-hour format or 6h for the 24-hour format.

*4) Collate alarm time with clock time through interrupt operation.

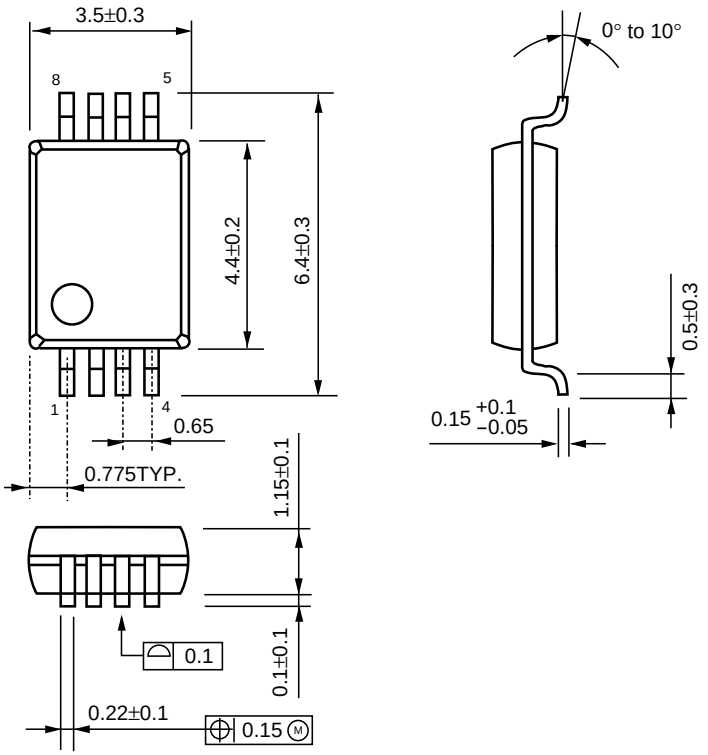
Interrupt Setting	Time Digit for Collation
Ch	10-hour and 1-hour digits
Bh	10-minute digit (10-hour and 1-hour digits)
Ah	1-minute digit (10-hour, 1-hour, and 10-minute digits)
(9h)	10-second digit (10-hour digit to 1-minute digit)
(8h)	1-second digit (10-hour digit to 10-second digit)

Note

In the above typical operation, alarm time (hour and minute) is collated with clock time by making interrupt operation a maximum of 37 times per day as shown by the following calculation:
23(1-hour digit)+5(10-minute digit)+9(1-minute digit)=37 times
In this connection, a total current consumption increase resulting from interrupt operation can also be calculated as follows:
Assuming, for example, that interrupt operation to the CPU takes 50 ms and consumes 10mA of current, an average current consumption increase resulting from interrupt operation can be calculated as follows: (50 ms×10mA×37 times) / (60 seconds×60 minutes×24 hours)=0.21µA Counting in a standard current consumption of about 0.91µA when the RS5C313 is set to 3V, a total current consumption can be calculated at about 1.1µA.

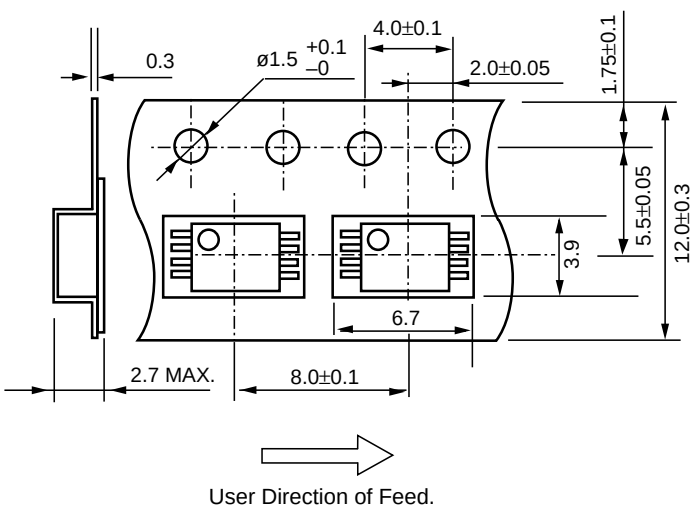
PACKAGE DIMENSIONS (Unit:mm)

• 8pin SSOP (0.65mm pitch)



TAPING SPECIFICATION (Unit:mm)

The RS5C313 has one designated taping direction. The product designation for the taping components is "RS5C313-E2".



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