

OVERVIEW

The SM5852FS is a digital signal processor IC that performs DDBB (digital dynamic bass boost) processing for use in digital audio reproduction equipment. It is designed for use with a 44.1 kHz sampling frequency.

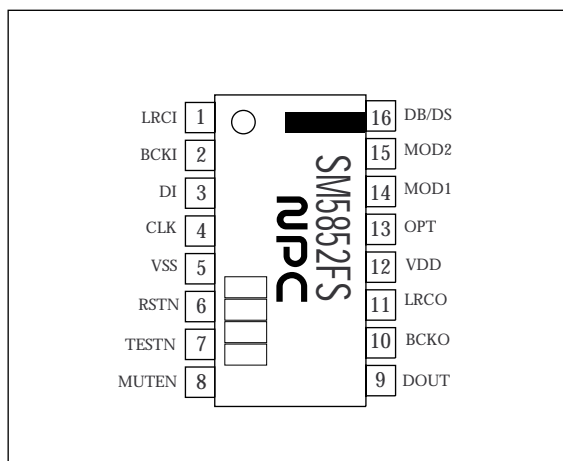
FEATURES

- 2-channel processing
- Improved DDBB mode channel separation
- 6 input-level dependent dynamic gain characteristics
- Serial input/output interface
2s complement, MSB first, 16-bit
- 384fs system clock
- 23 × 23-bit multiplier/30-bit high-precision accumulator
- TTL-compatible input/output
- 3.2 to 5.5 V operating voltage range
- 16-pin SOP
- Molybdenum-gate CMOS

ORDERING INFORMATION

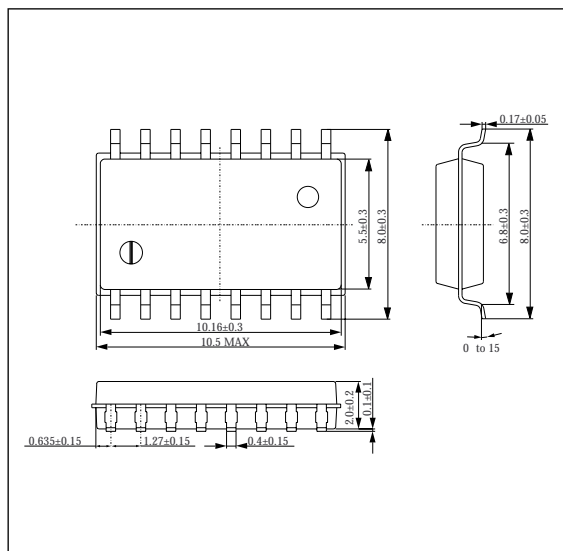
Device	Package
SM5852FS	16pin SOP

PINOUT

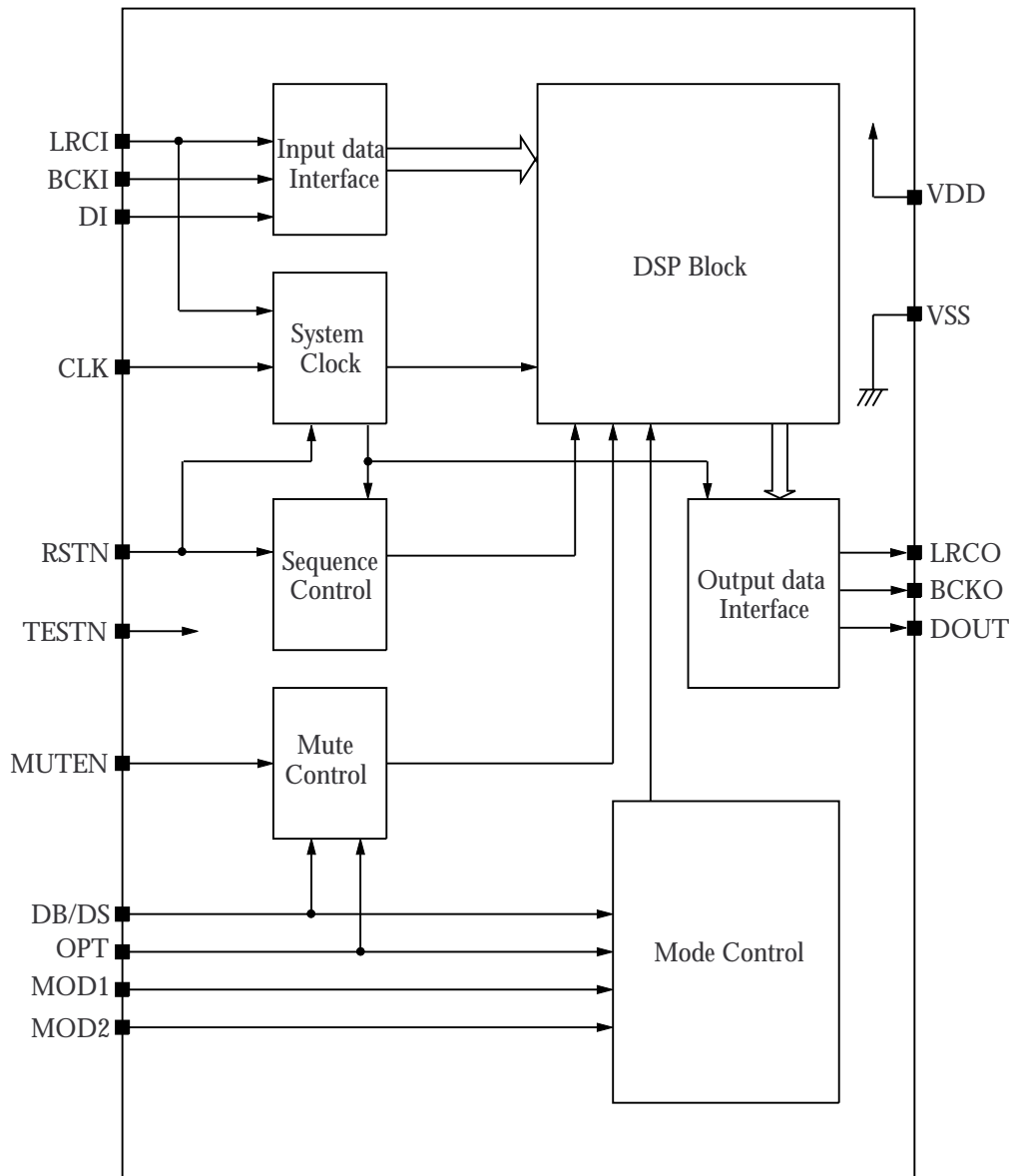


PACKAGE DIMENSIONS

16-pin SOP (Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O ¹	Description			
1	LRCI	Ip	Input data sample rate (fs) clock input			
2	BCKI	Ip	Bit clock input			
3	DI	Ip	Serial data input			
4	CLK	I	Clock input			
5	VSS	–	Ground			
6	RSTN	Ip	System reset initialization. Reset when LOW.			
7	TESTN	Ip	Test mode input. Testing when LOW.			
8	MUTEN	Ip	Mute input. Muting when LOW.			
9	DOUT	O	Serial data output			
10	BCKO	O	Bit clock output			
11	LRCO	O	Output data sample rate (fs) clock output			
12	VDD	–	3.2 to 5.5 V supply			
13	OPT	Ip	Not used. Tie HIGH for normal operation.			
14	MOD1	Ip	Gain characteristics switch inputs.			
			MOD1	MOD2	DB/DS	Gain mode
15	MOD2	Ip	LOW	LOW	LOW	18 dB
			LOW	LOW	HIGH	16 dB
16	DB/DS	Ip	LOW	HIGH	LOW	14 dB
			LOW	HIGH	HIGH	12 dB
			HIGH	LOW	LOW	10 dB
			HIGH	LOW	HIGH	6 dB
16	DB/DS	Ip	HIGH	HIGH	LOW	Off
			HIGH	HIGH	HIGH	Off

1. Ip = Input pin with pull-up resistor. Accordingly, they can be left open for HIGH-level input.

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0\text{ V}$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		-0.3 to 7.0	V
Input voltage	V_{IN}		$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Storage temperature	T_{stg}		-55 to 125	°C
Power dissipation	P_D		250	mW
Soldering temperature	T_{sld}		255	°C
Soldering time	t_{sld}		10	s

Recommended Operating Conditions

$V_{SS} = 0\text{ V}$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		3.2 to 5.5	V
Operating temperature	T_{opr}		-40 to 85	°C

DC Characteristics

$V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -40$ to 85 °C for nominal-voltage operation

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption ¹	I_{DD}	$V_{DD} = 5.0$ V	–	16	23	mA
Input voltage for all inputs ²	V_{IH}		2.4	–	–	V
	V_{IL}		–	–	0.5	V
Output voltage for all outputs ³	V_{OH}	$I_{OH} = -0.4$ mA	2.5	–	–	V
	V_{OL}	$I_{OL} = 1.6$ mA	–	–	0.4	V
Input leakage current for all inputs ²	I_{LH}	$V_{IN} = V_{DD}$	–	–	1.0	μA
CLK input leakage current	I_{LL}	$V_{IN} = 0$ V	–	–	1.0	μA
Input current for all inputs except CLK ²	I_{IL}	$V_{IN} = 0$ V	–	–	20	μA

- $f_{CLK} = 384$ fs = 16.9344 MHz, no output load, input data conformance with NPC test pattern
- LRCI, BCKI, DI, RSTN, TESTN, MUTEN, OPT, MOD1, MOD2, DB / DS, CKL
- LRCO, BCKO, DOUT

$V_{DD} = 3.2$ to 4.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 70 °C for low-voltage operation

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption ¹	I_{DD}	$V_{DD} = 3.4$ V	–	7	10	mA
Input voltage for all inputs ²	V_{IH}		2.4	–	–	V
	V_{IL}		–	–	0.5	V
Output voltage for all outputs ³	V_{OH}	$I_{OH} = -0.2$ mA	2.5	–	–	V
	V_{OL}	$I_{OL} = 0.8$ mA	–	–	0.4	V
Input leakage current for all inputs ²	I_{LH}	$V_{IN} = V_{DD}$	–	–	1.0	μA
CLK input leakage current	I_{LL}	$V_{IN} = 0$ V	–	–	1.0	μA
Input current for all inputs except CLK ²	I_{IL}	$V_{IN} = 0$ V	–	–	12	μA

- $f_{CLK} = 384$ fs = 16.9344 MHz, no output load, input data conformance with NPC test pattern
- LRCI, BCKI, DI, RSTN, TESTN, MUTEN, OPT, MOD1, MOD2, DB / DS, CLK
- LRCO, BCKO, DOUT

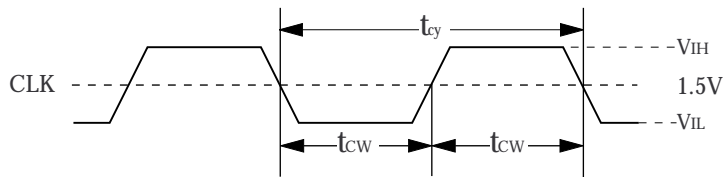
AC Characteristics

$V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -40$ to 85 °C for normal-voltage operation

$V_{DD} = 3.2$ to 4.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 70 °C for low-voltage operation

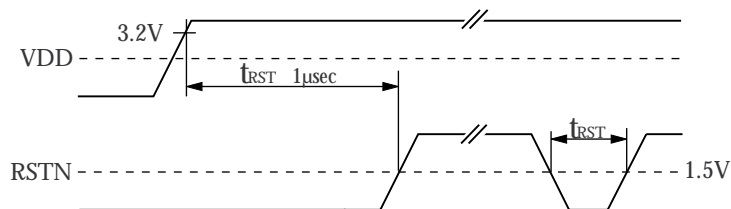
CLK (384fs)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock pulsewidth	t_{CW}		24	-	500	ns
Clock cycle time	t_{CY}		55	59	1000	ns



RSTN

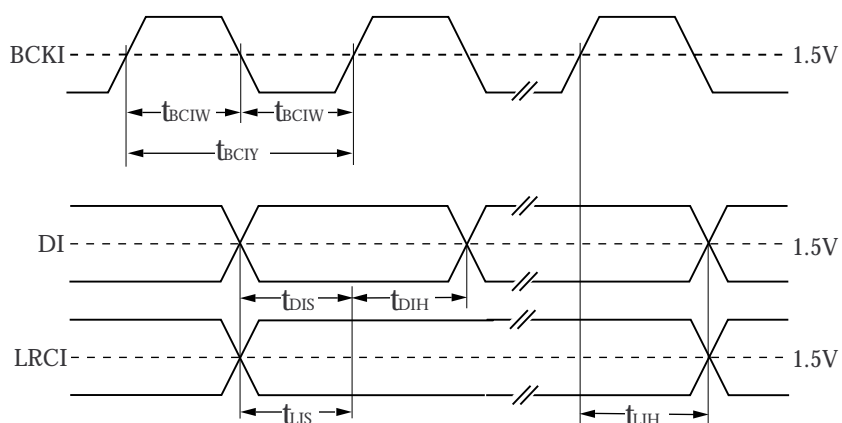
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reset LOW-level pulsewidth	t_{RST}	At power-ON	1	-	-	μ s
		At all other times	50	-	1000	ns



RSTN should be set LOW at power-ON and after reacquiring synchronization. Note that if RSTN is LOW for longer than 1 μ s, a through-current flows in the internal dynamic circuits because the internal clock is stopped. The through-current has no rated value, so the reset pulse should be kept as short as possible at all times other than at power-ON.

Serial input timing

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCKI pulsewidth	t_{BCIW}		100	-	-	ns
BCKI cycle time	t_{BCIY}		200	-	-	ns
DI setup time	t_{DIS}		75	-	-	ns
DI hold time	t_{DIH}		75	-	-	ns
LRCI setup time	t_{LIS}		75	-	-	ns
LRCI hold time	t_{LIH}		75	-	-	ns



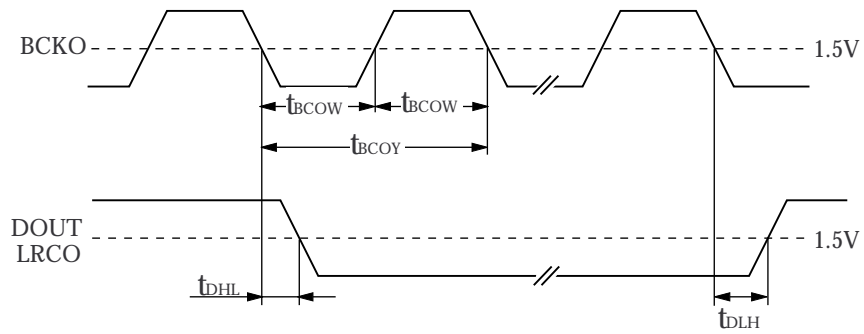
DB/DS, OPT

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Minimum pulsewidth	t_w		$2/f_s$	-	-	ns

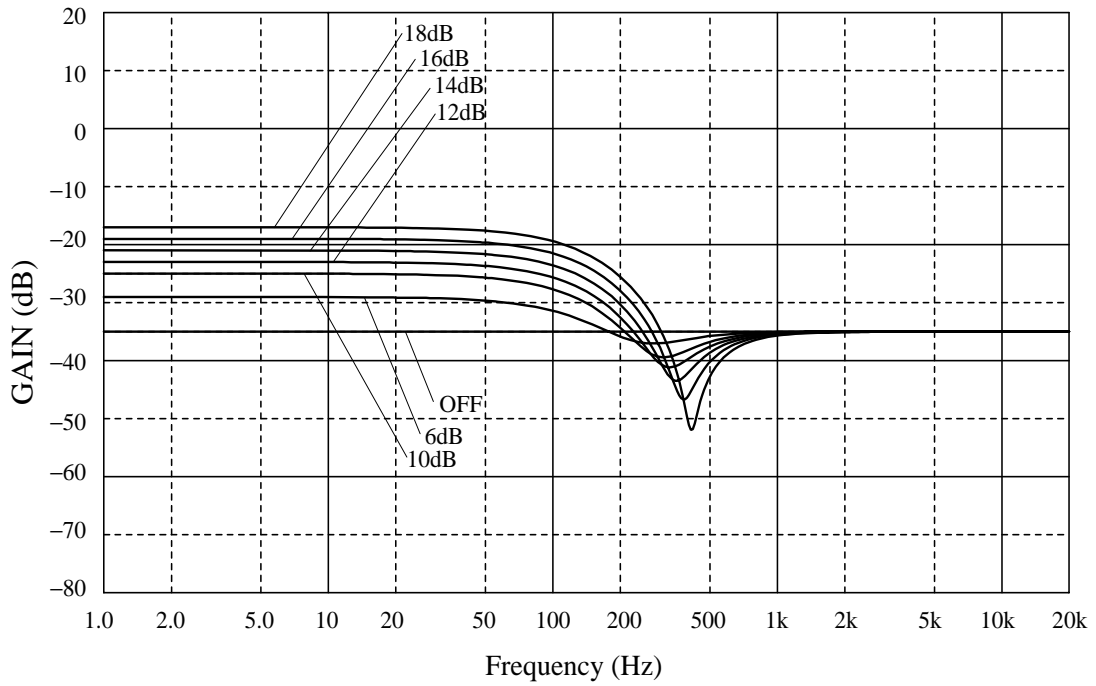
When DB/DS or OPT change state, the input level must be constant for a minimum of $2/f_s$ ($2 \times$ LRCI cycle time). Input levels of duration less than $2/f_s$ may be ignored.

Serial output timing

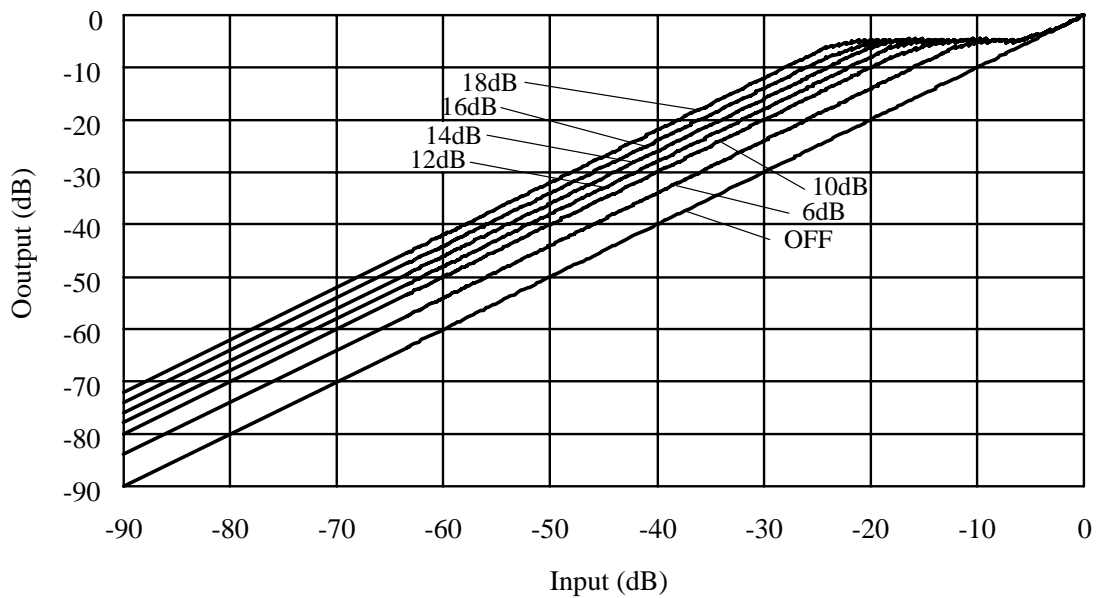
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCKO pulsewidth	t_{BCOW}	15 pF load	180	1/96fs	–	ns
BCKO cycle time	t_{BCOY}	15 pF load	400	1/48fs	–	ns
DOUT, LRCO output delay time	t_{DHL}	15 pF load	–20	–	60	ns
	t_{DLH}	15 pF load	–20	–	60	ns



Low-pass Gain Characteristics



DDBB Mode Filter Characteristics



FUNCTIONAL DESCRIPTION

DDBB (Digital Dynamic Bass Boost)

The DDBB function emphasizes the low-frequency components of the input signal by picking out the low-frequency components and passing them through a DDBB 3rd-order IIR low-pass filter and then changing the gain for the low-frequency components.

Two independent DDBB filters are used, one for each the left and right channels, to maintain full channel separation. The DDBB boost is determined by DB/DS, MOD1 and MOD2.

MOD1	MOD2	DB/DS	Gain mode
LOW	LOW	LOW	18 dB
LOW	LOW	HIGH	16 dB
LOW	HIGH	LOW	14 dB
LOW	HIGH	HIGH	12 dB
HIGH	LOW	LOW	10 dB
HIGH	LOW	HIGH	6 dB
HIGH	HIGH	LOW	Off
HIGH	HIGH	HIGH	Off

Soft Muting

Soft muting is active when MUTEN is LOW. When MUTEN is LOW, the attenuation changes smoothly from 0 to $-\infty$ dB in $1024/f_s$, or approximately 23.2 ms.

When MUTEN goes HIGH, soft muting is released and the attenuation changes smoothly from $-\infty$ to 0 dB, again taking approximately 23.2 ms.

Also, if a MUTEN transition occurs while the attenuation is changing, the attenuation then changes smoothly in the direction specified by the new level of MUTEN.

DB/DS Switching Shock Noise

The soft muting function is also activated to eliminate switching shock noise when DB/DS changes state. When DB/DS changes state, the attenuation changes to $-\infty$ dB, the internal circuit settings are activated and then soft muting is released. Therefore, a maximum time of approximately 46.4 ms is required to change the compression mode. Of course, if the attenuation is already $-\infty$ dB after soft muting using MUTEN, then no time is required to change compression mode.

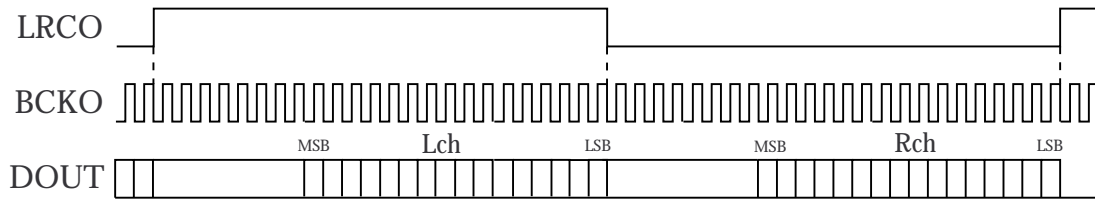
Reset Initialization

RSTN should be set LOW at power-ON and after reacquiring synchronization. Note that if RSTN is LOW for longer than $1\ \mu\text{s}$, a through-current flows in the LSI's internal dynamic circuits because the internal clock is stopped. The through-current has no rated value, so the reset pulse should be kept as short as possible at all times other than at power-ON.

When RSTN goes from LOW to HIGH, initialization hold is released and the initialization routine first resets the internal data over an interval of $4f_s$. During the initialization routine, the output data is forcibly muted so that there is no output signal.

INPUT/OUTPUT TIMING

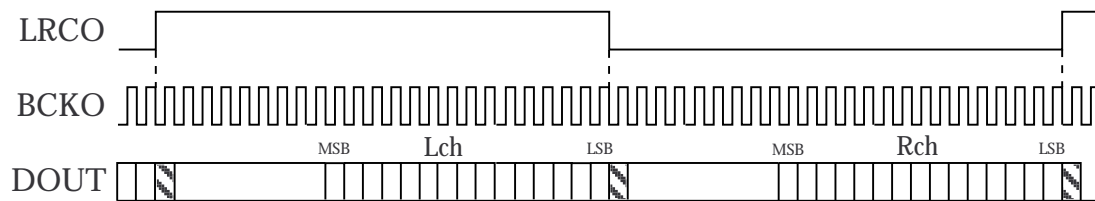
Input Timing



There must be a minimum of 16 BCKI clock cycles to read in a single word of data.

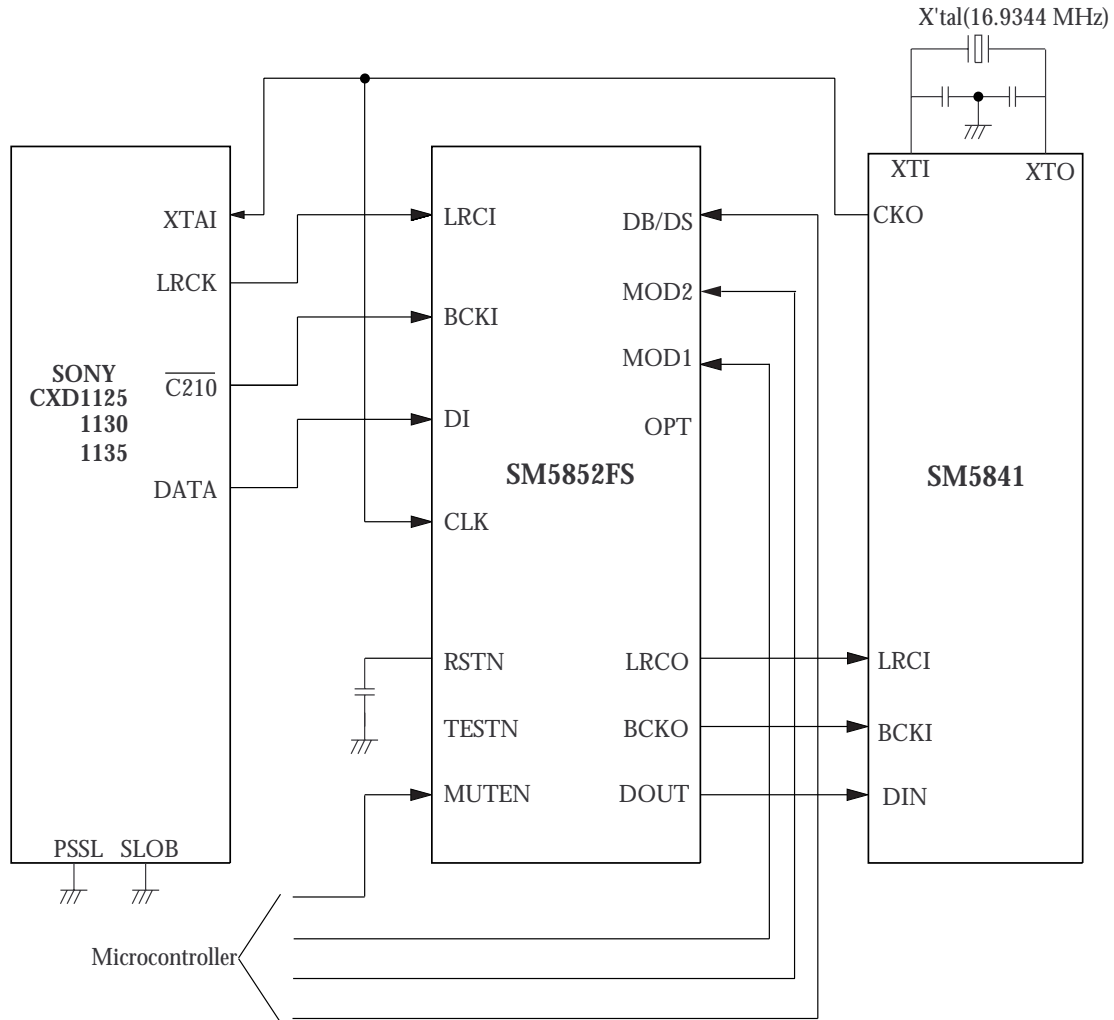
Data on DI is input in sync with the falling edge of BCKI in 16-bit serial, MSB first, 2s complement format.

Output Timing



Shaded areas represent intervals of invalid data.

APPLICATION CIRCUIT



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