

# 8253

Programmable Interval Timer  
iAPX86 Family  
MILITARY INFORMATION

8253

## DISTINCTIVE CHARACTERISTICS

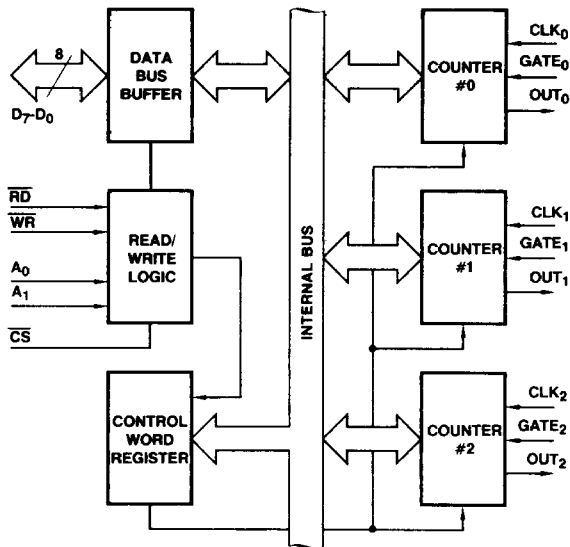
- SMD/DESC qualified
- Both Binary and BCD counting
- Single +5-V supply
- Three independent 16-bit counters
- DC to 5 MHz
- Programmable counter modes
- Bus-oriented I/O

## GENERAL DESCRIPTION

The 8253 is a programmable counter/timer chip designed for use with 8080A/8085A microprocessors. It uses NMOS technology with a single +5-V supply and is a direct replacement for Intel's 8253/8253-5.

Each device is organized as three independent 16-bit counters, each counter having a rate of up to 5 MHz. All modes of operation are software-programmable. For improved performance devices, see the Am9513A System Timing Controller.

## BLOCK DIAGRAM

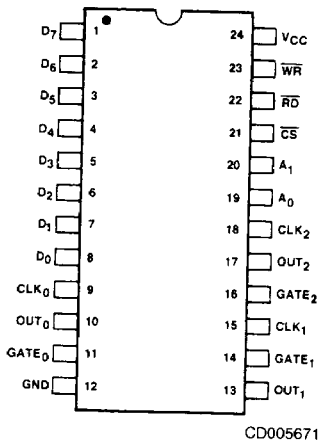


BD003760

Power { +5 V  
Supplies { GND

Publication # 07935 Rev. B Amendment /0  
Issue Date: November 1987

### CONNECTION DIAGRAM Top View



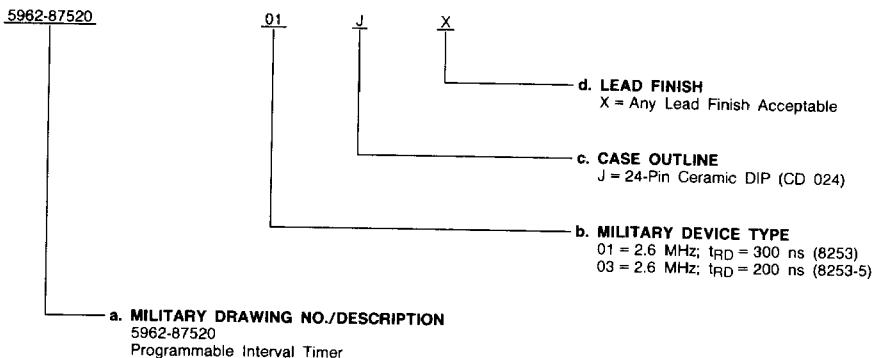
Note: Pin 1 is marked for orientation.

### MILITARY ORDERING INFORMATION

#### Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of:

- a. Military Drawing Part Number
- b. Device Type
- c. Case Outline
- d. Lead Finish



#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
5962-8752001	JX
5962-8752003	

#### Group A Tests

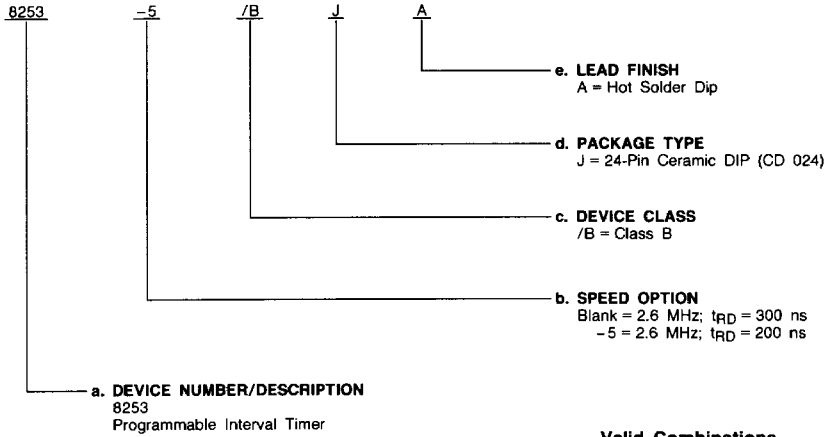
Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

# MILITARY ORDERING INFORMATION (Cont'd.)

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
8253	/BJA
8253-5	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A Tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

### ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65 to +150°C  
 Voltage On Any Pin  
 with Respect to Ground ..... -0.5 to +7.0 V  
 Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

### OPERATING RANGES

Military (M) Devices  
 Temperature (T<sub>C</sub>) ..... -55 to 125°C  
 Supply Voltage (V<sub>CC</sub>) ..... 5 V ±10%  
 Operating ranges define those limits between which the functionality of the device is guaranteed.

### DC CHARACTERISTICS

over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

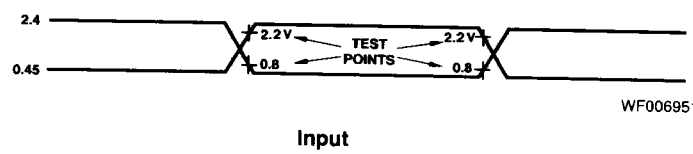
Parameter Symbol	Parameter Description	Test Conditions	8253-5		8253		Unit
			Min.	Max.	Min.	Max.	
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 5 V ±10%	-0.5*	0.7	-0.5*	0.7	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 5 V ±10%	2.4	V <sub>CC</sub> + .5 V*	2.2	V <sub>CC</sub> + .5 V*	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 1.6 mA, V <sub>CC</sub> = 5 V ±10%	0.45		0.45		V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -150 μA, V <sub>CC</sub> = 5 V ±10%	2.4		2.4		V
I <sub>IL</sub>	Input Load Current	V <sub>IN</sub> = V <sub>CC</sub> to 0 V, V <sub>CC</sub> = Max.		±20		±20	μA
I <sub>OFL</sub>	Output Float Leakage	V <sub>OUT</sub> = V <sub>CC</sub> to 0 V, V <sub>CC</sub> = Max.		±20		±20	μA
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	V <sub>CC</sub> = 5 V ±10%, Output Unloaded Static (Note 1)		140		140	mA

### CAPACITANCE T<sub>C</sub> = 25°C, V<sub>CC</sub> = 5 V, GND = 0 V

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
C <sub>IN</sub> †	Input Capacitance	f <sub>c</sub> = 1 MHz			10*	pF
C <sub>I/O</sub> †	I/O Capacitance	Unmeasured pins returned to V <sub>SS</sub>			20*	pF

\*Guaranteed by design; not tested.  
 †Not included in Group A tests.

### SWITCHING TEST WAVEFORM



WF006951

**SWITCHING CHARACTERISTICS** over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 2)

No.	Parameter Symbol	Parameter Description	8253		8253-5		Unit
			Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>							
1	t <sub>AR</sub>	Address Stable Before <u>READ</u>	50		30		ns
2	t <sub>RA</sub>	Address Hold Time for <u>READ</u>	5		5		ns
3	t <sub>RR</sub>	<u>READ</u> Pulse Width	400		300		ns
4	t <sub>RD</sub> (Note 3)	Data Delay from <u>READ</u>		300		200	ns
5	t <sub>DF</sub>	<u>READ</u> to Data Floating	25	105	25	100	ns
6	t <sub>RV</sub>	Recovery Time Between <u>READ</u> and Any Other Control Signal	1		1		μs
<b>WRITE CYCLE</b>							
7	t <sub>AW</sub>	Address Stable Before <u>WRITE</u>	50		30		ns
8	t <sub>WA</sub>	Address Hold Time for <u>WRITE</u>	30		30		ns
9	t <sub>WW</sub>	<u>WRITE</u> Pulse Width	400		300		ns
10	t <sub>DW</sub>	Data Setup Time for <u>WRITE</u>	300		250		ns
11	t <sub>WD</sub>	Data Hold Time for <u>WRITE</u>	40		30		ns
12	t <sub>RV</sub>	Recovery Time Between <u>WRITE</u> and Any Other Control Signal	1		1		μs
<b>CLOCK AND GATE TIMING (Note 2)</b>							
13	t <sub>CLK</sub>	Clock Period	380	DC	380	DC	ns
14	t <sub>PWH</sub>	HIGH Pulse Width	230		230		ns
15	t <sub>PWL</sub>	LOW Pulse Width	150		150		ns
16	t <sub>GW</sub>	Gate Width HIGH	150		150		ns
17	t <sub>GL</sub>	Gate Width LOW	100		100		ns
18	t <sub>GS</sub>	Gate Setup Time to CLK <sub>1</sub>	100		100		ns
19	t <sub>GH</sub>	Gate Hold Time After CLK <sub>1</sub>	55		55		ns
20	t <sub>OD</sub> (Note 3)	Output Delay from CLK <sub>1</sub>		400		400	ns
21	t <sub>ODG</sub> (Note 3)	Output Delay from Gate <sub>1</sub>		300		300	ns

Notes: 1. t<sub>CC</sub> is measured in a static condition with no output loads applied.

2. Test Conditions: V<sub>CC</sub> = 5 V ± 10%  
V<sub>IL</sub> = 0.45 V, V<sub>IH</sub> = 2.4 V  
V<sub>OL</sub> = 0.8 V, V<sub>OH</sub> = 2.2 V  
I<sub>OL</sub> = 1.6 mA, I<sub>OH</sub> = 150 μA

3. Test Condition: C<sub>L</sub> = 100 pF ± 20 pF.