AMENDMENT

Am29030™ and Am29035™

RISC Microprocessors with 8-Kbyte/4-Kbyte Instruction Cache

Advanced Micro Devices

This amendment adds preliminary information on switching characteristics over commercial operating ranges for the 25-MHz Am29030™ microprocessor.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. Valid order numbers are formed by a combination of the elements below.

AM29030 –25 F C /W

SHIPPING OPTION
Blank = For PGA package only
/W = For Cerquad package only:
denotes leads are trimmed/formed

TEMPERATURE RANGE
C = Commercial (T_C = 0°C to +85°C)

PACKAGE TYPE
F = 144-Lead Cerquad (GQD144)
G = 145-Lead Pin Grid Array without Heat Sink (CGY145)

SPEED OPTION
–33 = 33 MHz
–25 = 25 MHz
–20 = 20 MHz
–16 = 16 MHz

DEVICE NUMBER/DESCRIPTION
Am29030 RISC Microprocessor with 8 Kbyte of Instruction Cache
Am29035™ RISC Microprocessor with 4 Kbyte of Instruction Cache

Valid Combinations	
AM29030–33 AM29030–25	GC
AM29030–25 AM29030–20 AM29035–16	FC/W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume. Consult the local AMD sales office to confirm availability of specific valid combinations, and check on newly released combinations.

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SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE (CERQUAD)

No.	Parameter Description	Test Conditions	PRELIMINARY 25 MHz		Unit
			Min	Max	
1	INCLK Period (T)		40	100	ns
2	INCLK High Time		18	82	ns
3	INCLK Low Time		18	82	ns
4	INCLK Rise Time		0	6	ns
5	INCLK Fall Time		0	6	ns
6	MEMCLK Delay from INCLK	Notes 1, 2	0	6	ns
7	Synchronous Output Valid Delay for signals not broken out below	MEMCLK Output MEMCLK Input	1 2	16 20	ns
7a	Synchronous Output Valid Delay for ID31–ID0	MEMCLK Output MEMCLK Input	1 2	18 22	ns
7b	Synchronous Output Valid Delay for $\overline{\text{PGMODE}}$	MEMCLK Output MEMCLK Input	1 2	18 22	ns
8	Synchronous Output Invalid Delay for signals not broken out below	MEMCLK Output MEMCLK Input	1 2	16 20	ns
8a	Synchronous Output Invalid Delay for ID31–ID0	MEMCLK Output MEMCLK Input	1 2	18 22	ns
8b	Synchronous Output Invalid Delay for $\overline{\text{PGMODE}}$	MEMCLK Output MEMCLK Input	1 2	18 22	ns
9	Synchronous Input Setup Time for signals not broken out below (Note 3)	MEMCLK Output MEMCLK Input MEMCLK=INCLK	17 17 12		ns
9a	Synchronous Input Setup Time for ID31–ID0 (Note 3)	MEMCLK Output MEMCLK Input MEMCLK=INCLK	9 9 6		ns
9b	Synchronous Input Setup Time for $\overline{\text{ERR}}$ (Note 3)	MEMCLK Output MEMCLK Input MEMCLK=INCLK	11 11 7		ns
9c	Synchronous Input Setup Time for $\overline{\text{RDN}}$ (Note 3)	MEMCLK Output MEMCLK Input MEMCLK=INCLK	18 18 12		ns
10	Synchronous Input Hold Time	MEMCLK Output MEMCLK=INCLK	0 2		ns
11	Setup Time for Synchronous $\overline{\text{RESET}}$ Deassertion			2	ns
12	Hold Time for Synchronous $\overline{\text{RESET}}$ Deassertion			5	ns
13	$\overline{\text{WARN}}$ Pulse Width		4T		ns
14	Asynchronous Input Pulse Width		T+10		ns
15	MEMCLK High Time	MEMCLK Period=T MEMCLK Period=2T	18 T–3	82 T+3	ns
16	MEMCLK Low Time	MEMCLK Period=T MEMCLK Period=2T	18 T–3	82 T+3	ns
17	MEMCLK Rise Time		0	5	ns
18	MEMCLK Fall Time		0	5	ns

Notes:

1. *MEMCLK as an input is always CMOS level.*
2. *MEMCLK can drive an external load of 150 pF.*
3. *The input setup times with MEMCLK used as an input are improved if MEMCLK and INCLK are tied to the same clock input. This is possible only if the processor and bus operate at the same frequency.*
4. *Except where noted, measurement conditions are the same as the Am29000 microprocessor.*
5. *All output valid delays are measured with V_{OL} = 1.5 V and V_{OH} = 1.5 V.*

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