



# AWT921S11

Integrated High Power Amp 900 MHz  
Advanced Product information  
Rev. 6

## DESCRIPTION

The AWT921 is a monolithic amplifier for use in communication systems that require high gain and output intercept point. This device has been specifically designed for multi carrier and micro cell base station applications.

## FEATURES

- High output power levels
- High Efficiency
- True Surface Mount Package with Integrated Heat Slug
- Internal Bias Circuit Requiring Nominal Input Voltages  $\pm 10\%$
- Low Cost
- Off Chip Output Matching Circuit Allows Application Optimization



**S11**  
**SSOP-28 Wide Body**  
**28 Pin Wide Body w/ Heat Slug**

## ABSOLUTE MAXIMUM RATINGS

PIN	SIGNAL	MAX RATING	PIN	SIGNAL	MAX RATING
2	$V_{DD}$	$+7V_{DC}$	11	$V_{REF}$	$+7 V_{DC}$
3	$RF_{IN}$	$+20 \text{ dBm}$	12	$V_{SS}$	$-7 V_{DC}$
4,5	$V_{D1}$	$+10 V_{DC}$	18,19,20,21,22,23,24,25	$V_{D3}$	$+10 V_{DC}$
8,9	$V_{D2}$	$+10 V_{DC}$			

Operating Temperature:  $-30$  to  $+85^\circ \text{C}$

Storage Temperature:  $-55$  to  $+100^\circ \text{C}$

ELECTRICAL SPECIFICATIONS: <sup>(1)</sup>(Pin +12 dBm, fo = 925-960 MHz, V<sub>DS1</sub> = V<sub>DS2</sub> = V<sub>DS3</sub> = 8.5V, V<sub>SS</sub> = -3V, V<sub>REF</sub> = +5V, V<sub>DD</sub> = +5V, Tc=25°C, 50Ω System <sup>(2)</sup>)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Frequency	fo	925	-	960	MHz
Power Output	P <sub>OUT</sub>	-	+ 39	-	dBm
Power Added Efficiency	η <sub>Eff</sub>	-	40	-	%
Gain @ P <sub>OUT</sub> = +39 dBm @ P <sub>OUT</sub> = +30 dBm	PG	-	29 30	-	dB
Harmonics <sup>(3)</sup> 2nd 3rd 4th	-	-	37 47 50	-	dBc
Stability: - 60 dBc all spurious outputs relative to desired signal	-	-	3:1	-	VSWR load, all phase angles
Bias supply currents	I <sub>SS</sub> I <sub>REF</sub> I <sub>DD</sub>	-	8 1.2 8	-	mA mA mA
Quiescent Currents	I <sub>DQ1</sub> I <sub>DQ2</sub> I <sub>DQ3</sub>	-	100 250 200	-	mA mA mA
Input Return Loss		10	-	-	dB
Gain Flatness vs. Frequency @ Pout = +39 dBm @ Pout = +30 dBm	ΔPG	± 0.5 ± 0.5	-	-	dB dB
Thermal Resistance <sup>4</sup>	-	-	4.5	-	C/W

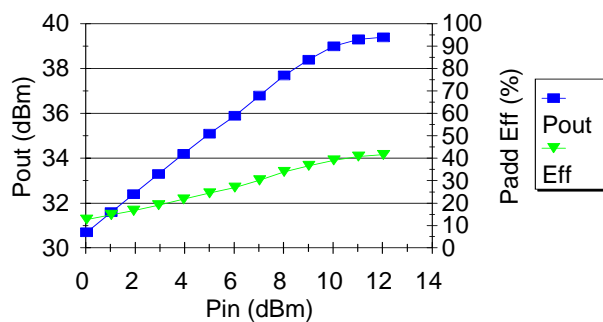
## NOTES:

- 1: As measured in ANADIGICS test fixture, see application section
- 2: 50Ω Measurement system after off chip matching circuit, input terminated in 50Ω
- 3: Measured at Pout = +39 dBm
- 4: Thermal resistance for junction to bottom of slug. Qjc = (Tj - Tc) / ((I<sub>D1</sub> + I<sub>D2</sub> + I<sub>D3</sub>) \* V<sub>SUP</sub> - P<sub>OUT</sub>)

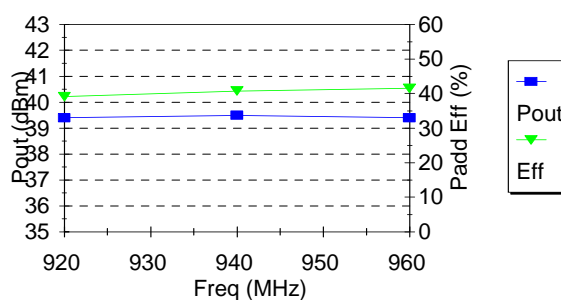
CHARACTERIZATION DATA <sup>(1)</sup> -

Conditions unless otherwise stated (Pin +12 dBm, fo = 925-960 MHz, V<sub>DS1</sub> = V<sub>DS2</sub> = V<sub>DS3</sub> = 8.5V, V<sub>SS</sub> = -3V, V<sub>REF</sub> = +5V, V<sub>DD</sub> = +5V, Tc=25°C, 50 W system <sup>(2)</sup>)

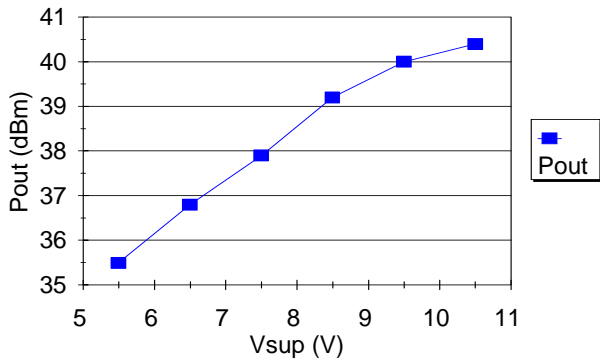
Pout &amp; Eff vs. Pin



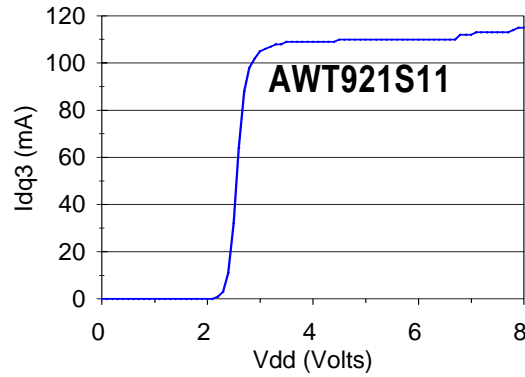
Pout &amp; Eff vs. Frequency



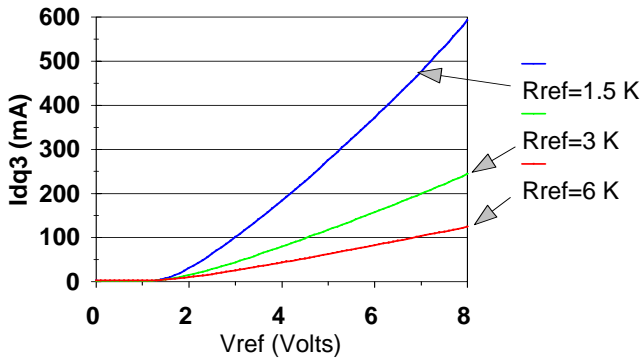
Pout vs. Supply Voltage



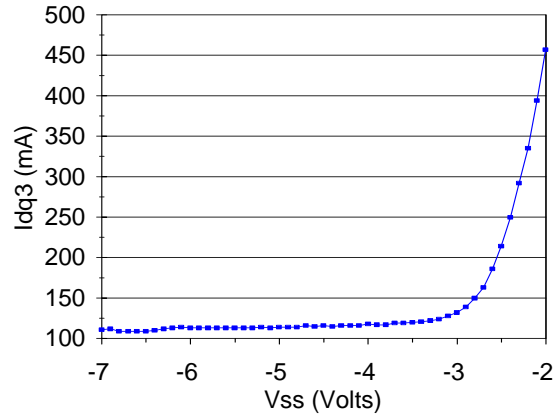
Idq3 vs Vdd



Idq3 vs Vref



Idq3 vs Vss



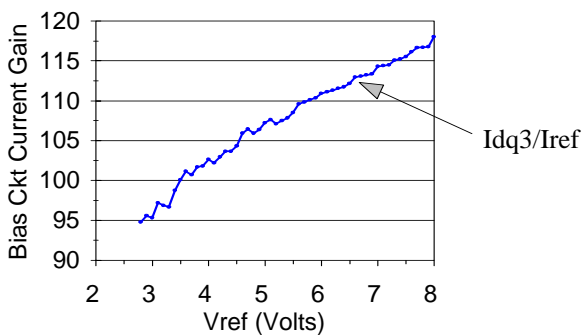
**Notes:**

- 1: As measured in ANADIGICS test fixture, see application section
- 2: 50Ω Measurement system after off chip matching circuit, input terminated in 50Ω

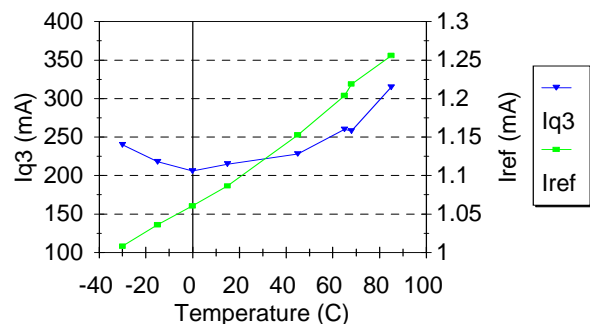
**CHARACTERIZATION DATA: <sup>(1)</sup>**

Conditions unless otherwise stated (Pin +12 dBm, fo = 925-960 MHz,  
 $V_{DS1} = V_{DS2} = V_{DS3} = 8.5V$ ,  $V_{SS} = -3V$ ,  $V_{REF} = +5V$ ,  $V_{DD} = +5V$ ,  $T_c = 25^\circ C$ , 50Ω system) <sup>(2)</sup>

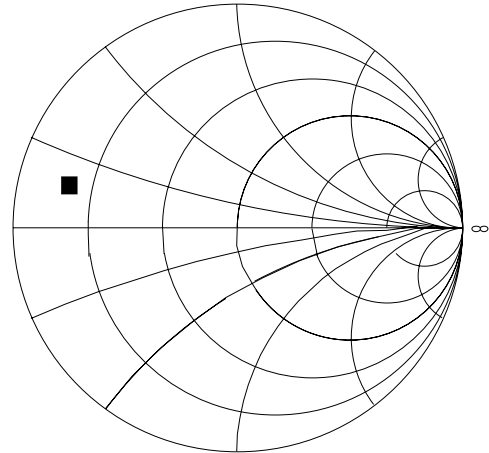
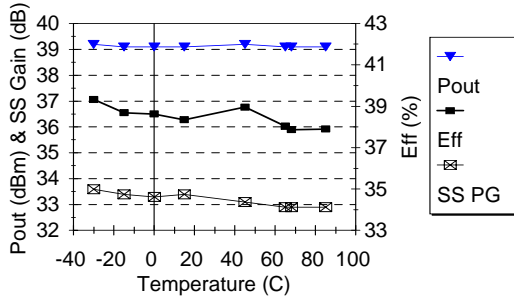
Bias Ckt Gain vs Vref



Iq3 & Iref vs Temperature

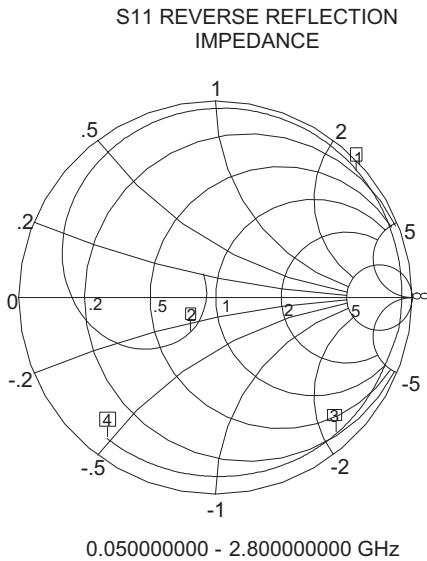


### Pout,PG,& Eff vs Temperature



Load + 3.7 + 3.9 jΩ

Output Load Impedance as seen by the device



CH 4 - S11  
REFERENCE PLANE  
9.0821 cm

MARKER 1  
0.957500000 GHz  
7.074 Ω  
131.906 jΩ

MARKER TO MAX  
MARKER TO MIN

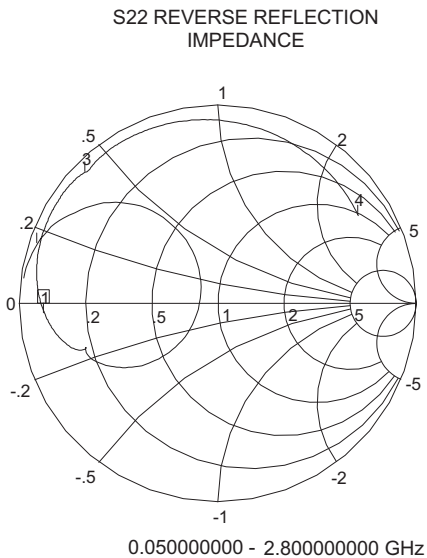
2 0.098125000 GHz  
36.919 Ω  
-13.501 jΩ

3 1.920000000 GHz  
11.446 Ω  
-111.641 jΩ

4 2.800000000 GHz  
3.133 Ω  
-24.550 jΩ

MARKER READOUT  
FUNCTIONS

Impedance as seen by  $V_{DS1}$



TRACE MEMORY  
DISK OPERATIONS

CHANNEL 4

SAVE MEMORY  
TO HARD DISK

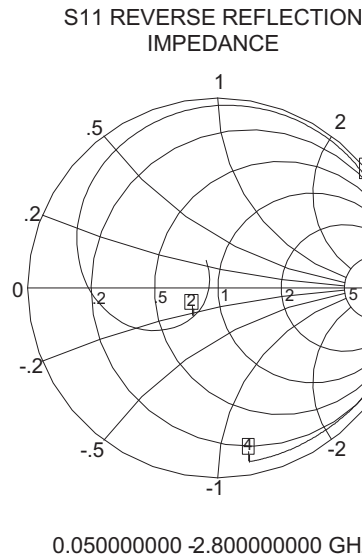
SAVE MEMORY  
TO FLOPPY DISK

RECALL MEMORY  
FROM HARD DISK

RECALL MEM0ORY  
FROM FLOPPY DISK

PRESS<ENTER>  
TO SELECT

Output Impedance as seen by  $V_{DS3}$



CH 4 - S11  
REFERENCE PLANE  
9.0821 cm

MARKER 1  
0.957500000 GHz  
7.659 Ω  
161.181 j Ω

MARKER TO MAX  
MARKER TO MIN

2 0.098125000 GHz  
37.237 Ω  
-11.817 j Ω

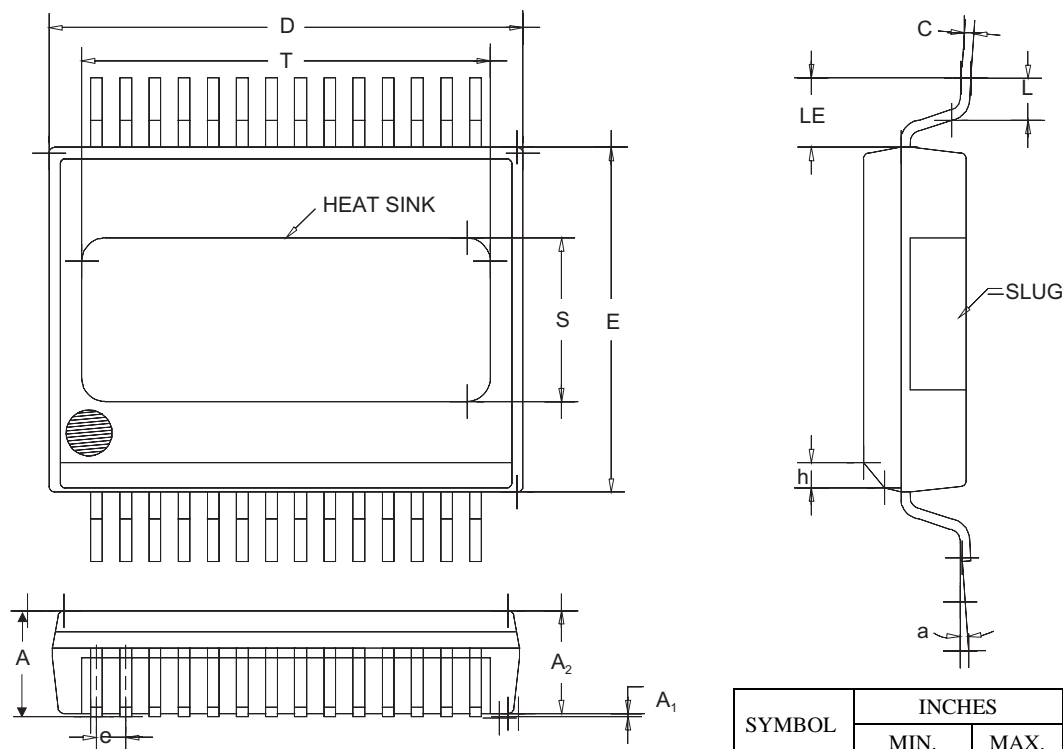
3 1.920000000 GHz  
13.308 Ω  
-171.126 j Ω

4 2.800000000 GHz  
4.466 Ω  
-60.044 j Ω

MARKER READOUT  
FUNCTIONS

Impedance as seen  $V_{DS2}$

## PACKAGE OUTLINE DRAWING

**Notes:**

1. Controlling dimensions : inches.
2. Dimension "d" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.006 (0.16mm).
3. Dimension "e" does not include inter-lead or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 (0.25mm) per side.
4. Maximum lead twist/skew to be 0.002 (0.05mm).
5. Mold flash shall not extend more than 0.010 (0.25mm) on any edge of heat slug.

SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.087	0.093	2.21	2.36	
A <sub>1</sub>	0.000	0.004	0.00	0.10	
A <sub>2</sub>	0.087	0.089	2.21	2.25	
B	0.008	0.012	0.36	0.46	
C	0.007	0.009	0.18	0.25	
D	0.400	0.408	10.16	10.36	2
E	0.292	0.296	7.42	7.52	2
e	0.025	BSC	0.64	BSC	4
H	0.410	0.418	10.41	40.62	
h	0.018	0.024	0.48	0.61	
L	0.034	0.038	0.86	0.97	
LE	0.84		1.37		
a	0	8	0	8	
S	0.139	0.141	3.54	3.55	5
T	0.349	0.351	8.86	8.92	5

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