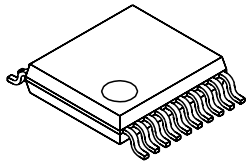
SONY

CXG1092N

SP5T GSM Triple-Band Antenna Switch

20 pin SSOP (Plastic)



Description

The CXG1092N is a high power antenna MMIC switch for use in triple-band GSM handsets.

One antenna can be routed to either of the 2 Tx or 3 Rx ports.

Features

- 4 CMOS compatible control lines
- Standby control
- 34.5dBm power handling at 5.0V (GSM900)
- Low second harmonic < –36dBm at 34.5dBm
- Small package size: 20-pin SSOP (6.4 × 5.0 × 1.25mm)

Applications

Triple-band handsets using combinations of GSM900/DCS1800/PCS1900 and DECT

Structure

GaAs J-FET MMIC (The Sony JFET process is used for low insertion loss.)

Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

Note on Handling

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E99Z07-PS

Truth Table

On Pass	GSM900	DCS1800	PCS1900	Rx ON	STDBY
Ant.-Tx1 GSM900	H	L	L	L	H
Ant.-Tx2 GSM1800	L	H	L	L	H
Ant.-Rx1 GSM900/1800/1900	H	L	L	H	H
Ant.-Rx2 GSM900/1800/1900	L	H	L	H	H
Ant.-Rx3 GSM900/1800/1900	L	L	H	H	H
OFF	—	—	—	—	L

CMOS logic values (Ta = 25°C)

Logic	Min.	Typ.	Max.	Unit
High	2.4	2.8	3.2	V
Low	0.0		0.4	V

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Ant-Tx1, Tx2	*1		0.6	0.9	dB
			*2		0.7	1.0	dB
		Ant-Rx1, Rx2, Rx3	*3		0.6	0.9	dB
			*4		0.85	1.1	dB
			*5		0.9	1.15	dB
Isolation	ISO.	Ant-Tx1, Tx2	*3	15			dB
			*4, *5	14			dB
		Ant-Rx1, Rx2, Rx3	*1	18			dB
			*2	17			dB
VSWR	VSWR				1.2		
Harmonics**Note)**	2fo	Ant-Tx1, Tx2	*1, *2			–36	dBm
	3fo		*1, *2			–30	dBm
P_{1dB} compression input power	P_{1dB}	Ant-Tx1			36		dBm
		Ant-Tx2			35.5		
Control current	Ictl					170	µA
Supply current Tx mode	I_{TX}		STBY = H TxON = L			1	mA
Supply current Rx mode	I_{RX}		STBY = H RxON = H			1	mA
Leakage current	I_{IK}		STBY = L			100	µA

*1 Pin 1 = 34.5dBm, 880 to 915MHz, V_{DD} = 5.0V (GSM Tx)

*2 Pin 2 = 32dBm, 1710 to 1910MHz, V_{DD} = 5.0V (DCS & PCS Tx)

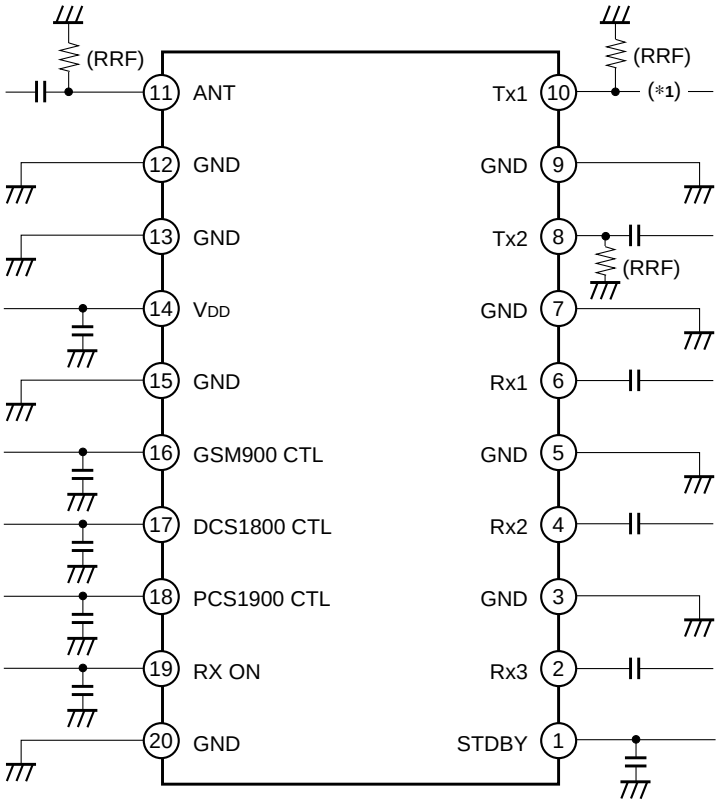
*3 Pin 3 = 10dBm, 925 to 960MHz (GSM Rx)

*4 Pin 4 = 10dBm, 1805 to 1880MHz (DCS Rx)

*5 Pin 5 = 10dBm, 1930 to 1990MHz (PCS Rx)

Note) Harmonics measured with Tx inputs harmonically matched.
Sony recommends the use of harmonic matching to ensure optimum device performance Application Note (1).

Recommended Circuit



Recommended PCB Layout

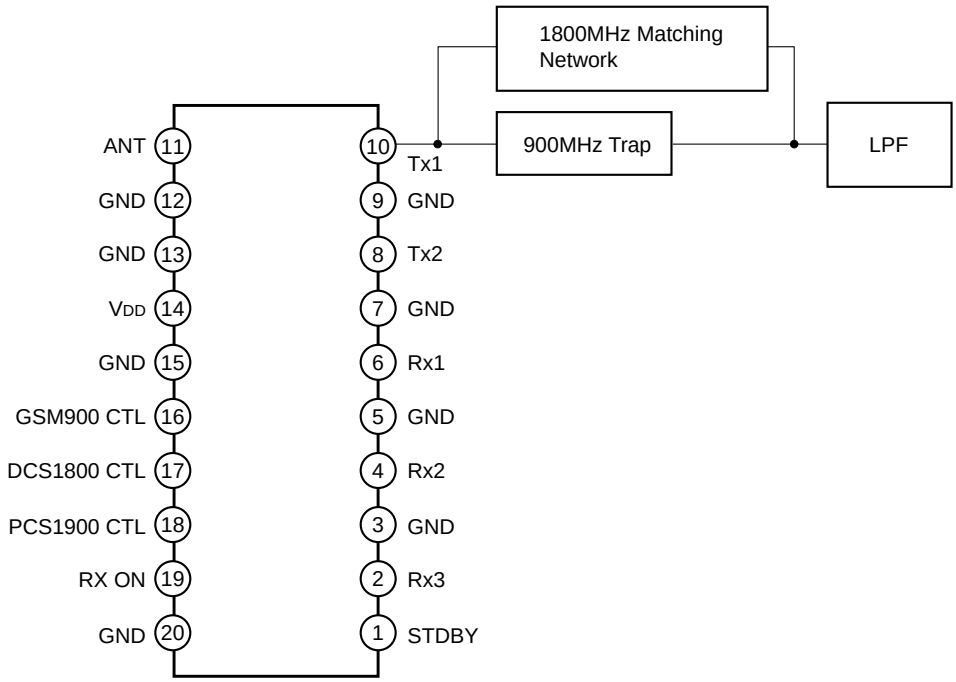
* As indicated in the diagram AC coupling capacitors are necessary to the Ant, Tx1, Tx2, Rx1, Rx2 and Rx3 pins, and decoupling capacitors are necessary to the V_{DD}, STDBY and CTL lines.
* The ground plane should be included under the device and all ground pins connected to this.
* RRF (200kΩ) is used to stabilize the electrical characteristics at the high power signal input. These resistors are required to ensure correct operation of the switch.

*1 See Application Note (1).

Application Note (1)

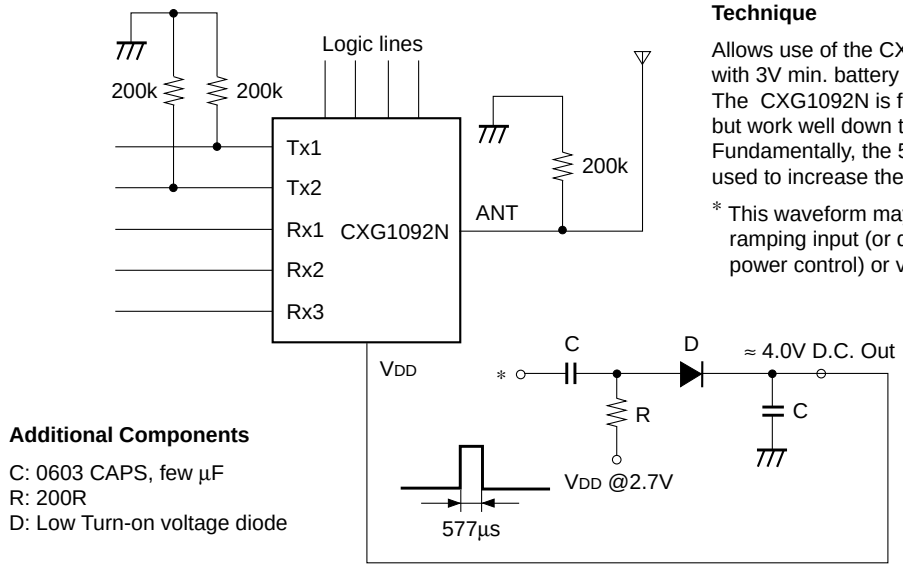
Impedance matching for harmonic minimization

To achieve the 2nd harmonic levels lower than –36dBm for GSM900
Design of 1.8GHz harmonic matching network and the 900MHz trap network is dependent on the board design and components.



Application Note (2)

Operating the CXG1092 from a 3V supply



Technique

Allows use of the CXG1092N (SP5T) in handsets with 3V min. battery voltage (2.7V SW supply). The CXG1092N is for 5V nominal battery voltage but work well down to 4V.
Fundamentally, the 577µs time slot waveform is used to increase the 2.7V supply to over 4V.

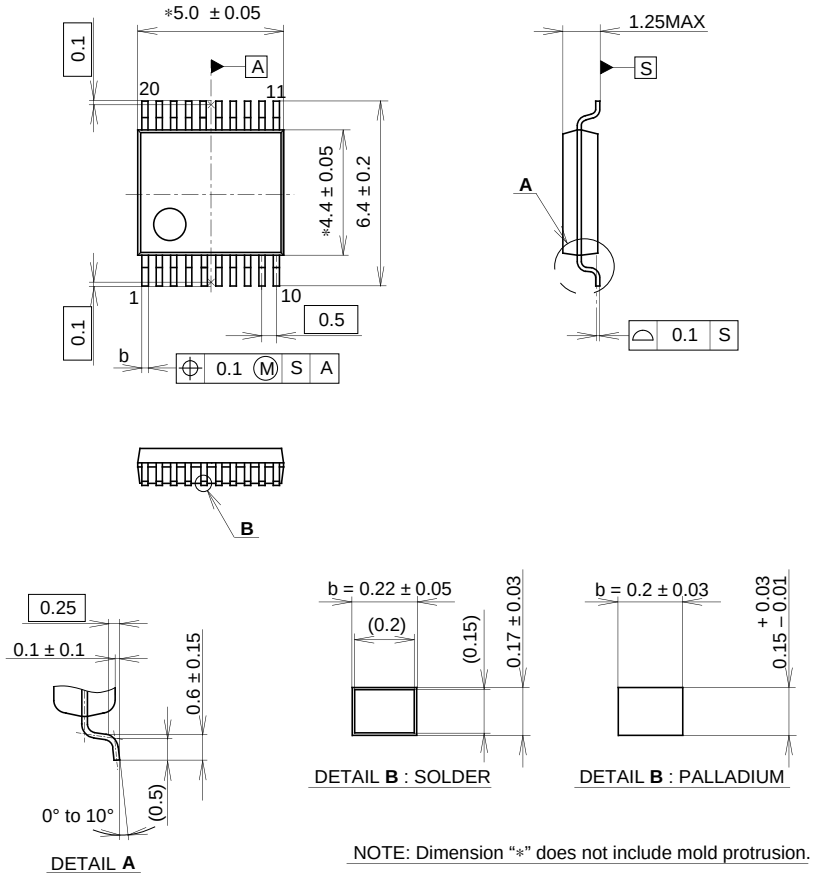
* This waveform may be taken from the PA ramping input (or drain supply in case of drain power control) or via the TX ON/OFF logic.

Additional Components

C: 0603 CAPS, few µF
R: 200R
D: Low Turn-on voltage diode

Package Outline Unit: mm

20PIN SSOP(PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-20P-L03
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g