MN86157 Shading Correction LSI

Overview

The MN86157 contains a 7-bit A/D converter for use in correcting, at the bit level, shading distortion for signals from image sensors, optics, and similar sources.

It uses external RAM to support adaptive correction that responds to changes in distortion patterns. It also uses ROM to provide fixed correction when a white reference plane signal is not available.

The chip is also usable as a stand-alone A/D converter.

Features

- Choice of correction range (50% or 75%) depending on extent of shading distortion
- Parallel A/D converter functions

Resolution: 7 bits

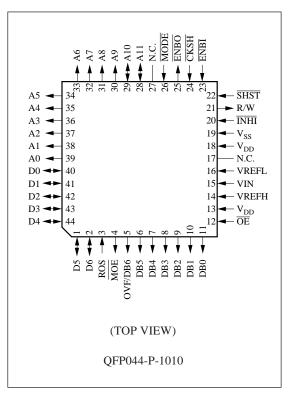
Non-linearity: ±1/2 LSB

Conversion speed: max. 5 MHz

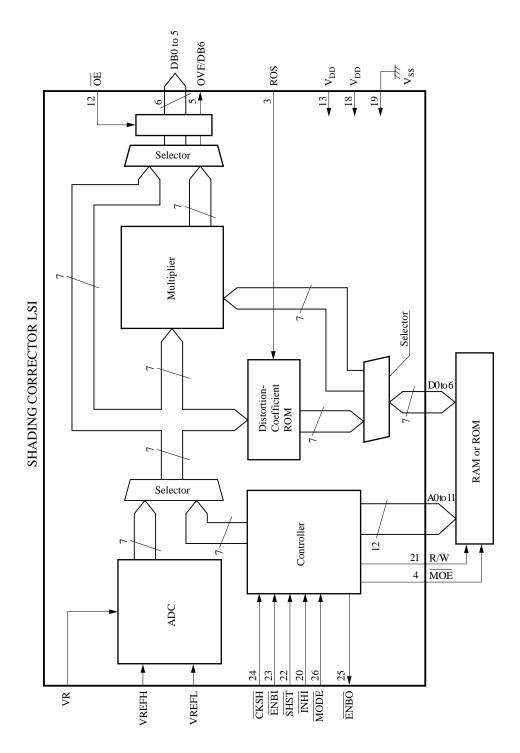
Note: This is the guaranteed design value for the chip used as a stand-alone A/D converter. The guaranteed value at shipment is ± 3 LSB

- Ability to start and stop clock in the middle of a line to support CdS contacting image sensors and other devices with variable scanning rates
- Overflow pin that simplifies task of adding auto background control (ABC) circuit
- Single 5 volt power supply
- Guaranteed TTL levels for input
- Applications
- Facsimile equipment

Pin Assignment



Block Diagram



MN86157 Block Configuration

The MN86157 consists of four basic blocks: (1) A/D converter, (2) distortion coefficient mapping ROM, (3) multiplier, and (4) controller.

The following are brief descriptions of each block.

(1) A/D converter

This uses comparison with the reference voltages to convert the scanner's image data signal from the VIN pin to a 7-bit digital output.

- (2) Distortion coefficient mapping ROM This constitutes a look-up table for converting the A/D converter output to a final value for storage in the external RAM.
- Multiplier
 This provides high-speed parallel multiplication of 7 × 7 bits data.
- (4) Controller

This controls operation of the shading correction circuits, the A/D converter, and interface to external ROM or RAM.

Operation

- Shading correction (MODE pin at "H" level)
 - Fixed distortion coefficients (external memory is ROM)

This configuration provides 6-bit corrected data using fixed distortion coefficients stored in an external ROM and thus invariant.

• Adaptive distortion coefficients (external memory is RAM)

This configuration provides 6-bit corrected data using distortion coefficients, stored in external RAM, that the chip constantly updates using white reference plane line training.

• Pixels per line

The chip supports line lengths up to 4096 pixels with a built-in 12-bit address counter supporting interfaces to two $2^{11} \times 8$ -bit RAM chips or the equivalent of a 2732 ROM ($2^{12} \times 8$ bits).

- Input clock The chip uses an input clock signal with a frequency twice that of the image clock.
- Selecting correction range The ROS pin provides a choice of two correction ranges and consequently correction precisions.

ROS	Correction Range	Correction Precision
Н	50%	±1.5%
L	75%	±3.0%

Correction start/stop function Pulling the INHI pin to "L" level in the middle of a line suspends correction and maintains the output data at its current value. Returning the pin to "H" level restarts correction.

Auto clamp and overflow functions for output data

If the image input signal level exceeds the white reference plane level, the chip clamps the output data at the full-scale value $(3F_H)$ and drives the overflow pin (OVF) at "H" level.

MN86157

- Stand-alone A/D converter (MODE pin at "L" level, A10 pin at "L" level)
 - In this configuration, the chip functions as a parallel A/D converter consisting of 128 chopper comparators.

Resolution: 7 bits Non-linearity: $\pm 1/2$ LSB Conversion speed: max. 5 MHz Analog input range: 3V p-p (V_{DD} 5V)

 Clock mode selection The A11 pin provides a choice of two clock modes.

	modes	5.			
A11	Input Clock Conditions				
	CKSH:	Supply a clock signal with a frequency			
L		twice that of the input image clock. *1			
	SHST:	Supply the A/D start signal for use in			
		synchronizing phase.			
Н	CKSH:	Supply a clock signal with a			
		frequency twice that of the input			
		image clock. *2			
	ENBI :	Supply a clock signal with the same			
		frequency as the input image clock.			

Notes

*1: ENBI

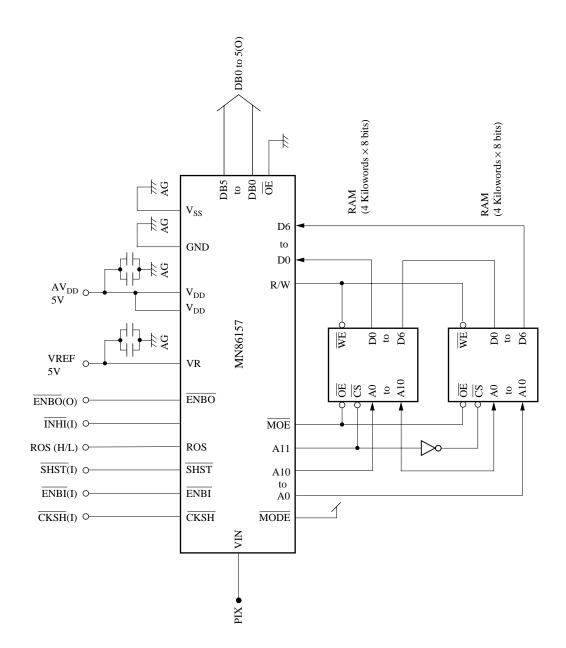
*2: SHST: Keep this pin at "H" level.

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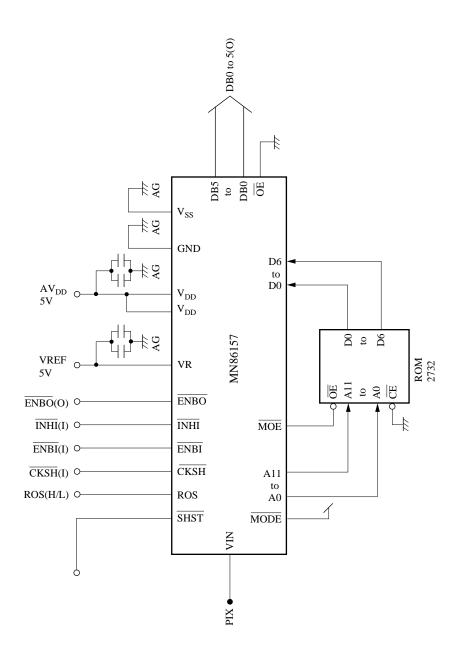
	scriptions				
Parameter	Pin No.	Symbol	I/O	Function Description	Remarks
A/D	15	VIN	Ι	Analog image signal input	
converter	14	VREFH		Reference voltage input	"H" level reference voltage input
block	16	VREFL		Reference ground	"L" level reference voltage input
MULT	11 to 6	DB 0 to 5	0	Corrected image signal output	MODE: H
converter				/A/D converter data output	/MODE: L
block	5	OVF/DB6	0	Corrected image signal overflow	MODE: H
				output/A/D converter data output	/MODE: L
	12	ŌĒ	Ι	Output enable signal input	H: Pins are high-impedance;
				for DB0 – DB5 and OVF	L: Pins provide output
CTL	23	ENBI	Ι	Enable signal input for single line	
converter	22	SHST	Ι	Start input for reading white	Low pulse
block				reference signal	signals start.
	24	CKSH	Ι	Clock signal input	The frequency must be twice
					that of the image clock.
	20	ĪNHĪ	Ι	Signal for suspending correction in	H: Normal correction
				the middle of a line and holding	operation;
				the output at the current value	L: Stop and hold
	25	ENBO	0	Enable signal for corrected	
				image data output	
	3	ROS	Ŧ		H: 50% correction;
			Ι	Correction range selection	L: 75% correction
	26	MODE	Ŧ		H: Shading correction;
			Ι	Operating mode selection	L: A/D conversion only
DAM	39 to 28	A 0 to 11	0	RAM/ROM address output	
RAM /ROM	40 to 44,	DOLL	L/O		
IO	1, 2	D 0 to 6	I/O	RAM/ROM data I/O	
converter	21	R/W	0	RAM read/write signal	
block	4	MOE	0	RAM/ROM output enable signal	

Pin Descriptions

■ Application Circuit Example #1: Using RAM



■ Application Circuit Example #2: Using ROM



Packing Dimensions (Unit: mm)

QFP044-P-1010

