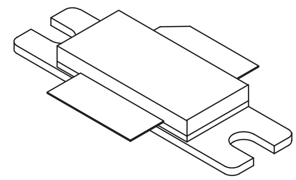
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19060
MRF19060R3
MRF19060SR3

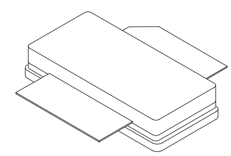
1990 MHz, 60 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for CDMA, TDMA, GSM and multicarrier amplifier applications.

- Typical CDMA Performance: 1960 MHz, 26 Volts
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  - Output Power — 7.5 Watts
  - Power Gain — 12.5 dB
  - Adjacent Channel Power —
    - 885 kHz: –47 dBc @ 30 kHz BW
    - 1.25 MHz: –55 dBc @ 12.5 kHz BW
    - 2.25 MHz: –55 dBc @ 1 MHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 60 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.



CASE 465–06, STYLE 1
NI–780
MRF19060R3



CASE 465A–06, STYLE 1
NI–780S
MRF19060SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Total Device Dissipation @ $T_C \geq = 25°C$ Derate above 25°C	P_D	180 1.03	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

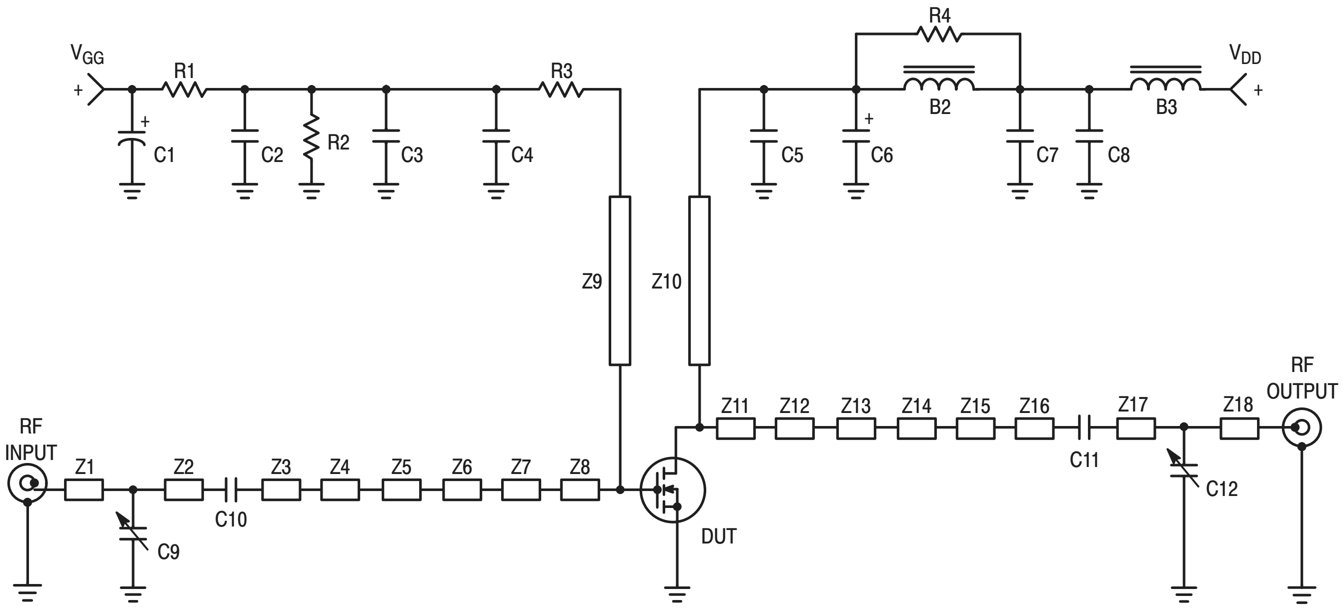
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$VGS_{(th)}$	2	—	4	V
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	V
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	V
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	G_{ps}	11	12.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	η	33	36	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 60 W CW, f = 1990 MHz)	P1dB	—	60	—	W
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B2 – B3	Ferrite Beads, Fair Rite, 2743019447
C1	10 μF, 50 V Electrolytic Capacitor, Panasonic #ECEV1HV100R
C2, C7	1000 pF Chip Capacitors, B Case, ATC #100B102JCA500X
C3, C8	0.10 μF Chip Capacitors, B Case, Kemet #CDR33BX104AKWS
C4	5.1 pF Chip Capacitor, B Case, ATC #100B5R1JCA500X
C5	6.2 pF Chip Capacitor, B Case, ATC #100B6R2JCA500X
C6	22 μF, 35 V Tantalum Capacitor, SMT, Sprague
C9	0.8 pF – 8.0 pF Variable Capacitor, Johanson Gigatrim
C10, C11	10 pF Chip Capacitors, B Case, ATC #100B100JCA500X
C12	0.4 pF – 2.5 pF Variable Capacitor, Johanson Gigatrim
R1	1 kΩ, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″
R2	560 kΩ, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″
R3	15 Ω, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″
R4	10 Ω, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″
Z1	0.580″ x 0.074″ Microstrip
Z2	0.100″ x 0.074″ Microstrip
Z3	0.384″ x 0.074″ Microstrip
Z4	0.152″ x 0.140″ Microstrip
Z5	0.090″ x 0.102″ Microstrip
Z6	0.245″ x 0.217″ Microstrip
Z7	0.090″ x 0.737″ Microstrip
Z8	0.530″ x 0.941″ Microstrip
Z9	1.010″ x 0.050″ Microstrip
Z10	1.060″ x 0.050″ Microstrip
Z11	0.446″ x 1.137″ Microstrip
Z12	0.152″ x 0.567″ Microstrip
Z13	0.183″ x 0.220″ Microstrip
Z14	0.100″ x 0.338″ Microstrip
Z15	0.480″ x 0.142″ Microstrip
Z16	0.140″ x 0.080″ Microstrip
Z17	0.173″ x 0.080″ Microstrip
Z18	0.420″ x 0.080″ Microstrip
Board	0.030″ Glass Teflon® Arlon GX–0300–55–22, 2 oz Cu

Figure 1. MRF19060 Test Circuit Schematic

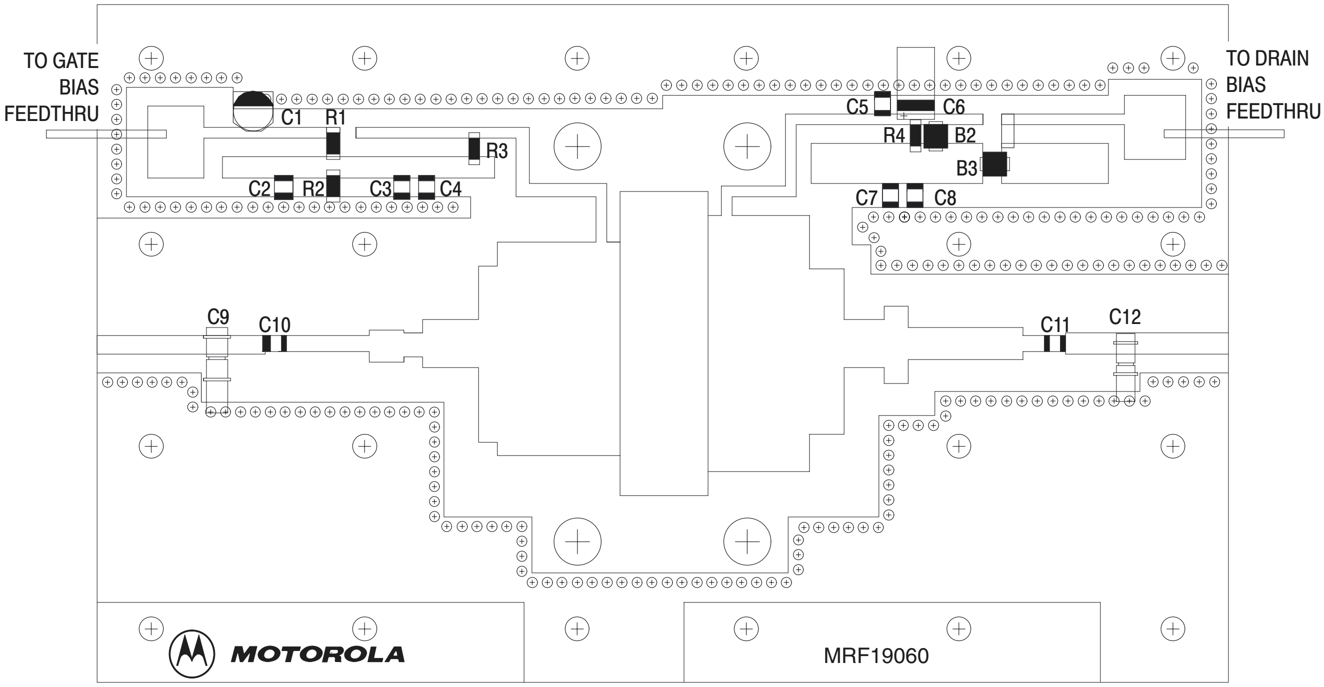


Figure 2. MRF19060 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

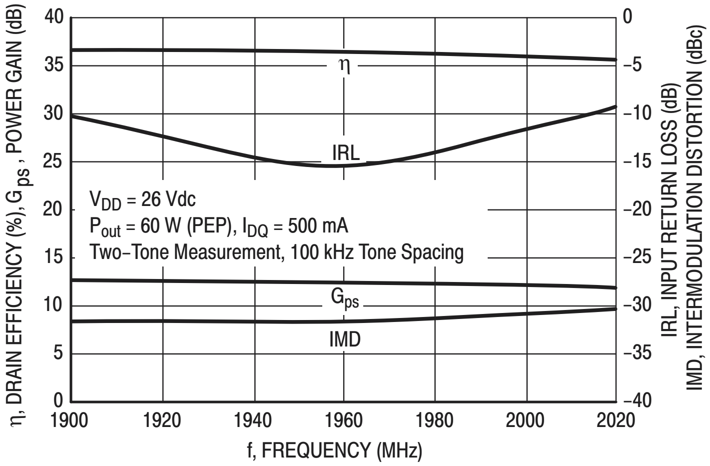


Figure 3. Class AB Broadband Circuit Performance

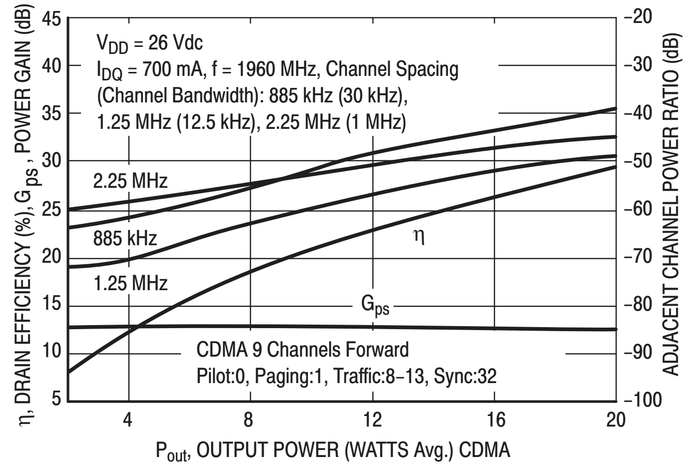


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

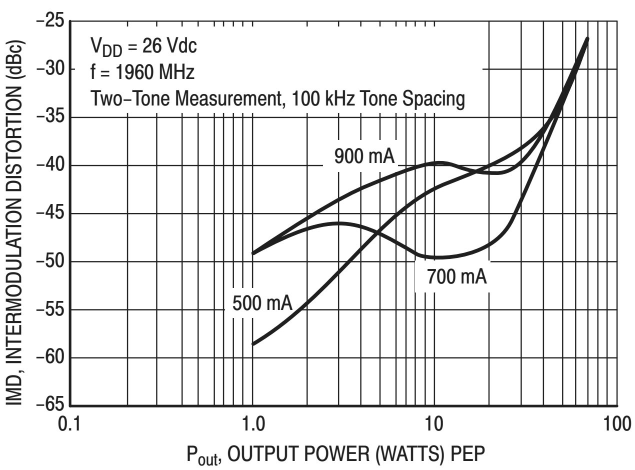


Figure 5. Intermodulation Distortion versus Output Power

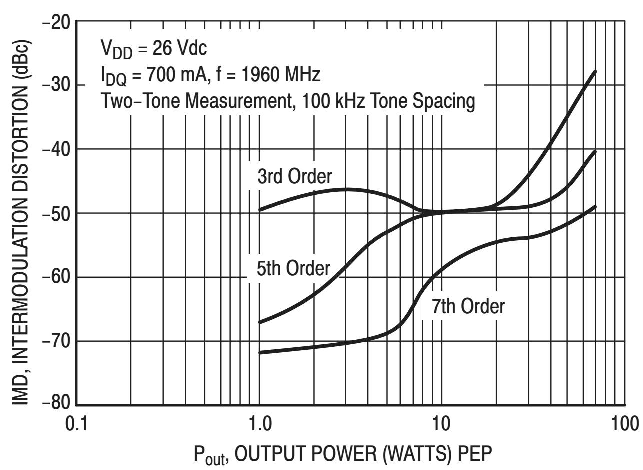


Figure 6. Intermodulation Products versus Output Power

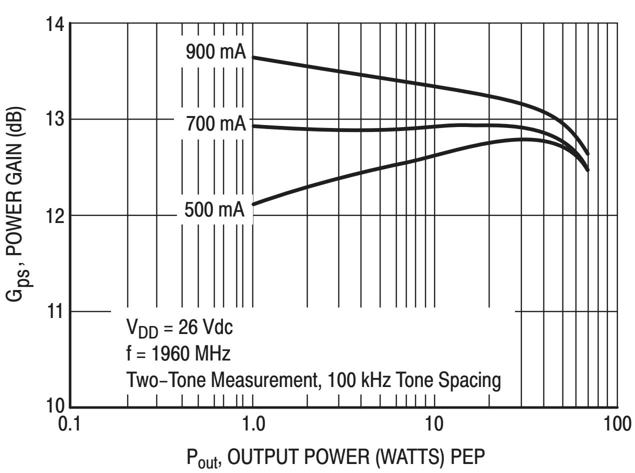


Figure 7. Power Gain versus Output Power

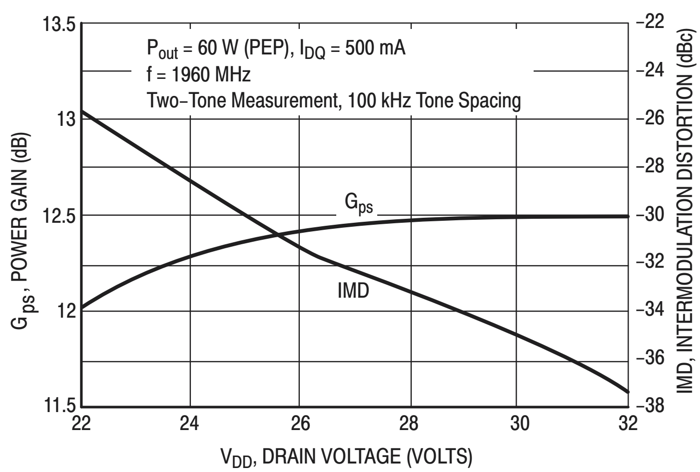
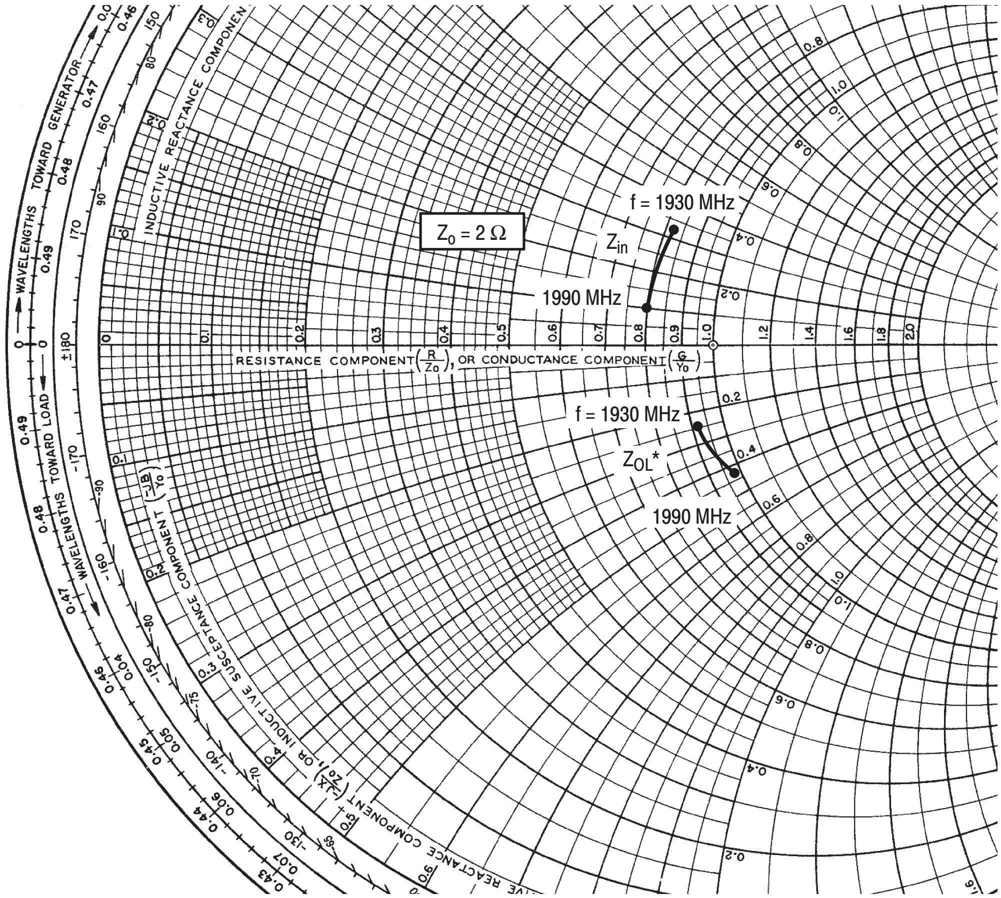


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 26 V, I_{DQ} = 500 mA, P_{out} = 60 W PEP

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	1.65 + j0.67	1.85 – j0.50
1960	1.64 + j0.45	1.89 – j0.74
1990	1.60 + j0.20	1.96 – j0.94

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

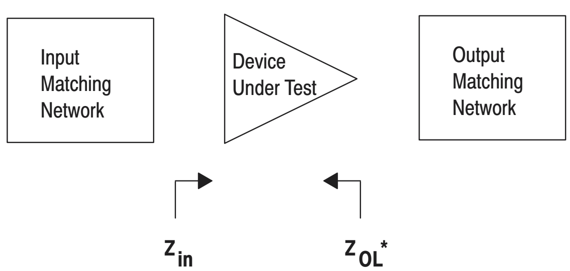
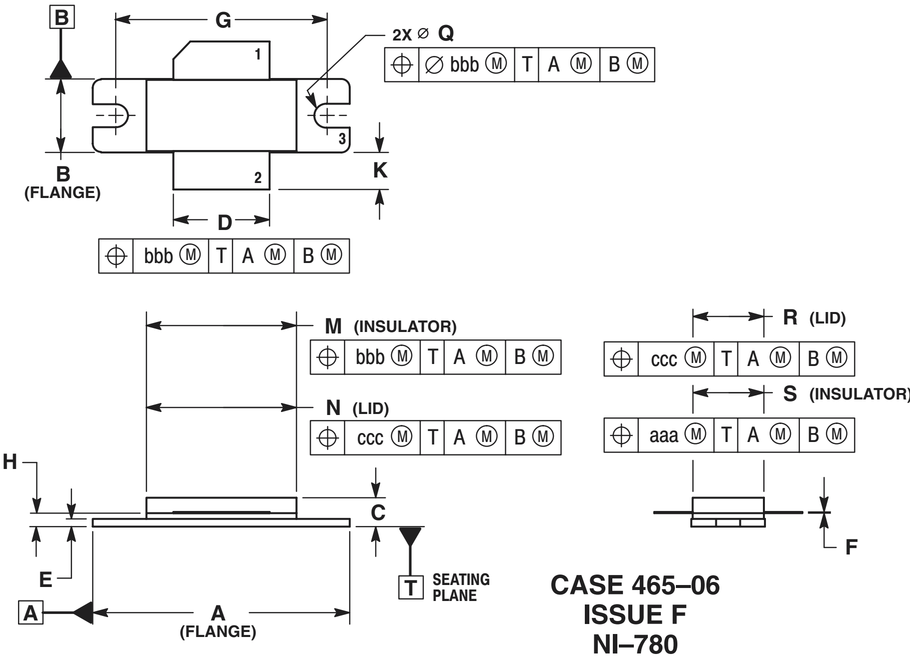


Figure 9. Series Equivalent Input and Output Impedance

PACKAGE DIMENSIONS

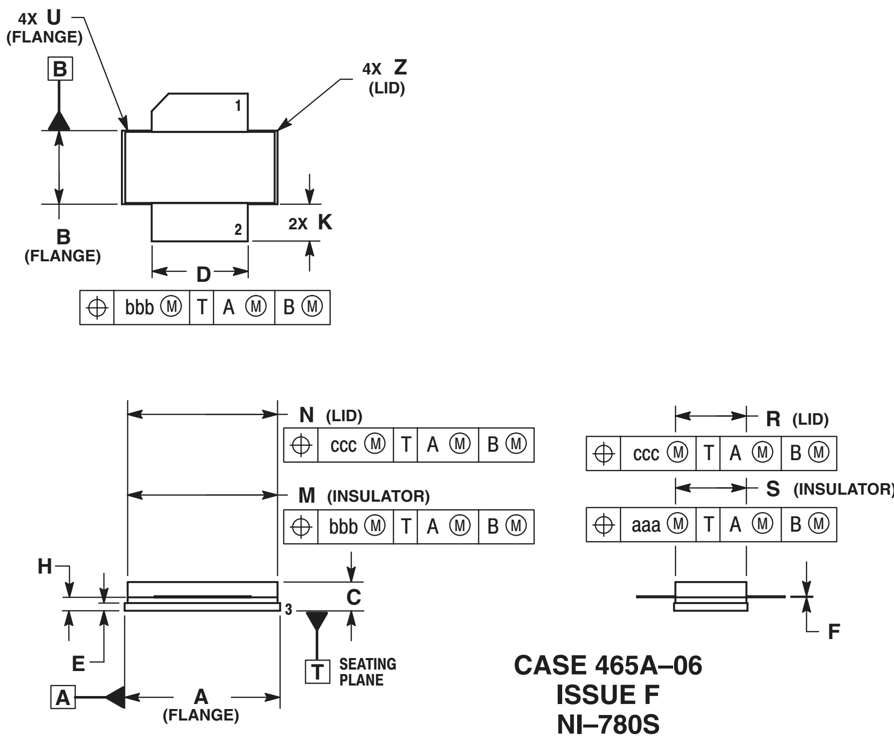


CASE 465–06
ISSUE F
NI–780
MRF19060

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE



CASE 465A–06
ISSUE F
NI–780S
MRF19060SR3

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3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

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