ST10F280-AB

16-Bit MCU with 512K Byte FLASH and 18K Byte RAM Memories

ERRATA SHEET

1 - DESCRIPTION

This errata sheet describes the functional and electrical problems known in the revision AB of the ST10F280-AB engineering samples.

The ST10F280-AB engineering samples marked as EAB-xxxx are not completely tested in all electrical and functional characteristics and should be used for functional evaluation only.

Test conditions for these engineering samples are:

– TA Room Temperature (25°C)

– Vcc 5.0V ±10%

– Fosc 40MHz, PLL disabled, direct drive (f_{CPU} = 40MHz)

2 - FUNCTIONAL PROBLEMS

The following malfunctions are known in this step:

2.1 - PWRDN.1 - Execution of PWRDN Instruction

When instruction PWRDN is executed while pin $\overline{\text{NMI}}$ is at a high level (if PWRDCFG bit is clear in SYSCON register) or while at least one of the port 2 pins used to exit from power-down mode (if PWRDCFG bit is set in SYSCON register) is at the active level, power down mode is not entered, and the PWRDN instruction is ignored.

However, under the conditions described below, the PWRDN instruction is not ignored, and no further instructions are fetched from external memory, i.e. the CPU is in a quasi-idle state.

This problem only occurs in the following situations:

a) The instructions following the PWRDN instruction are located in an external memory, and a **multiplexed bus** configuration **with memory tristate waitstate** (bit MT-TCx = 0) is used.

   Or

b) The instruction preceeding the PWRDN instruction **writes** to external memory or an XPeripheral (XRAM,CAN), and the instructions following the PWRDN instruction are located in external memory. In this case, the problem occurs for any bus configuration.

Note: The on-chip peripherals are still working correctly, in particular the Watchdog Timer, if not disabled, resets the device upon an overflow. Interrupts and PEC transfers, however, cannot be processed. In case NMI is asserted low while the device is in this quasi-idle state, power-down mode is entered.

No problem occurs if the $\overline{\text{NMI}}$ pin is low (if PWRDCFG = 0) or if all P2 pins used to exit from power-down mode are at inactive level (if PWRDCFG = 1): the chip normally enters powerdown mode.

Workaround:

Ensure that no instruction that writes to external memory or an XPeripheral preceeds the PWRDN instruction, otherwise insert a NOP instruction in front of PWRDN. When a multiplexed bus with memory tristate wait state is used, the PWRDN instruction must be executed from internal RAM or XRAM.

2.2 - MAC.9 - CoCMP Instruction Inverted Operands

The ST10 Family Programming Manual describes the CoCMP instruction as: subtracts a 40-bit signed operand from th 40-bit accumulator content (acc - op2\op1), and updates the N, Z and C flags in the MSW register, leaving the accumulator unchanged. On the device the reverse operation (op2\op1 - acc) has been implemented in the Mac Unit. Therefore, the N and C flags are set according to the reverse operation (Z flag is not affected).

Workaround:

Change interpretation of the N and C flags in the MSW register.

Example:

```
MOV     R12, #07h
MOV     R13, #06h
MOV     R14, #0
CoLOAD  R14, R12        ; Accumulator = 70000h
CoCMP   R14, R13        ; Compares 70000h to 60000h
```

Here the content of MSW is 0500h, i.e. C = 1, Z = 0 and N = 1.

To test if the Accumulator was greater than or equal the compared value, the "normal" test, according to the description in the ST10 Programming Manual, would be:

```
JNB     MSW.10, Greater ; If C flag cleared, then greater than or equal
```

With the implementation, this test does not provide the expected result.

To obtain the correct comparison, use instead:

```
JB      MSW.10, Greater ; C flag set: 60000h < 70000h (60000h-70000h implemented)
                        ; i.e. the accumulator is greater than or equal compared value
```

2.3 - MAC.10 - E Flag Evaluation for CoSHR and CoASHR Instructions when Saturation Mode is Enabled

The Logical and the Arithmetic Right Shift instructions (CoSHR/CoASHR) are specifiifed not to be affected by the saturation mode (MS bit of the MCW register): the shift operation is always made on the 40 bits of the accumulator. The result shifted in the accumulator is never saturated. Only when the saturation mode is enabled, the evaluation of the E Flag (in the MSW register) is erroneous.

Comment to the example:

In the example below (Table 1), the E Flag is kept cleared however MAE is used: bit 0 of MAE has been shifted into bit 15 of MAH. The MAE part has been used and it contents significant bits but the E Flag has not been set.

The content of the flags is given after the execution of the instruction.

Table 1 : MAC.10 Example

MS Bit is Set, Saturation Mode is Enabled					Status of Flags After Instruction Execution						
Code		Accumulator Value (Hexa.)			SL	E	SV	C	Z	N	Remark
MOV	R5, #5555h	--	----	----	-	-	-	-	-	-	-
CoLOAD	R5, R5	00	5555	5555	0	0	0	0	0	0	Right
NOP		00	5555	5555	0	0	0	0	0	0	Right
MOV	MSW, #007Fh	7F	5555	5555	0	0	0	0	0	0	Right
NOP		7F	5555	5555	0	0	0	0	0	0	Right
CoSHR	#1	3F	AAAA	AAAA	0	0*	0	0	0	0	*E is wrong

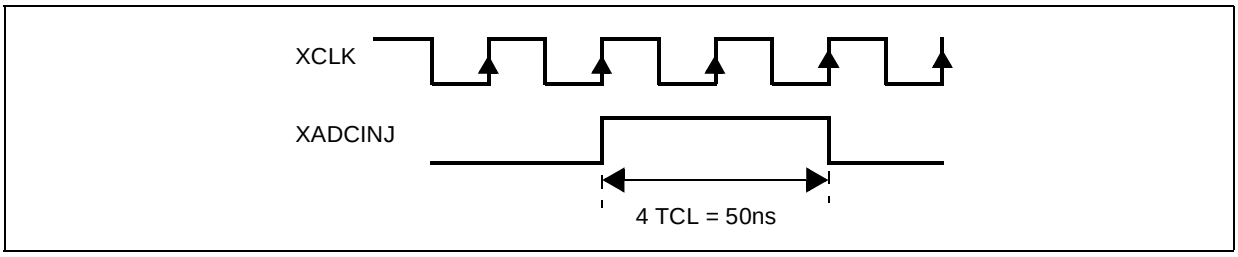
Workaround:

If the MAE flag is used, the saturation mode must be disabled before running Logical and/or Arihmetic Right Shift instructions and re-enable just after.

2.4 - ST_XTIMER.01 - XADCINJ Signal Output Too Short for ADC Channel Injection

The duration of the XADCINJ output lasts two cycles (50ns at 40MHz) but to ensure that a signal transition is properly recognized, an external capture input signal should be held for at least 8 CPU clock cycles before it changes its level so the duration of the XADCINJ signal is too short.

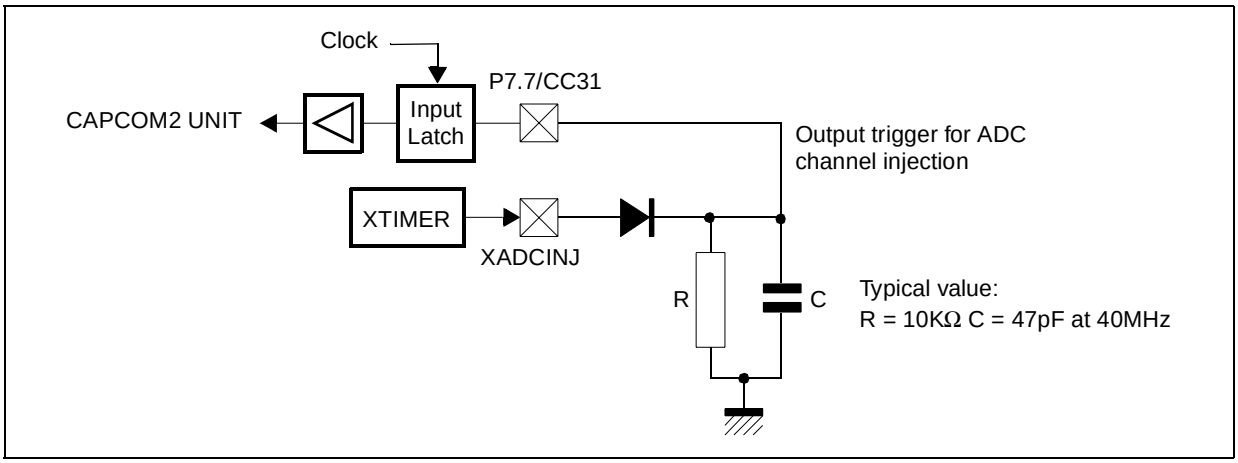
Figure 1 : XADCINJ Timing



Workaround:

The falling edge of the XADCINJ signal must be delayed up to 8 CPU clock cycles.

Figure 2 : External Connection for ADC Channel Injection



History of Fixed Functional Problems of the ST10F280

Name	Short Description	Fixed in Step
ST_XADCMUX.01	Erroneous Conversion Result in Overload Condition	AB

Summary of Remaining Functional Problems Known on the ST10F280-AB

Name	Short Description
PWRDN.1	Execution of PWRDN Instruction
MAC.9	CoCMP Instruction Inverted Operands
MAC.10	E Flag Evaluation for CoSHR and CoASHR Instructions when Saturation Mode is Enabled
ST_XTIMER.01	XADCINJ Signal Output Too Short for ADC Channel Injection

3 - DEVIATIONS FROM DC/AC PRELIMINARY SPECIFICATION

DC Parameters

Engineering data are not completly collected yet.

AC Timings

Engineering data are not completly collected yet.

Note on On-Chip Oscillator

The XTAL2 output is not designed to provide a valid signal when XTAL1 is supplied by an external clock signal. It may happen, if the external clock signal is not perfectly symetrical and centered on V_{DD} / 2, that XTAL2 signal is not equal to XTAL1.

This is due to the design of the oscillator, which has a auto-adaptation gain control dedicated to external crystal.

If an external clock signal is directly provided on XTAL1 pin, then leave XTAL2 pin disconnected to achieve the lowest consumption of the on-chip oscillator.

4 - ERRATA SHEET VERSION INFORMATION

This document has been released on the 6th of February 2002. It reflects the current silicon status of the ST10F280-AB.

F280-AB.REF