Data Sheet June 1999 File Number 3147.2

8-Channel/Differential 4-Channel, CMOS High Speed Analog Multiplexer

The HI-518 is a monolithic, dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_2 enables the HI-518 to be user programmed either as a single ended 8-Channel multiplexer by connecting 'Out A' to 'Out B' and using A_2 as a digital address input, or as a 4-Channel differential multiplexer by connecting A_2 to the V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Intersil Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current ($I_{D(OFF)}$ < 100pA at 25^{o}C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI3-0518-5	0 to 75	18 Ld PDIP	E18.3
HI1-0518-5	0 to 75	18 Ld CERDIP	F18.3
HI1-0518-8	-55 to 125	18 Ld CERDIP	F18.3

Features

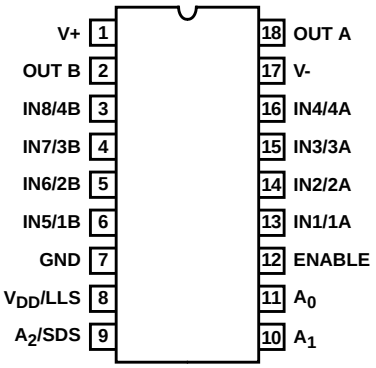
- Access Time (Typical) 130ns
- Settling Time 250ns (0.1%)
- Low Leakage (Typical)
  - $I_{S(OFF)}$ 10pA
  - $I_{D(OFF)}$ 15pA
- Low Capacitance (Max)
  - $C_{S(OFF)}$ 5pF
  - $C_{D(OFF)}$ 10pF
- Off Isolation at 500kHz . . . . . 45dB (Min)
- Low Charge Injection Error 25mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

Pinout

HI-518 (CERDIP, PDIP)
TOP VIEW



Truth Tables

TABLE 1. HI-518 USED AS AN 8-CHANNEL MULTIPLEXER OR DUAL 4-CHANNEL MULTIPLEXER (NOTE 1)

USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	None
H	L	L	H	2A	None
H	L	H	L	3A	None
H	L	H	H	4A	None
H	H	L	L	None	1B
H	H	L	H	None	2B
H	H	H	L	None	3B
H	H	H	H	None	4B

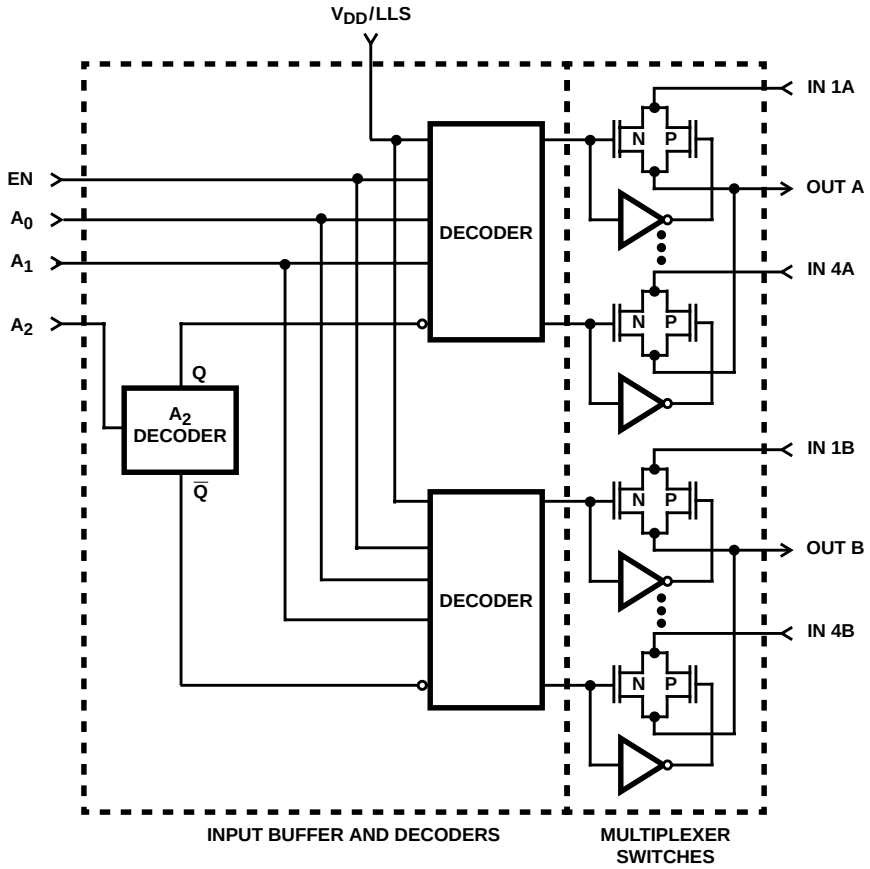
NOTE:

1. For 8-Channel single ended function, tie “Out A” to “Out B”; for dual 4-Channel function, use the A_2 address pin to select between Mux A and Mux B, where Mux A is selected with A_2 low.

TABLE 2. HI-518 USED AS A DIFFERENTIAL 4-CHANNEL MULTIPLEXER

A_2 CONNECTED TO V- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	None	None
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

Functional Block Diagram



A_2 DECODE		
A_2	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

Absolute Maximum Ratings

V+ to V- 33V
Analog (V_{IN}, V_{OUT}) . . . . . (V-) -2V to (V+) +2V
Digital Input Voltage:
TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
V_{A0-1} . . . . . -6V to +6V
$V_{A2/SDS}$ . . . . . (V-) -2V to (V+) +2V
CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
V_{A0-2} . . . . . -2V to (V+) +2V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
PDIP Package	90	N/A
CERDIP Package	70	18

Maximum Junction Temperature
Ceramic Package . . . . . .175^{o}C
Plastic Package . . . . . .150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C

Operating Conditions

Temperature Ranges
HI-518-8 . . . . . -55^{o}C to 125^{o}C
HI-518-5 . . . . . 0^{o}C to 75^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = 0.8V; V_{DD}/LLS = GND (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	-8			-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS									
Access Time, t_A		25	-	130	175	-	130	175	ns
		Full	-	-	225	-	-	225	ns
Break-Before-Make Delay, t_{OPEN}		25	10	20	-	10	20	-	ns
Enable Delay (ON), $t_{ON(EN)}$		25	-	120	175		120	175	ns
Enable Delay (OFF), $t_{OFF(EN)}$		25	-	140	175		140	175	ns
Settling Time	To 0.1%	25	-	250	-	-	250	-	ns
	To 0.01%	25	-	800	-	-	800	-	ns
Charge Injection Error	Note 6	25	-	-	25	-	-	25	mV
Off Isolation	Note 7	25	45	-	-	45	-	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	-	5	-	-	5	pF
Channel Output Capacitance, $C_{D(OFF)}$		25	-	-	10	-	-	10	pF
Digital Input Capacitance, C_A		25	-	-	5	-	-	5	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.02	-	-	0.02	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL} (TTL)	Note 3	Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH} (TTL)	Note 3	Full	2.4	-	-	2.4	-	-	V
Input Low Threshold, V_{AL} (CMOS)	Note 3	Full	-	-	$0.3V_{DD}$	-	-	$0.3V_{DD}$	V
Input High Threshold, V_{AH} (CMOS)	Note 3	Full	$0.7V_{DD}$	-	-	$0.7V_{DD}$	-	-	V
Input Leakage Current, I_{AH} (High)		Full	-	-	1	-	-	1	µA
Input Leakage Current, I_{AL} (Low)		Full	-	-	20	-	-	20	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_{IN}	Note 4	Full	-14	-	+14	-15	-	+15	V
On Resistance, r_{ON}	Note 5	25	-	480	750	-	480	750	Ω
		Full	-	-	1,000	-	-	1,000	Ω
Off Input Leakage Current, $I_{S(OFF)}$		25	-	0.01	-	-	0.01	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$		25	-	0.015	-	-	0.015	-	nA
		Full	-	-	50	-	-	50	nA
On Channel Leakage Current, $I_{D(ON)}$		25	-	0.015	-	-	0.015	-	nA
		Full	-	-	50	-	-	50	nA
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	-	450	-	-	540	mW

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = 0.8V; V_{DD}/LLS = GND (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	-8			-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I+, Current	V_{EN} = 2.4V	Full	-	-	15	-	-	18	mA
I-, Current		Full	-	-	15	-	-	18	mA

NOTES:

3. V_{DD}/LLS pin = open or grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS compatibility.
4. At temperatures above 90^oC, care must be taken to assure V_{IN} remains at least 1.0V below the V_{SUPPLY} for proper operation.
5. V_{IN} = ±10V, I_{OUT} = -100µA.
6. V_{IN} = 0V, C_L = 100pF, enable input pulse = 3V, f = 500kHz.
7. C_L = 40pF, R_L = 1K, V_{EN} = 0.8V, V_{IN} = $3V_{RMS}$, f = 500kHz. Due to the pin to pin capacitance between IN 8/4B and OUT B, channel 8/4B exhibits 60dB of OFF isolation under the above test conditions.

Test Circuits and Waveforms V_{DD}/LLS = GND, Unless Otherwise Specified

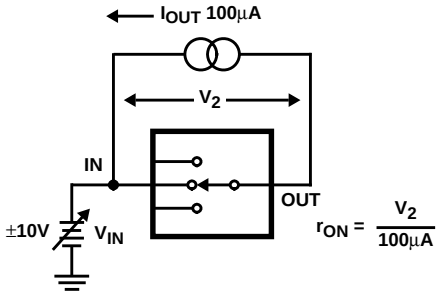


FIGURE 1. ON RESISTANCE TEST CIRCUIT

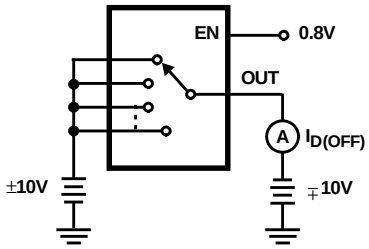


FIGURE 2. $I_{D(OFF)}$ TEST CIRCUIT (NOTE 8)

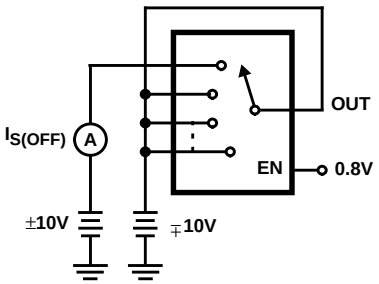


FIGURE 3. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 8)

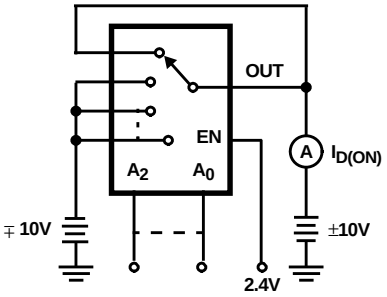


FIGURE 4. $I_{D(ON)}$ TEST CIRCUIT (NOTE 8)

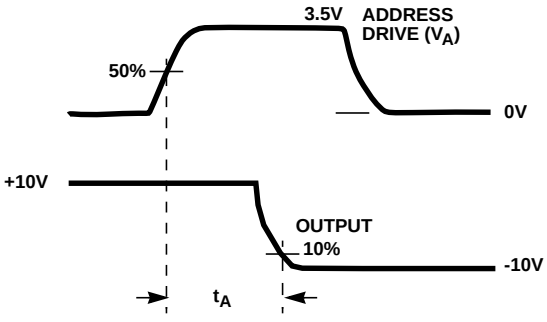


FIGURE 5A. MEASUREMENT POINTS

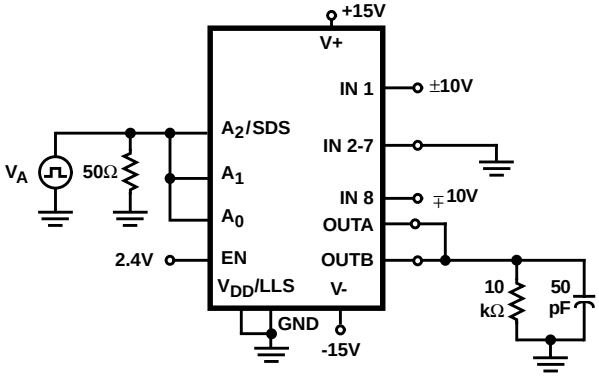


FIGURE 5B. TEST CIRCUIT

FIGURE 5. ACCESS TIME

NOTE:

8. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V.)

Test Circuits and Waveforms V_{DD}/LLS = GND, Unless Otherwise Specified **(Continued)**

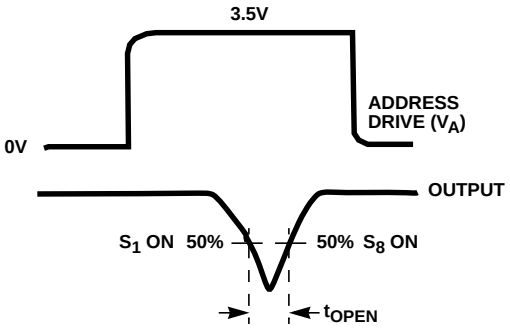


FIGURE 6A. MEASUREMENT POINTS

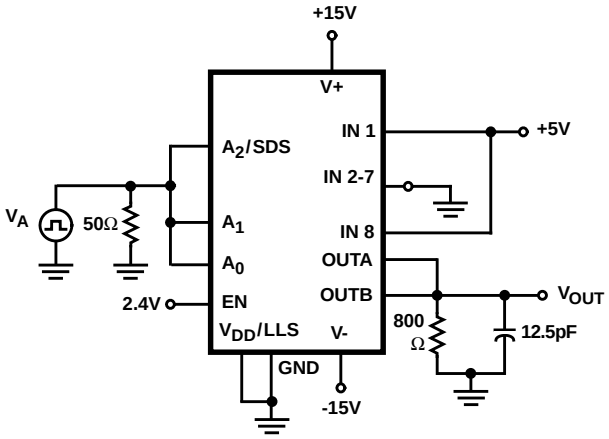


FIGURE 6B. TEST CIRCUIT

FIGURE 6. BREAK-BEFORE-MAKE DELAY

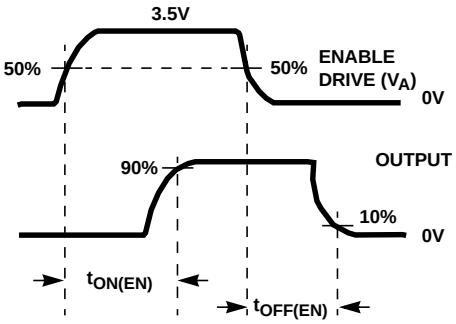


FIGURE 7A. MEASUREMENT POINTS

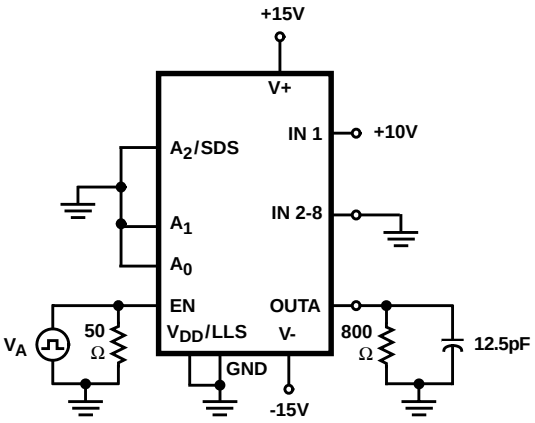


FIGURE 7B. TEST CIRCUIT

FIGURE 7. ENABLE DELAY

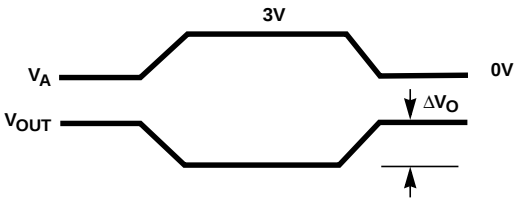


FIGURE 8A. MEASUREMENT POINTS

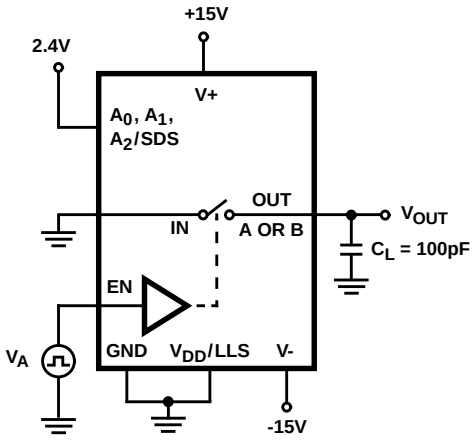


FIGURE 8B. TEST CIRCUIT

ΔV_O is the measured voltage error due to charge injection. The error in coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 8. CHARGE INJECTION

Die Characteristics

DIE DIMENSIONS:

89 mils x 93 mils

METALLIZATION:

Type: AlCu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE)**:**

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1.0kÅ
Silox Thickness: 12kÅ ±2.0kÅ

WORST CASE CURRENT DENSITY:

1.43×10^5 A/cm^2

TRANSISTOR COUNT:

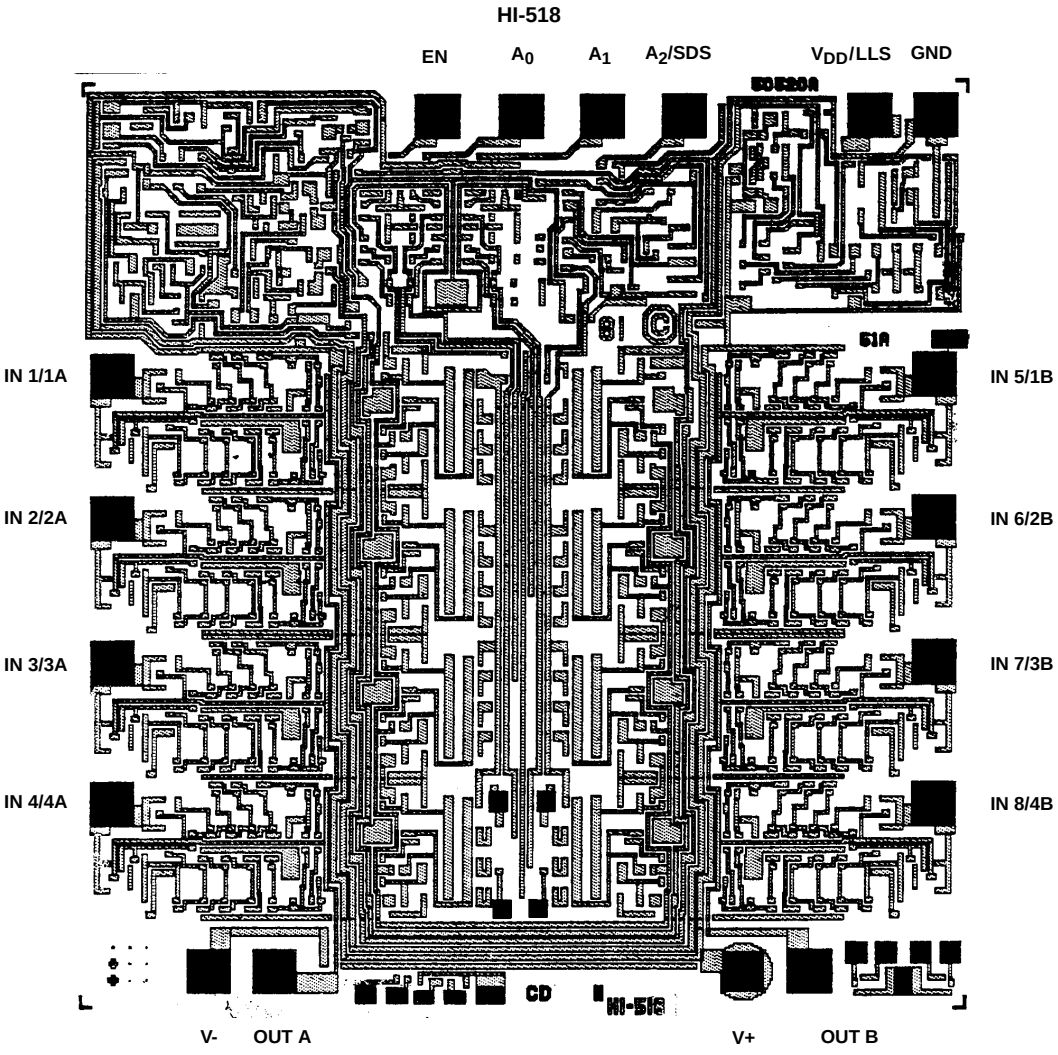
356

PROCESS:

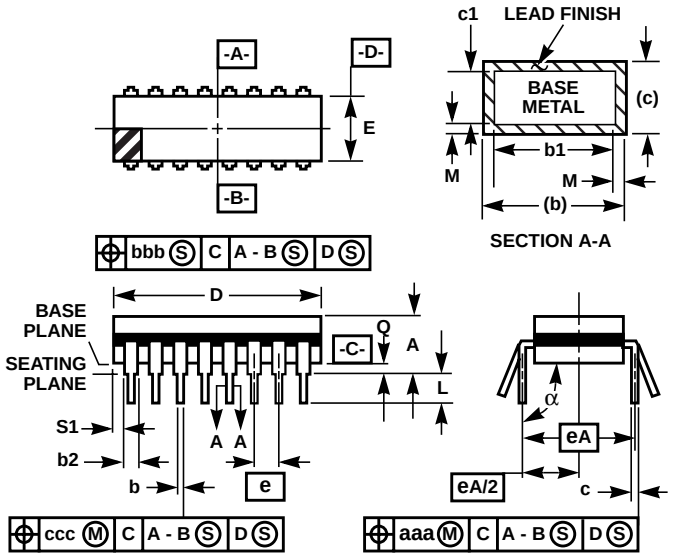
CMOS-DI

NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layout



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

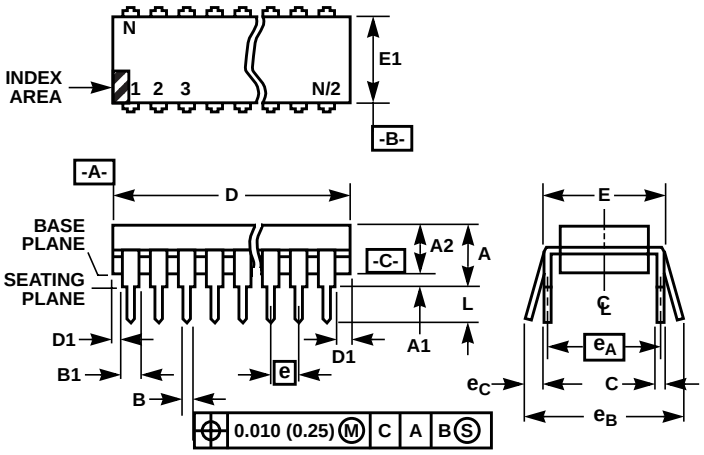
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F18.3 MIL-STD-1835 GDIP1-T18 (D-6, CONFIGURATION A)
18 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.960	-	24.38	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	18		18		8

Rev. 0 4/94

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E18.3 (JEDEC MS-001-BC ISSUE D)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.845	0.880	21.47	22.35	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	18		18		9

Rev. 0 12/93

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