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# HM62864 Series

65536-word  $\times$  8-bit High Speed CMOS Static RAM

# HITACHI

ADE-203-255B (Z)

Rev. 2.0

Jul. 4, 1995

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## Description

The Hitachi HM62864 is a CMOS static RAM organized 64-kword  $\times$  8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8  $\mu$ m Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. The device, packaged in a 525-mil SOP (460-mil body SOP) and a 8  $\times$  20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards.

## Features

- High speed
  - Fast access time: 55/70/85 ns (max)
- Low power
  - Active: 50 mW (typ) (f = 1 MHz)
  - Standby: 2  $\mu$ W (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Capability of battery backup operation
  - 2 chip selection for battery backup

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## HM62864 Series

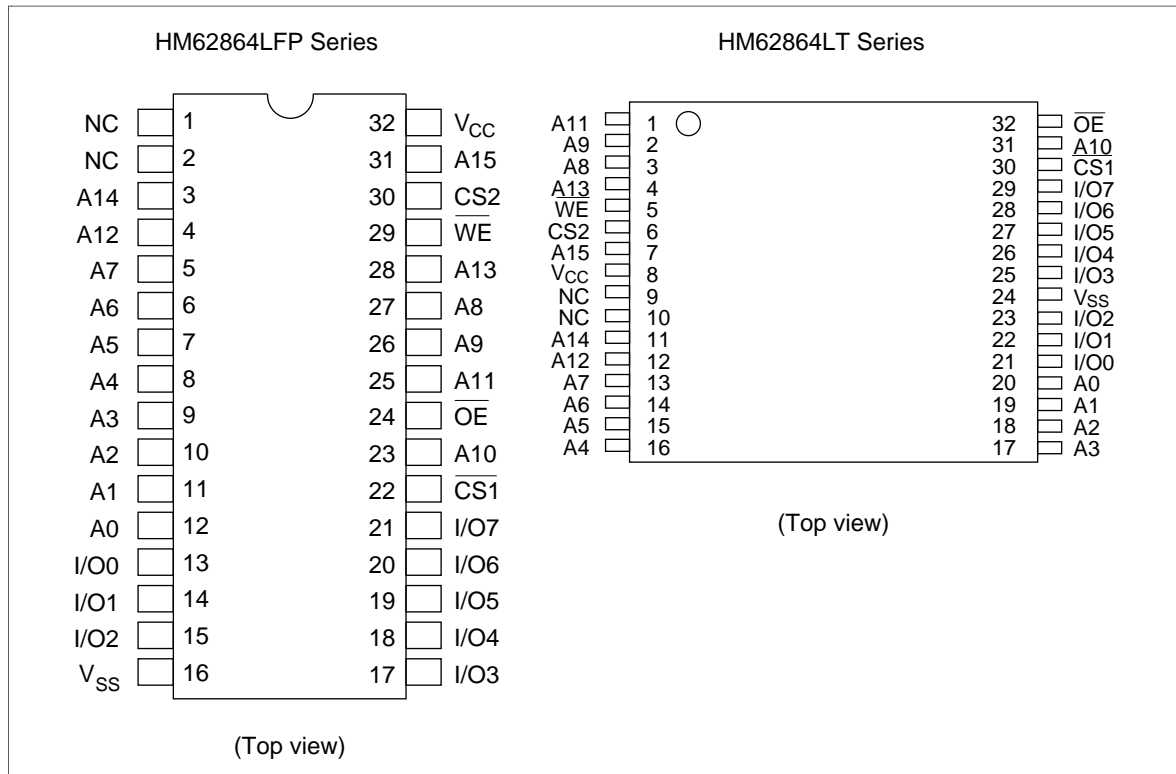
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### Ordering Information

Type No.	Access Time	Package
HM62864LFP-7	70 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62864LFP-8	85 ns	
HM62864LFP-5SL	55 ns	
HM62864LFP-7SL	70 ns	
HM62864LFP-8SL	85 ns	
HM62864LT-7	70 ns	8 mm × 20 mm 32-pin TSOP (normal type) (TFP-32D)
HM62864LT-8	85 ns	
HM62864LT-5SL	55 ns	
HM62864LT-7SL	70 ns	
HM62864LT-8SL	85 ns	

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## Pin Arrangement

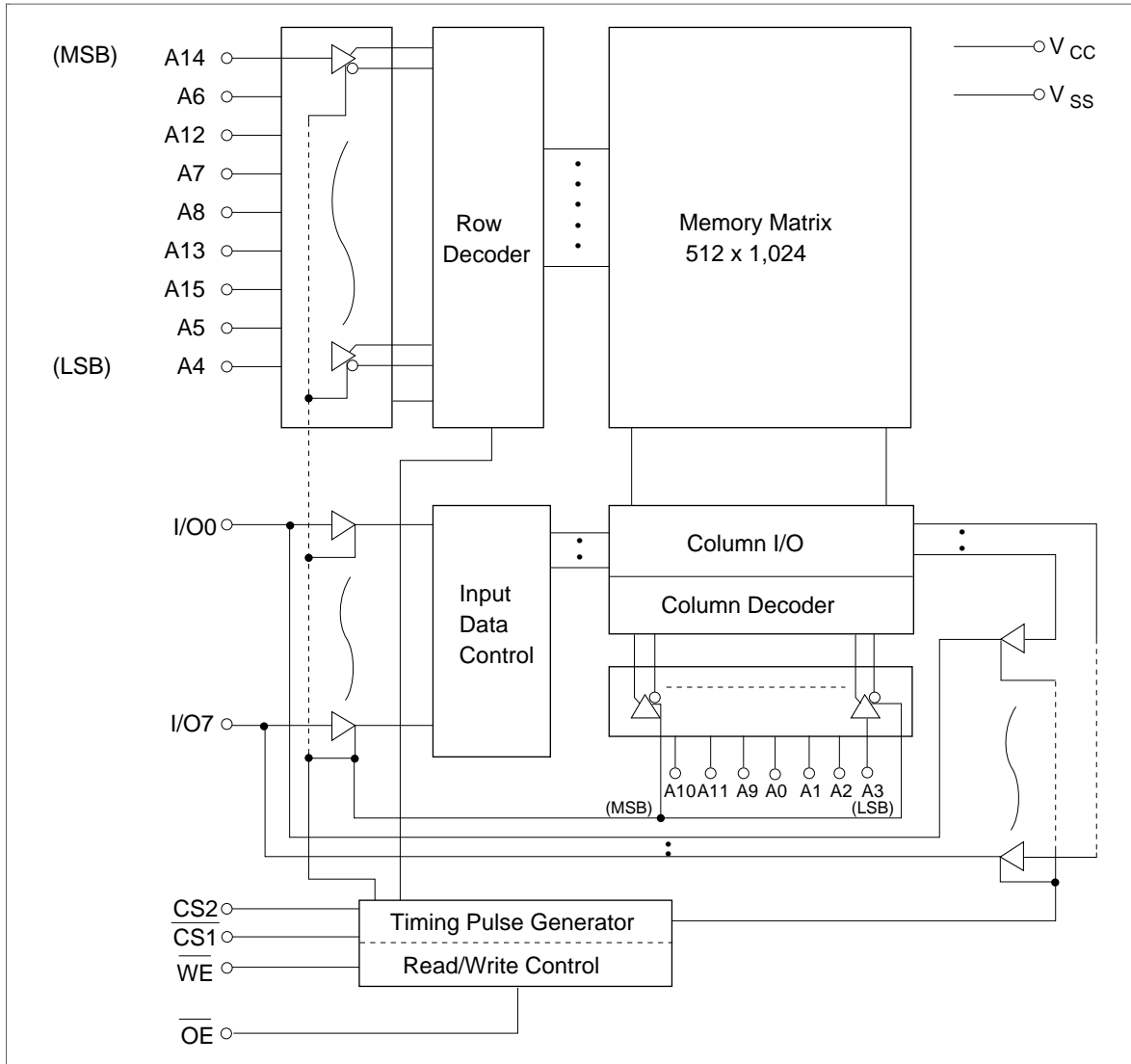


## Pin Description

Pin Name	Function
A0 to A15	Address
I/O0 to I/O7	Input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
NC	No connection
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

# HM62864 Series

## Block Diagram



**Function Table**

$\overline{\text{CS1}}$	$\text{CS2}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	$V_{\text{CC}}$ Current	I/O Pin	Ref. Cycle
H	X	X	X	Not selected	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
X	L	X	X	Not selected	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
L	H	H	H	Output disable	$I_{\text{CC}}$	High-Z	—
L	H	L	H	Read	$I_{\text{CC}}$	Dout	Read cycle (1) to (3)
L	H	H	L	Write	$I_{\text{CC}}$	Din	Write cycle (1)
L	H	L	L	Write	$I_{\text{CC}}$	Din	Write cycle (2)

Note: X: High or Low

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Power supply voltage <sup>1</sup>	$V_{\text{CC}}$	-0.5 to +7.0	V
Terminal voltage <sup>1</sup>	$V_{\text{T}}$	-0.5 <sup>2</sup> to $V_{\text{CC}} + 0.3$ <sup>3</sup>	V
Power dissipation	$P_{\text{T}}$	1.0	W
Operating temperature	$T_{\text{opr}}$	0 to +70	°C
Storage temperature	$T_{\text{stg}}$	-55 to +125	°C
Storage temperature under bias	$T_{\text{bias}}$	-10 to +85	°C

Notes: 1. Relative to  $V_{\text{SS}}$

2.  $V_{\text{T}}$  min: -3.0 V for pulse half-width  $\leq$  50 ns

3. Maximum voltage is 7.0V

**Recommended DC Operating Conditions ( $T_{\text{a}} = 0$  to +70°C)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{\text{CC}}$	4.5	5.0	5.5	V
	$V_{\text{SS}}$	0	0	0	V
Input high (logic 1) voltage	$V_{\text{IH}}$	2.2	—	$V_{\text{CC}} + 0.3$	V
Input low (logic 0) voltage	$V_{\text{IL}}$	-0.3 <sup>1</sup>	—	0.8	V

Note: 1.  $V_{\text{IL}}$  min: -3.0 V for pulse half-width  $\leq$  50 ns

## HM62864 Series

### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ±10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test conditions	
Input leakage current	I <sub>LI</sub>	—	—	1	μA	V <sub>SS</sub> ≤ Vin ≤ V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	—	—	1	μA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>CC</sub>	
Operating power supply current	I <sub>CC</sub>	—	10	15	mA	$\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA	
Average operating power supply current	HM62864-5	I <sub>CC1</sub>	—	55	70	mA	Min cycle, duty = 100%, $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> ,
	HM62864-7	I <sub>CC1</sub>	—	55	70		Others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA
	HM62864-8	I <sub>CC1</sub>	—	45	60		
		I <sub>CC2</sub>	—	10	15	mA	Cycle time = 1 μs, duty = 100%, I <sub>I/O</sub> = 0 mA, $\overline{CS1} \leq V_{IL}$ , CS2 ≥ V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub> , V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V, 0 V ≤ V <sub>IL</sub> ≤ 0.2 V
Standby power supply current	I <sub>SB</sub>	—	0.7	3	mA	(1) or (2) (1) $\overline{CS1} = V_{IH}$ , CS2 = V <sub>IH</sub> (2) CS2 = V <sub>IL</sub>	
	I <sub>SB1</sub>	—	0.4	100	μA	0 V ≤ Vin ≤ V <sub>CC</sub> (1) or (2) (1) $\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V <sub>CC</sub> - 0.2V	
	I <sub>SB1</sub>	—	0.4	50 <sup>-2</sup>		(2) 0 V ≤ CS2 ≤ 0.2 V	
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1 mA	
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1.0 mA	

Notes: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and not guaranteed.  
2. This characteristics is guaranteed only for SL version.

### Capacitance (Ta = 25°C, f = 1.0 MHz)<sup>\*1</sup>

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C <sub>in</sub>	—	—	5	pF	Vin = 0 V
Input/output capacitance	C <sub>I/O</sub>	—	—	8	pF	V <sub>I/O</sub> = 0 V

Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics** (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, unless otherwise noted.)

**Test Conditions**

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: HM62864-5: 1 TTL + 30 pF (Including scope & jig)  
HM62864-7/8: 1 TTL + 100 pF (Including scope & jig)

**Read Cycle**

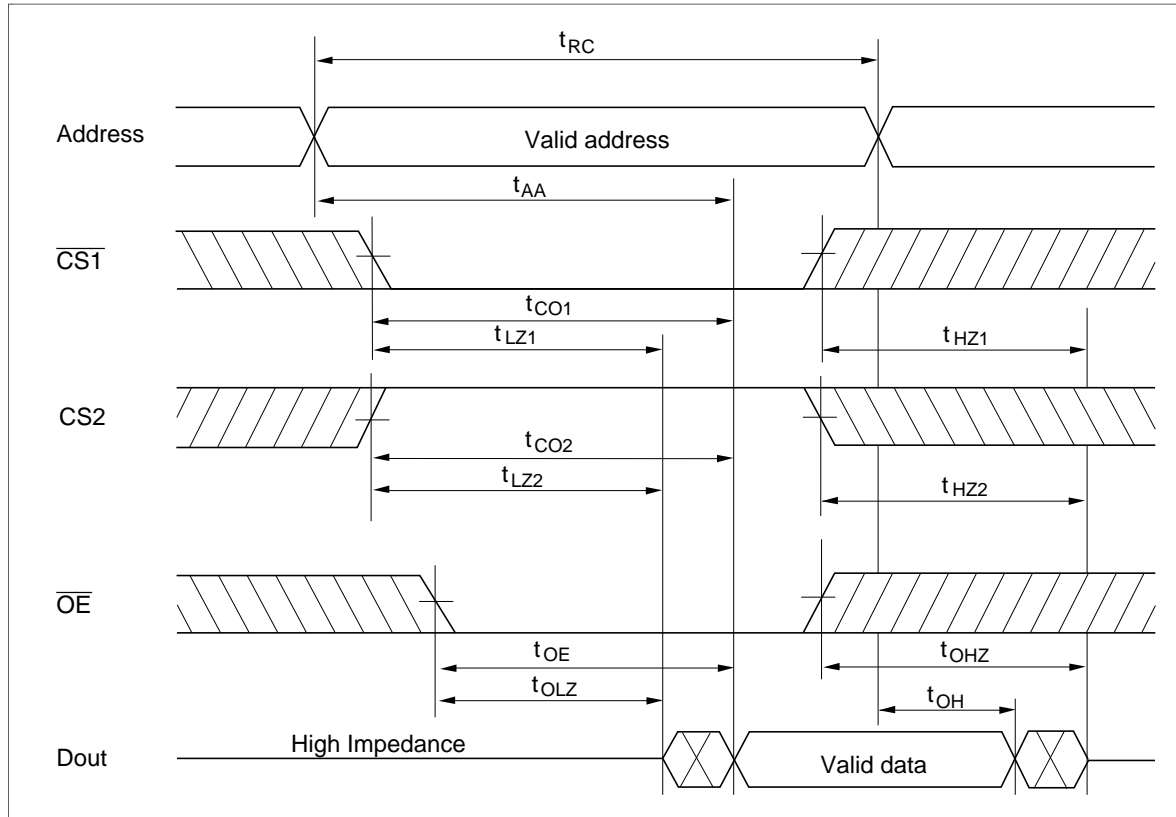
Parameter	Symbol	HM62864-5		HM62864-7		HM62864-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read cycle time	t <sub>RC</sub>	55	—	70	—	85	—	ns	
Address access time	t <sub>AA</sub>	—	55	—	70	—	85	ns	
Chip select access time	$\overline{\text{CS1}}$ t <sub>CO1</sub>	—	55	—	70	—	85	ns	
	CS2 t <sub>CO2</sub>	—	55	—	70	—	85	ns	
Output enable to output valid	t <sub>OE</sub>	—	30	—	40	—	45	ns	
Chip selection to output in low-Z	$\overline{\text{CS1}}$ t <sub>LZ1</sub>	5	—	10	—	10	—	ns	2
low-Z	CS2 t <sub>LZ2</sub>	5	—	10	—	10	—	ns	2
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	5	—	ns	2
Chip deselection in output in high-Z	$\overline{\text{CS1}}$ t <sub>HZ1</sub>	0	20	0	25	0	30	ns	1, 2
high-Z	CS2 t <sub>HZ2</sub>	0	20	0	25	0	30	ns	1, 2
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	0	25	0	30	ns	1, 2
Output hold from address change	t <sub>OH</sub>	5	—	10	—	10	—	ns	

Notes: 1. t<sub>HZ</sub> and t<sub>OHZ</sub> are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

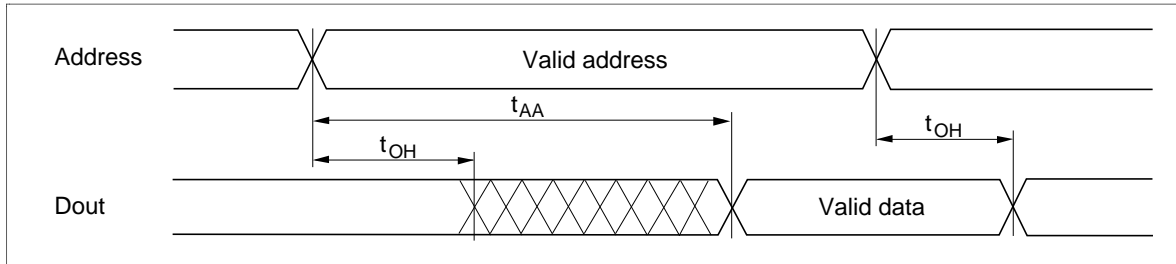
# HM62864 Series

## Read Timing Waveform (1) ( $\overline{WE} = V_{IH}$ )

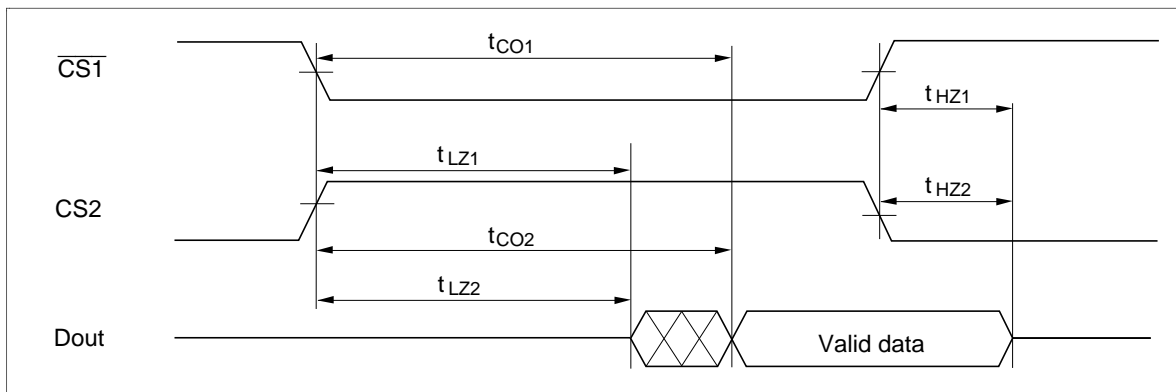




Read Timing Waveform (2) ( $\overline{WE} = V_{IH}$ )



Read Timing Waveform (3) ( $\overline{WE} = V_{IH}$ )



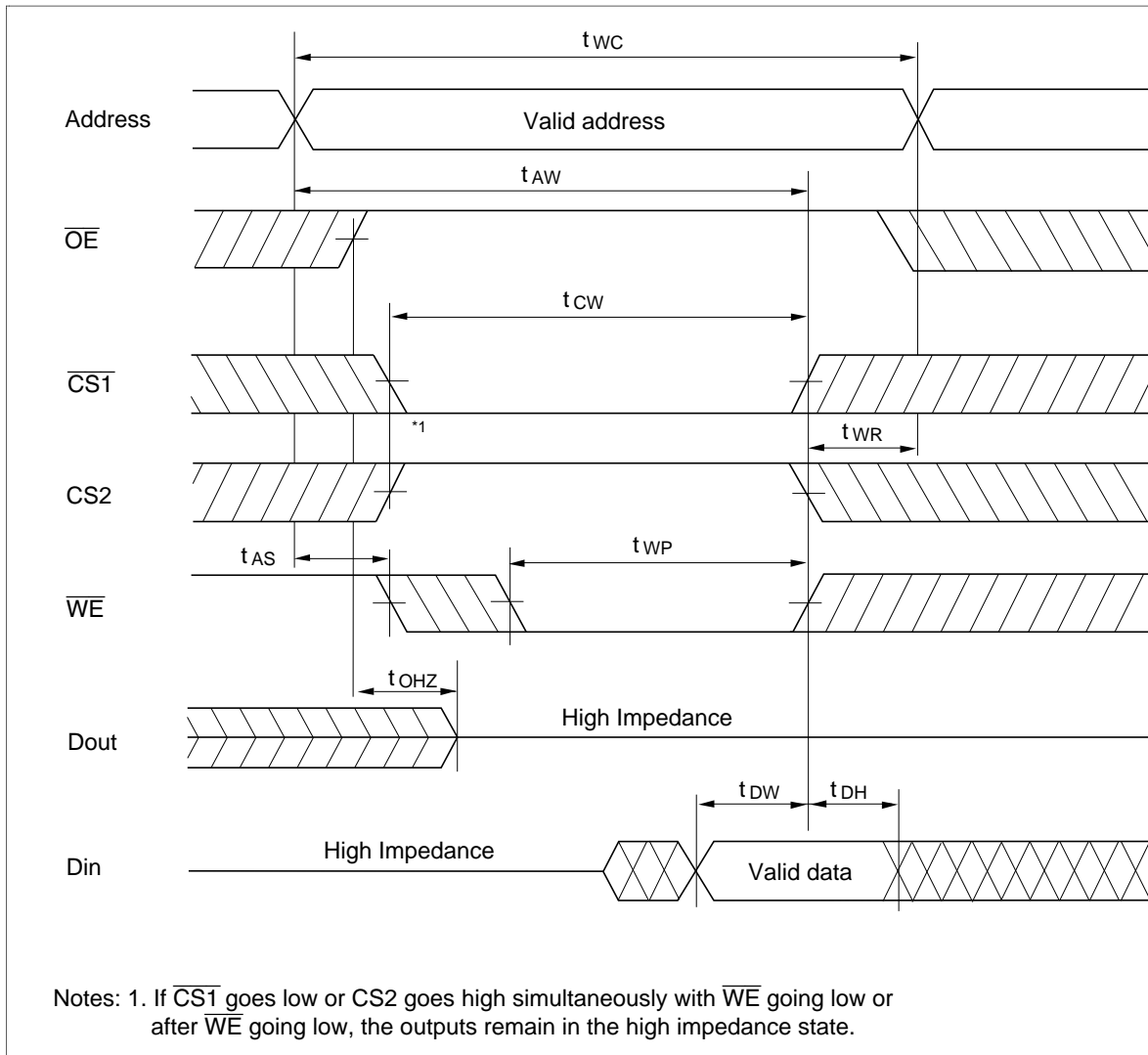
## HM62864 Series

### Write Cycle

Parameter	Symbol	HM62864-5		HM62864-7		HM62864-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	55	—	70	—	85	—	ns	
Chip selection to end of write	$t_{CW}$	50	—	60	—	75	—	ns	4
Address setup time	$t_{AS}$	0	—	0	—	0	—	ns	5
Address valid to end of write	$t_{AW}$	50	—	60	—	75	—	ns	
Write pulse width	$t_{WP}$	40	—	50	—	55	—	ns	3, 8
Write recovery time	$t_{WR}$	0	—	0	—	0	—	ns	6
Write to output in high-Z	$t_{WHZ}$	0	20	0	25	0	30	ns	1, 2, 7
Data to write time overlap	$t_{DW}$	30	—	30	—	35	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	0	30	ns	1, 2, 7

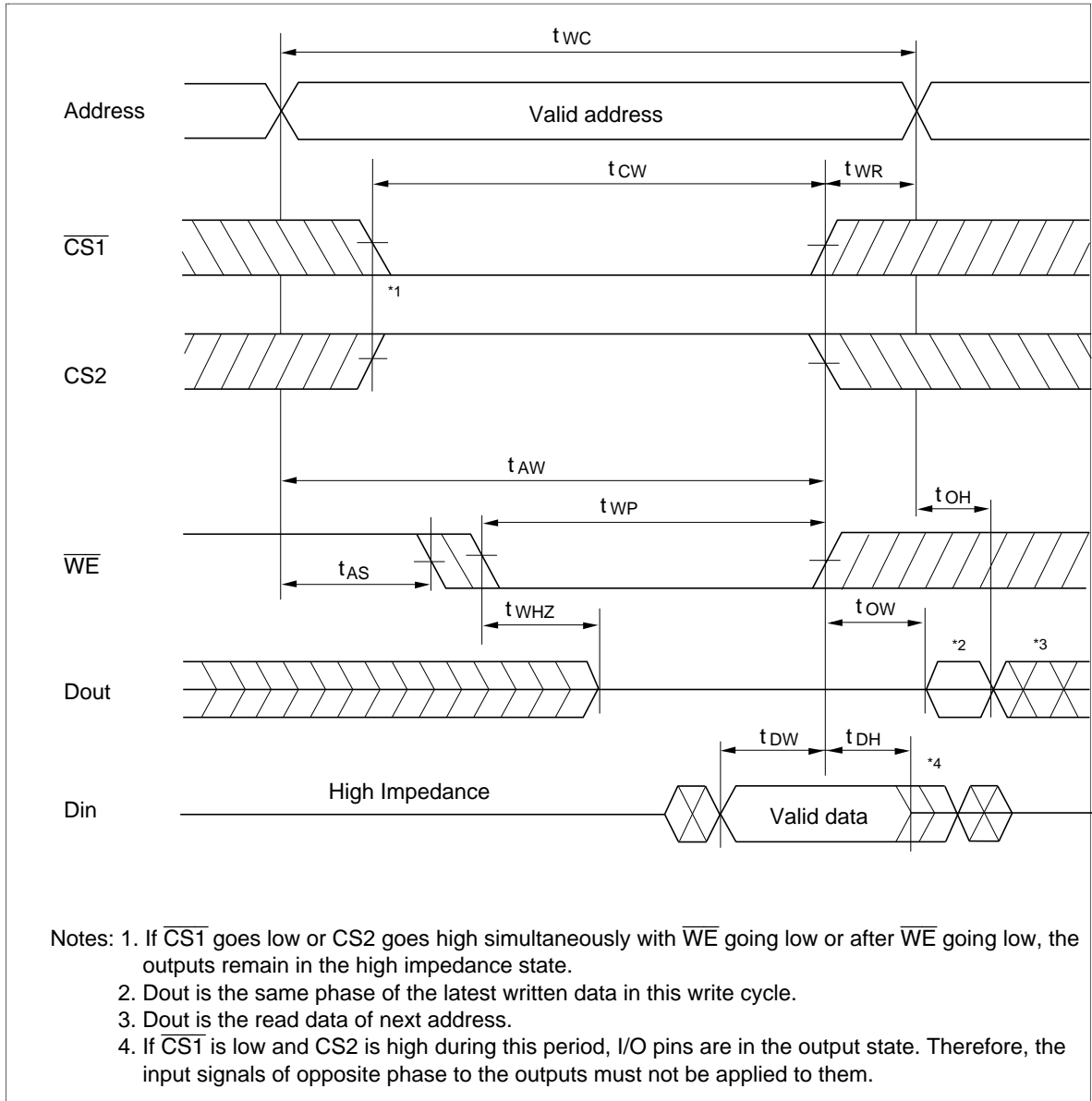
- Notes:
- $t_{WHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  - This parameter is sampled and not 100% tested.
  - A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2 and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high, and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low, and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  - $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or CS2 going high to the end of write.
  - $t_{AS}$  is measured from the address valid to the beginning of write.
  - $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going low to the end of write cycle.
  - During this period, I/O pin are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
  - In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention,  $t_{WP} \geq t_{WHZ} \max + t_{DW} \min$ .

Write Timing Waveform (1) ( $\overline{OE}$  Clock)



# HM62864 Series

## Write Timing Waveform (2) ( $\overline{OE}$ Low Fixed)



- Notes:
1. If  $\overline{CS1}$  goes low or CS2 goes high simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in the high impedance state.
  2. Dout is the same phase of the latest written data in this write cycle.
  3. Dout is the read data of next address.
  4. If  $\overline{CS1}$  is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

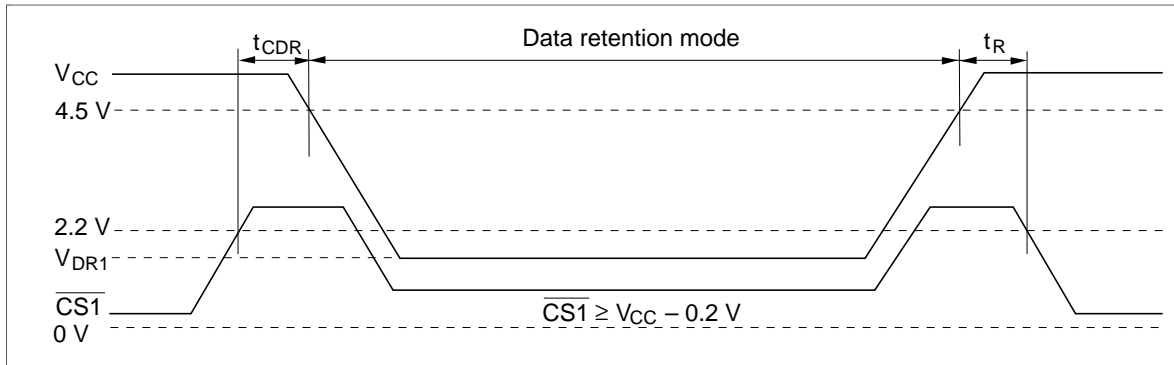
**Low  $V_{CC}$  Data Retention Characteristics ( $T_a = 0$  to  $+70^\circ\text{C}$ )**

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test conditions <sup>*5</sup>
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	5.5	V	$0\text{ V} \leq V_{in} \leq V_{CC}$ , (1) or (2) (1) $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$ , $CS2 \geq V_{CC} - 0.2\text{ V}$ (2) $0\text{ V} \leq CS2 \leq 0.2\text{ V}$
Data retention current	$I_{CCDR}$	—	0.1	$30^{-2}$	$\mu\text{A}$	$V_{CC} = 3.0\text{ V}$ , $0\text{ V} \leq V_{in} \leq V_{CC}$ , (1) or (2) (1) $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$ , $CS2 \geq V_{CC} - 0.2\text{ V}$ (2) $0\text{ V} \leq CS2 \leq 0.2\text{ V}$
	$I_{CCDR}$	—	0.1	$10^{-3}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$t_{RC}^{*4}$	—	—	ns	

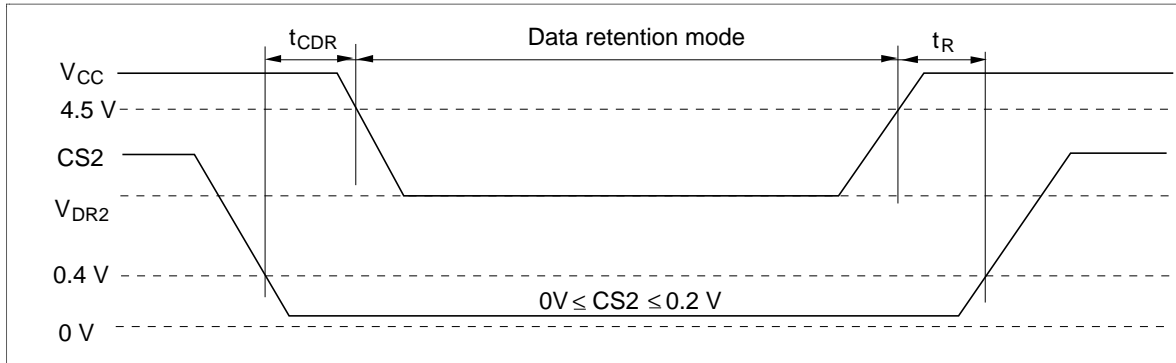
- Notes: 1. Typical values are at  $V_{CC} = 3.0\text{ V}$ ,  $T_a = 25^\circ\text{C}$  and not guaranteed.  
 2.  $10\ \mu\text{A}$  max at  $T_a = 0$  to  $40^\circ\text{C}$ .  
 3. This characteristics guaranteed for only L-SL version.  $3\ \mu\text{A}$  max at  $T_a = 0$  to  $40^\circ\text{C}$ .  
 4.  $t_{RC}$  = Read cycle time.  
 5.  $\overline{CS2}$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{CS1}$  buffer,  $\overline{OE}$  buffer, and  $D_{in}$  buffer. If  $\overline{CS2}$  controls data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{CS1}$ , I/O) can be in the high impedance state. If  $\overline{CS1}$  controls data retention mode,  $\overline{CS2}$  must be  $\overline{CS2} \geq V_{CC} - 0.2\text{ V}$  or  $0\text{ V} \leq \overline{CS2} \leq 0.2\text{ V}$ . The other input levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.

**Low  $V_{CC}$  Data Retention Timing Waveform (1) ( $\overline{CS1}$  Controlled)**



# HM62864 Series

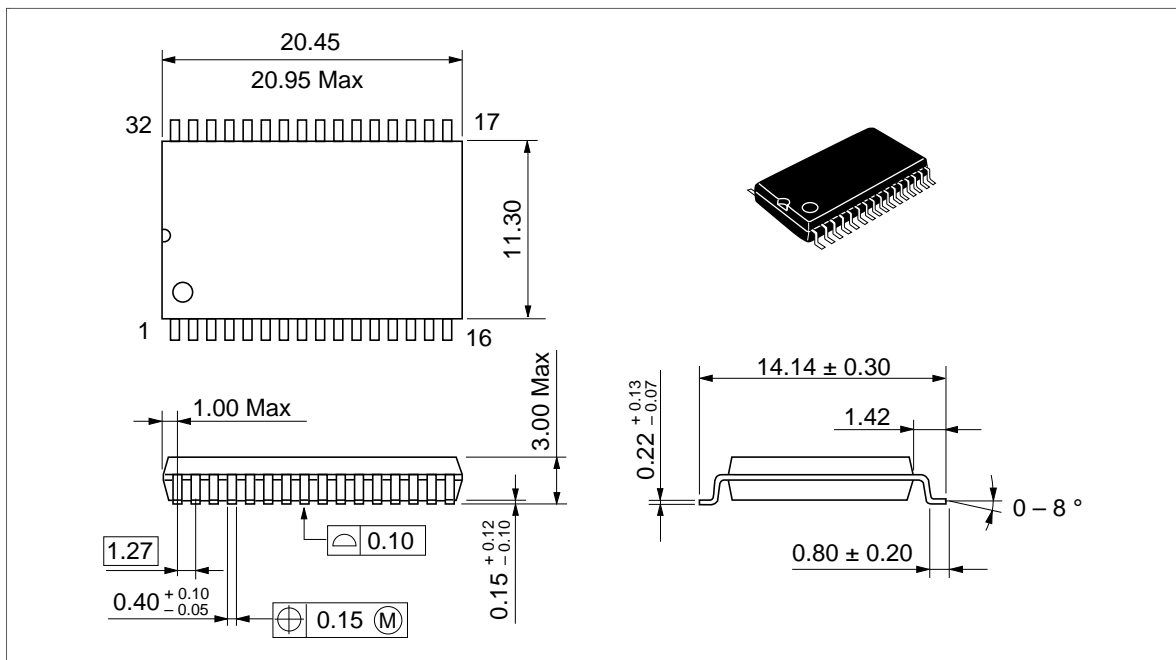
## Low $V_{CC}$ Data Retention Timing Waveform (2) (CS2 Controlled)



## Package Dimensions

### HM62864LFP Series (FP-32D)

Unit: mm



# HM62864 Series

HM62864LT Series (TFP-32D)

Unit: mm

