

Integrated Device Technology, Inc.

FAST CMOS DUAL 1-OF-4 DECODER WITH ENABLE

IDT54/74FCT139
IDT54/74FCT139A
IDT54/74FCT139C

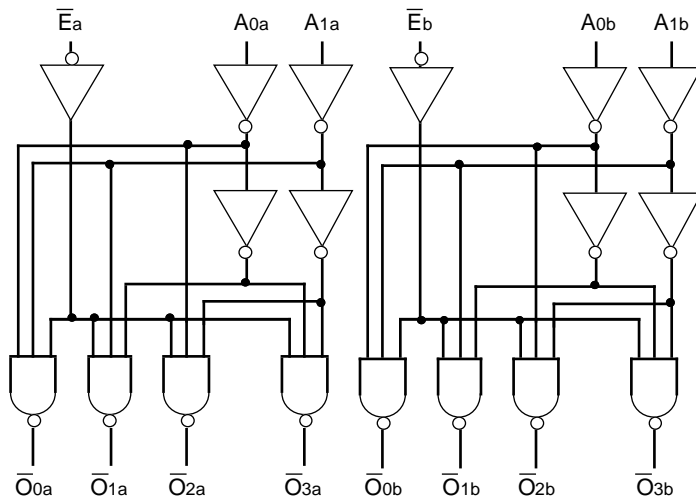
FEATURES:

- IDT54/74FCT139 equivalent to FAST™ speed
- **IDT54/74FCT139A 35% faster than FAST**
- **IDT54/74FCT139C 45% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- $I_{OL} = 48\text{mA}$ (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST ($5\mu\text{A}$ max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

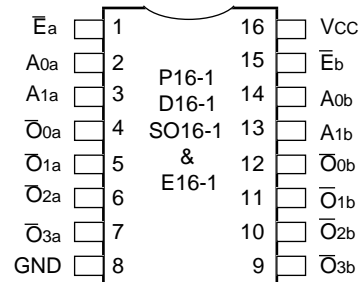
The IDT54/74FCT139/A/C are dual 1-of-4 decoders built using an advanced dual metal CMOS technology. These devices have two independent decoders, each of which accept two binary weighted inputs (A_0 - A_1) and provide four mutually exclusive active LOW outputs (\bar{O}_0 - \bar{O}_3). Each decoder has an active LOW enable (\bar{E}). When \bar{E} is HIGH, all outputs are forced HIGH.

FUNCTIONAL BLOCK DIAGRAM



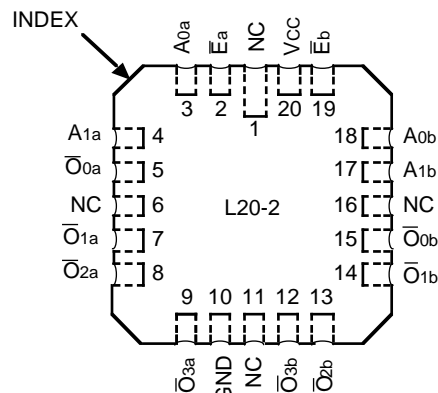
2605 cnv* 03

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

2605 cnv* 01



LCC
TOP VIEW

2605 cnv* 02

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FAST is a trademark of National Semiconductor Co.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

TRUTH TABLE⁽¹⁾

Inputs			Outputs			
\bar{E}	A ₀	A ₁	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

NOTE:

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- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC}	-0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

PIN DESCRIPTION

Pin Names	Description
A ₀ , A ₁	Address Inputs
\bar{E}	Enable Input (Active LOW)
$\bar{O}_0 - \bar{O}_3$	Outputs (Active LOW)

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CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

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- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	μA
			$V_I = 2.7V$	—	—	5 ⁽⁴⁾	
I_{IL}	Input LOW Current		$V_I = 0.5V$	—	—	-5 ⁽⁴⁾	
			$V_I = \text{GND}$	—	—	-5	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$	—	-0.7	-1.2	V	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = \text{GND}$	-60	-120	—	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$	V_{HC}	V_{CC}	—	V	
		$V_{CC} = \text{Min.}$	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}		—
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3		—
		$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3	—		
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$	—	GND	V_{LC}	V	
		$V_{CC} = \text{Min.}$	$I_{OL} = 300\mu A$	—	GND		$V_{LC}^{(4)}$
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 32mA \text{ MIL.}$	—	0.3		0.5
		$I_{OL} = 48mA \text{ COM'L.}$	—	0.3	0.5		

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.3	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _o = 10MHz 50% Duty Cycle One Output Toggling	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	1.7	4.5	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2.0	5.5	
		V _{CC} = Max. Outputs Open f _o = 10MHz 50% Duty Cycle One Output Toggling on Each Decoder	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	3.2	7.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	3.7	9.5 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_o N_o)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_o = Output Frequency
 N_o = Number of Outputs at f_o
 All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Condition ⁽¹⁾	IDT54/74FCT139		IDT54/74FCT139A				IDT54/74FCT139C				Unit		
			Com'l.		Mil.		Com'l.		Mil.		Com'l.			Mil.	
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.		Min. ⁽²⁾	Max.
t _{PLH} t _{PHL}	Propagation Delay A ₀ or A ₁ to \bar{O}_n	C _L = 50pF R _L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.9	1.5	7.8	1.5	5.0	1.5	6.2	ns
t _{PLH} t _{PHL}	Propagation Delay \bar{E} to \bar{O}_n		1.5	8.0	1.5	9.0	1.5	5.5	1.5	7.2	1.5	4.8	1.5	5.8	ns

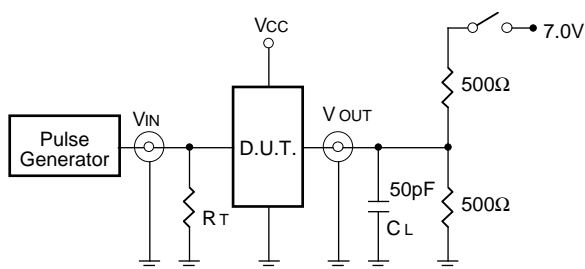
NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

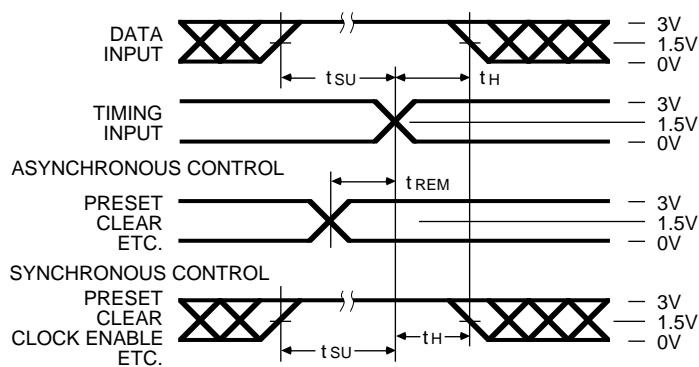
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

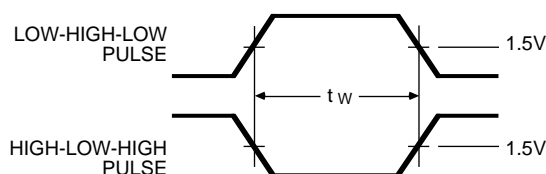
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

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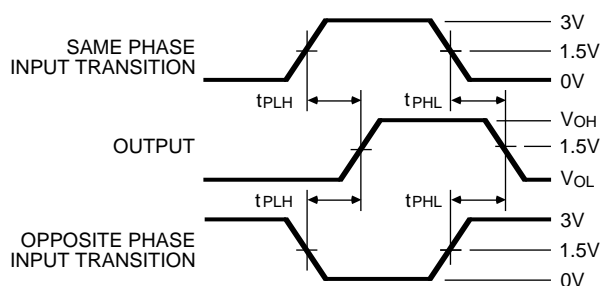
SET-UP, HOLD AND RELEASE TIMES



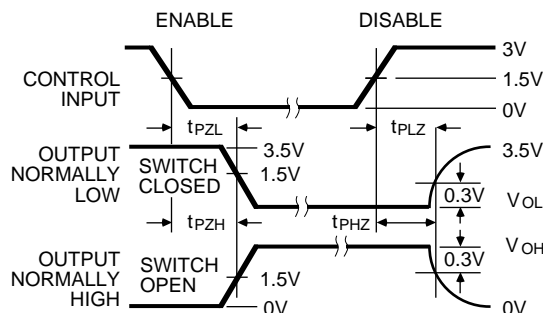
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

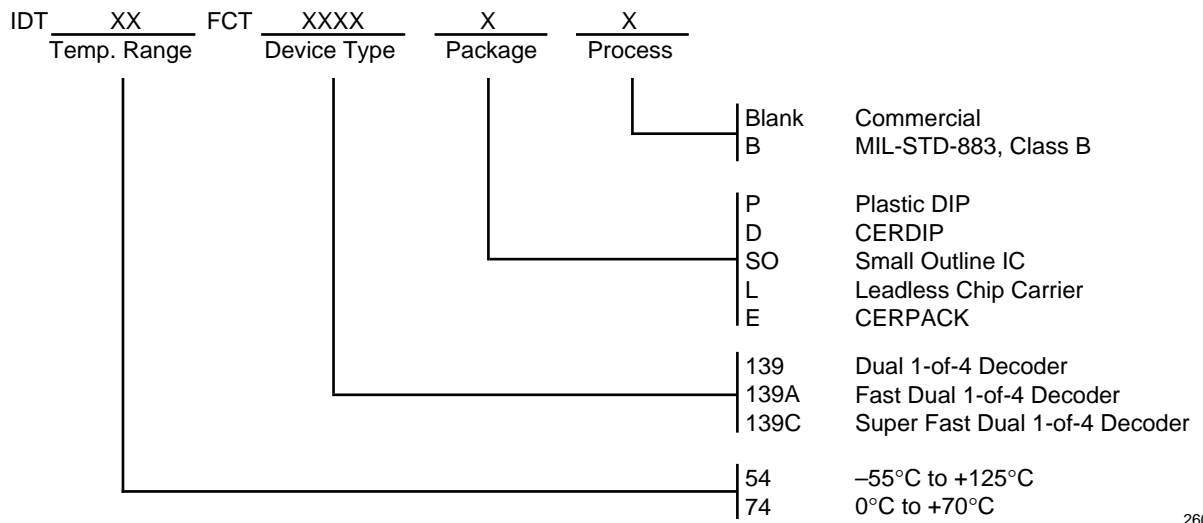


NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_o \leq 50\Omega$; $t_f \leq 2.5$ ns; $t_r \leq 2.5$ ns.

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ORDERING INFORMATION



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