Ordering number: EN5225

Monolithic Digital IC

LB1896

3-phase Brushless Motor Driver for CD-ROM Spindle Drive Use

Overview

The LB1896 is a 3-phase brushless motor driver IC that is ideal for driving CD-ROM spindle motors.

Functions and Features

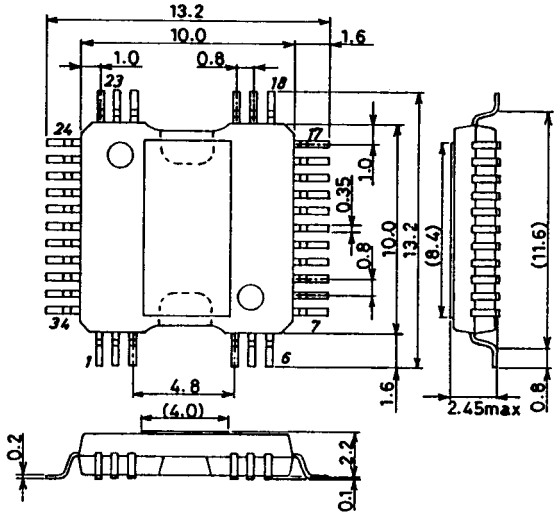
- 120 ° voltage linear technique
- V-type control voltage
- Switchable control gain
- Control, noncontrol, acceleration/deceleration mode select pins built in.
- Start/Stop pin built in, Hall bias built in.

Package Dimensions

unit : mm

3219-QFP34H-C

[LB1896]



SANYO : QFP34H – C

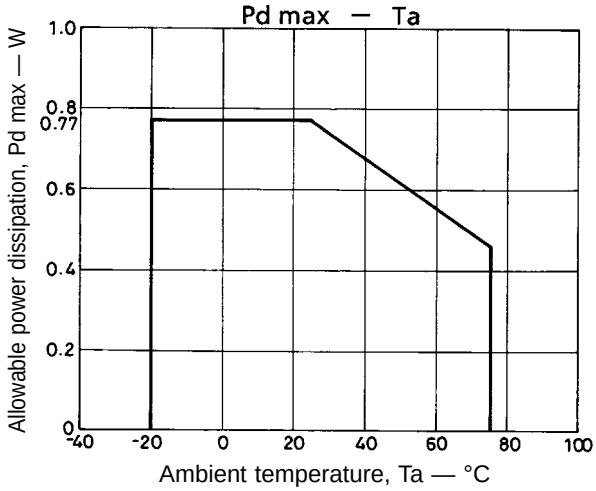
Specifications

Absolute Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}1$ max		20	V
	$V_{CC}2$ max		7.0	V
Applied output voltage	$V_{OU, V, W}$		20	V
Output current	I_{OUT}		1.2	A
Allowable power dissipation	Pd max	Independent IC	0.77	W
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +150	°C

Operating Conditions at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}1$		5 to 18	V
	$V_{CC}2$	$V_{CC}1 \geqq V_{CC}2$	4.3 to 6.5	V
V_{Cref} input voltage	V_{Cref}		$V_{CC}2/2 \pm 1.0$	V
V_{NS} input voltage	V_{NS}		0 to $V_{CC}2 - 1.0$	V



Electrical Characteristics at Ta = 25 °C, $V_{CC}1$ = 12 V, $V_{CC}2$ = 5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply current 1	$I_{CC}1$	V_C = open, V_{Cref} = open, R_L = ∞, $V_{S/S}$ = 5 V		17	30	mA
Supply current 2	$I_{CC}2$	V_C = open, V_{Cref} = open		7.5	10.5	mA
Supply current 3	$I_{CC}3$	V_C = open, V_{Cref} = open, R_L = ∞, $V_{S/S}$ = 0 V, (I_{CC} of $V_{CC}1$)		0.9	3	mA
[Drive block]						
Output saturation voltage	$V_{O(sat)}1$	I_{OUT} = 0.4 A, sink + source		1.6	2.2	V
	$V_{O(sat)}2$	I_{OUT} = 0.8 A, sink + source		2.0	3.0	V
Output TRS sustaining voltage	$V_{O(sus)}$	I_{OUT} = 20 mA	20			V
Output static voltage	V_{OQ}	V_C = 2.5 V, V_{Cref} = 2.5 V	5.7	6.0	6.3	V
Hall amplifier input offset voltage	$V_{H\ offset}$		–5		+5	mV
Hall amplifier input bias current	$I_{H\ bias}$			1	5	µA
Hall amplifier common-mode input voltage range	V_{Hch}		1.3		2.2	V
Hall input/output voltage gain	G_{VHO}		40	43	46	dB
Control/output drive gain 1	$G_{VCO}1$	RZ1 = RZ2, GC1 = L, GC2 = L	26	29		dB
Control/output channel difference 1	$\Delta G_{VCO}1$	RZ1 = RZ2, GC1 = L, GC2 = L	–1.5		+1.5	dB
Control/output drive gain 2	$G_{VCO}2$	RZ1 = RZ2, GC1 = L, GC2 = H	32	35		dB
Control/output channel difference 2	$\Delta G_{VCO}2$	RZ1 = RZ2, GC1 = L, GC2 = H	–1.9		+1.9	dB
Input dead zone voltage	V_{DZ}	RZ1 = RZ2, GC1 = L, GC2 = L V_O (voltage between out and out) = 0.1 V	±13	±38	±55	mV
Input bias current 1	$I_{B\ SERVO}$	V_C = 1.0 V			500	nA
Input bias current 2	$I_{B\ n.s}$	V_{NS} = 1.0 V			500	nA
S/S pin high voltage	$V_{S/S\ H}$	Input is CMOS level	4			V
S/S pin low voltage	$V_{S/S\ L}$	Note) S/S pin Vth = V_{CC}2/2			1	V
Gain control 1 high voltage	$V_{GC1\ H}$	Input is at CMOS level.	4			V
Gain control 1 low voltage	$V_{GC1\ L}$	Note) GC1 pin Vth = 2.0 V			1	V
Gain control 2 high voltage	$V_{GC2\ H}$	Input is at CMOS level.	4			V
Gain control 2 low voltage	$V_{GC2\ L}$	Note) GC2 pin Vth = 2.0 V			1	V
S/S pin input current	$I_{S/S}$	Input voltage = 5 V		50	100	µA
Gain control 1, 2 current	I_{GC}	Input voltage = 5 V		53	110	µA
Rotation output saturation voltage	$V_{(sat)\ H.FG}$	I_O = –5 mA		0.24	0.5	V
Rotation output saturation sustaining voltage	$V_{(sus)\ H.FG}$				7	V
Hall bias voltage	V_H±	I_O = 5 mA, R_H = 200 Ω	0.7	0.97	1.2	V
CTRL pin high voltage	$V_{CTRL\ H}$	Common for CTRL1 and CTRL2 input CMOS level	4			V
CTRL pin low voltage	$V_{CTRL\ L}$	Note) CTRL pin Vth = 2.5 V			1.0	V
CTRL input current	I_{CTRL}	Input voltage = 5 V		53	110	µA
TSD operation voltage	TSD	Design target	150	180	210	°C
TSD hysteresis	ΔTSD	Design target		15		°C

Note) Vth is a design target and not measured.

Mode Switching Truth Table

CTRL0	CTRL1	Mode
L	L	Control
L	H	Noncontrol
H	L	Acceleration
H	H	Deceleration

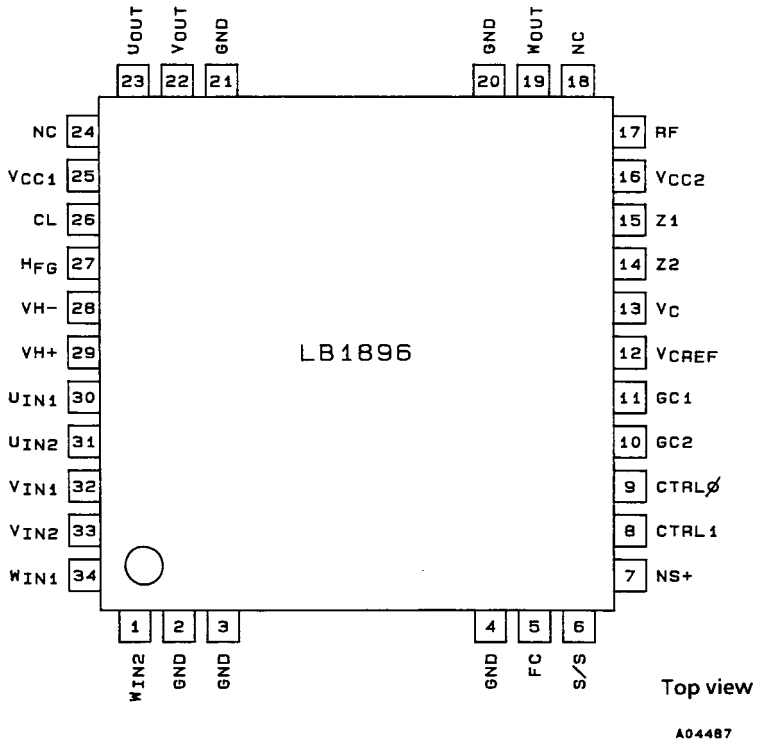
L = 0 to 1.0 V
H = 4.0 V or more

Hall Logic Truth Table

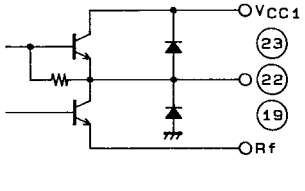
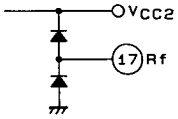
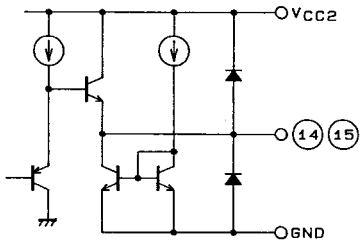
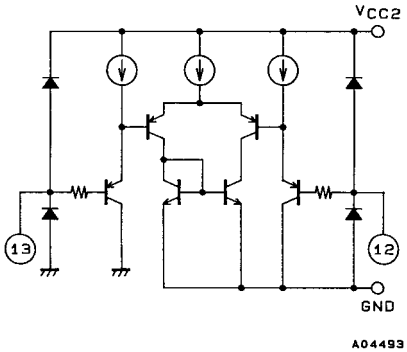
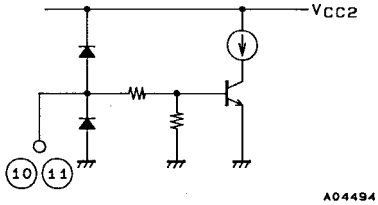
	Source → Sink	Hall input			F/R Control
		U_{IN}	V_{IN}	W_{IN}	
1	W → V V → W	H	H	L	Forward Reverse
2	W → U U → W	H	L	L	Forward Reverse
3	V → W W → V	L	L	H	Forward Reverse
4	U → V V → U	L	H	L	Forward Reverse
5	V → U U → V	H	L	H	Forward Reverse
6	U → W W → U	L	H	H	Forward Reverse

An input is considered to be HIGH when $U_{IN}1 > U_{IN}2$, $V_{IN}1 > V_{IN}2$, and $W_{IN}1 > W_{IN}2$ by 0.2 V or more.
Forward when $V_C > V_{Cref}$
Reverse when $V_C < V_{Cref}$

Pin Assignment



Pin Functions

Pin No.	Pin Name	Pin Voltage	Equivalent Circuit Diagram	Pin Function
3, 4 20, 21	Frame GND			Frame GND. GND must be shared.
2	GND			GND
23 22 19	U_{OUT} V_{OUT} W_{OUT}			Output pins. Motor connection
17	Rf			Output Tr GND. A resistor can be connected between this pin and GND to sense the output current as a voltage drop to provide for overcurrent protection.
18, 24	NC			Idle pins.
16	$V_{CC}2$	4.3 to 6.5 V		• Power supply for blocks other than the output block. • This supply should be kept stable to prevent ripple and noise from entering this pin.
15 14	Z1 Z2			• First-stage amplifier gain setting resistors. • Z1 and Z2 normally range from several tens of kΩ to several hundreds of kΩ. • The gain is about 6 dB.
13 12	V_C V_{Cref}	$V_{CC}2/2$ ±1.0		• V_C is the speed control pin. Forward when $V_C > V_{Cref}$. Reverse when $V_C < V_{Cref}$. V_C is used to control the output voltage. • V_{Cref} determines the motor control stop voltage. $V_{CC}2/2$ in normal use.
11 10	GC1 GC2	0 to $V_{CC}2$		• Input/output gain switching pins. • GC1 is for first-stage amplifier Z1/Z2 switching. When GC1 is LOW, Z1 is selected; when HIGH, Z2 is selected. GC2 is for next-stage amplifier switching.

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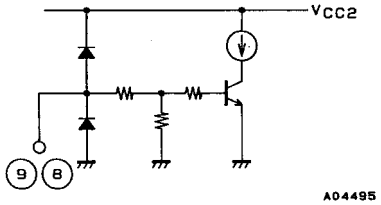
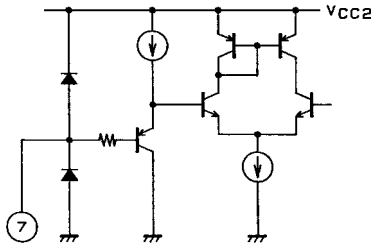
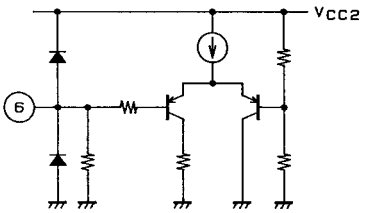
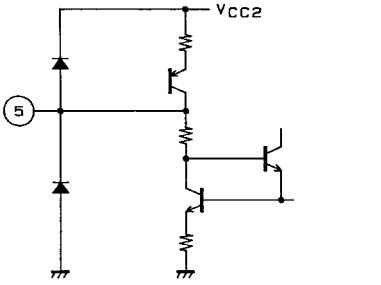
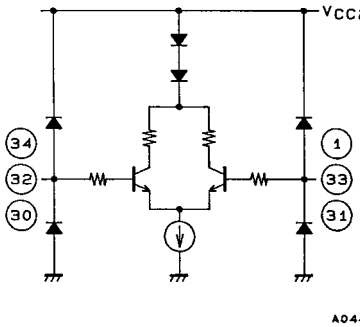
Pin No.	Pin Name	Pin Voltage	Equivalent Circuit Diagram	Pin Function
9 8	CTRLϕ CTRL1	0 to $V_{CC}2$		• Operation mode switching pins. • Refer to the Mode Switching Truth Table for selection of control, acceleration, or deceleration.
7	NS+	0 to $V_{CC}2 - 1$ V		• Input pin at noncontrol mode. • The input-output gain is 14 dB. (GC2: LOW) • Motor stops when V_{NS} = 0 V.
6	S/S	0 to $V_{CC}2$		• When the S/S pin is HIGH, START; when LOW, STOP. • The threshold is $V_{CC}2/2$.
5	FC			• Connect a capacitor between this pin and GND to reduce the input/output gain frequency response and to stop the oscillator.
1 34 33 32 31 30	$W_{IN}2$ $W_{IN}1$ $V_{IN}2$ $V_{IN}1$ $U_{IN}2$ $U_{IN}1$	1.3 to 2.2 V		W-phase Hall device input pins. Logic “H” represent $W_{IN}1 > W_{IN}2$ V-phase Hall device input pins. Logic “H” represent $V_{IN}1 > V_{IN}2$ U-phase Hall device input pins. Logic “H” represent $U_{IN}1 > U_{IN}2$

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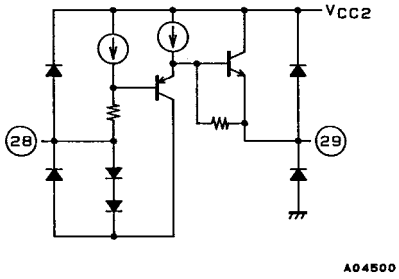
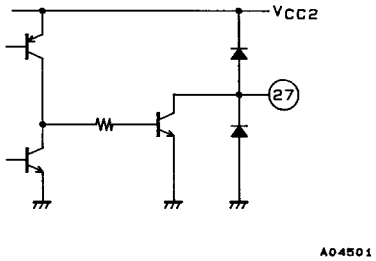
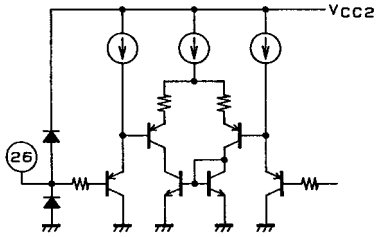
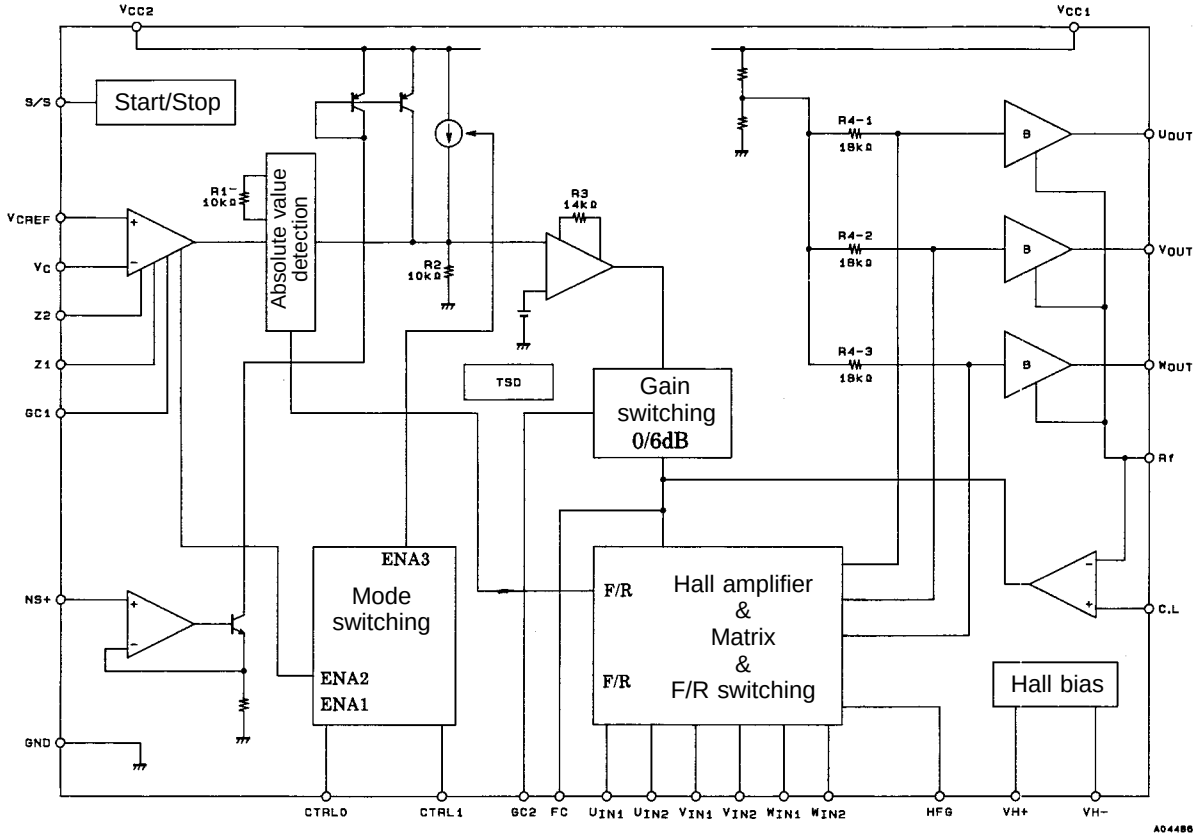
Pin No.	Pin Name	Pin Voltage	Equivalent Circuit Diagram	Pin Function
29 28	VH+ VH–	2.4 V 1.4 V		• Hall device power supply pins. A voltage difference of 1.0 V is developed between VH+ and VH–.
27	H.FG	0 to $V_{CC}2$		• Hall FG pin. • The Hall waveform is converted into a pulse signal and then used as the FG pulse signal.
26	CL	0 to $V_{CC}2$		• When the Rf pin voltage becomes equal to the C_L pin voltage, the current limiter operate. The C_L voltage is determined externally.
25	$V_{CC}1$	5 to 18 V		• Power supply for output block. • This supply should be kept stable to prevent ripple and noise from entering this pin.

Block Diagram



Sample Application Circuit