


**LB1896**

## 3-phase Brushless Motor Driver for CD-ROM Spindle Drive Use

### Overview

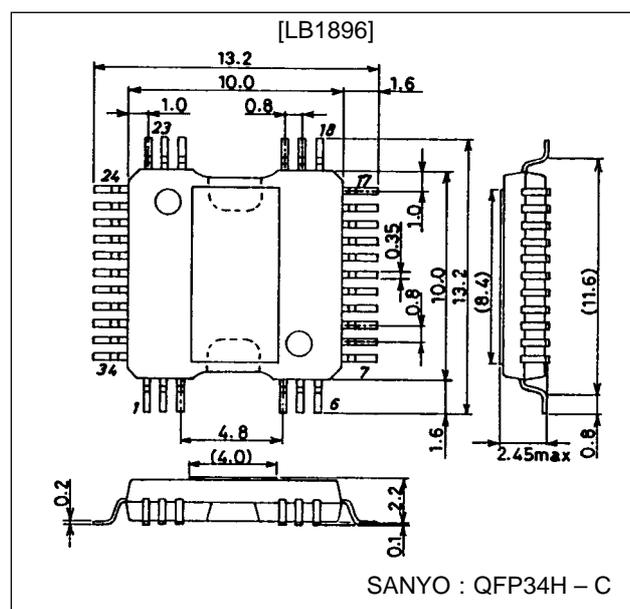
The LB1896 is a 3-phase brushless motor driver IC that is ideal for driving CD-ROM spindle motors.

### Functions and Features

- 120° voltage linear technique
- V-type control voltage
- Switchable control gain
- Control, noncontrol, acceleration/deceleration mode select pins built in.
- Start/Stop pin built in, Hall bias built in.

### Package Dimensions

unit : mm

**3219-QFP34H-C**

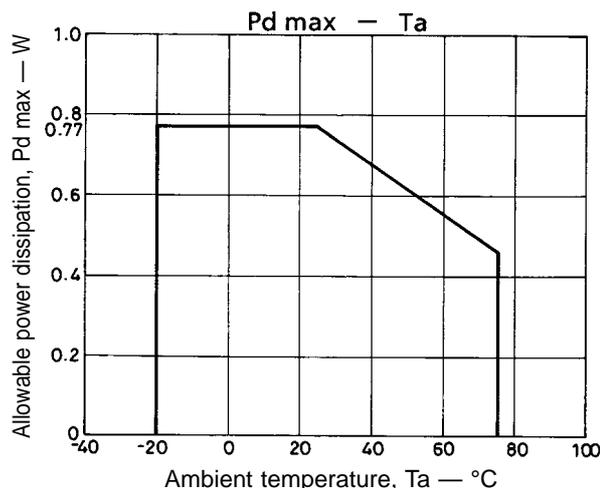
### Specifications

#### Absolute Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC1</sub> max		20	V
	V <sub>CC2</sub> max		7.0	V
Applied output voltage	V <sub>OU, v, w</sub>		20	V
Output current	I <sub>OUT</sub>		1.2	A
Allowable power dissipation	P <sub>d</sub> max	Independent IC	0.77	W
Operating temperature	T <sub>opr</sub>		-20 to +75	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

#### Operating Conditions at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>CC1</sub>		5 to 18	V
	V <sub>CC2</sub>	V <sub>CC1</sub> ≥ V <sub>CC2</sub>	4.3 to 6.5	V
V <sub>Cref</sub> input voltage	V <sub>Cref</sub>		V <sub>CC2</sub> /2 ±1.0	V
V <sub>NS</sub> input voltage	V <sub>NS</sub>		0 to V <sub>CC2</sub> -1.0	V



**Electrical Characteristics at Ta = 25 °C, V<sub>CC1</sub> = 12 V, V<sub>CC2</sub> = 5 V**

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply current 1	I <sub>CC1</sub>	V <sub>C</sub> = open, V <sub>Cref</sub> = open, R <sub>L</sub> = ∞, V <sub>S/S</sub> = 5 V		17	30	mA
Supply current 2	I <sub>CC2</sub>	V <sub>C</sub> = open, V <sub>Cref</sub> = open		7.5	10.5	mA
Supply current 3	I <sub>CC3</sub>	V <sub>C</sub> = open, V <sub>Cref</sub> = open, R <sub>L</sub> = ∞, V <sub>S/S</sub> = 0 V, (I <sub>CC</sub> of V <sub>CC1</sub> )		0.9	3	mA
[Drive block]						
Output saturation voltage	V <sub>O(sat)1</sub>	I <sub>OUT</sub> = 0.4 A, sink + source		1.6	2.2	V
	V <sub>O(sat)2</sub>	I <sub>OUT</sub> = 0.8 A, sink + source		2.0	3.0	V
Output TRS sustaining voltage	V <sub>O(sus)</sub>	I <sub>OUT</sub> = 20 mA	20			V
Output static voltage	V <sub>OQ</sub>	V <sub>C</sub> = 2.5 V, V <sub>Cref</sub> = 2.5 V	5.7	6.0	6.3	V
Hall amplifier input offset voltage	V <sub>H offset</sub>		-5		+5	mV
Hall amplifier input bias current	I <sub>H bias</sub>			1	5	μA
Hall amplifier common-mode input voltage range	V <sub>Hch</sub>		1.3		2.2	V
Hall input/output voltage gain	G <sub>VHO</sub>		40	43	46	dB
Control/output drive gain 1	G <sub>VCO1</sub>	RZ1 = RZ2, GC1 = L, GC2 = L	26	29		dB
Control/output channel difference 1	ΔG <sub>VCO1</sub>	RZ1 = RZ2, GC1 = L, GC2 = L	-1.5		+1.5	dB
Control/output drive gain 2	G <sub>VCO2</sub>	RZ1 = RZ2, GC1 = L, GC2 = H	32	35		dB
Control/output channel difference 2	ΔG <sub>VCO2</sub>	RZ1 = RZ2, GC1 = L, GC2 = H	-1.9		+1.9	dB
Input dead zone voltage	V <sub>DZ</sub>	RZ1 = RZ2, GC1 = L, GC2 = L V <sub>O</sub> (voltage between out and out) = 0.1 V	±13	±38	±55	mV
Input bias current 1	I <sub>B SERVO</sub>	V <sub>C</sub> = 1.0 V			500	nA
Input bias current 2	I <sub>B n.s</sub>	V <sub>NS</sub> = 1.0 V			500	nA
S/S pin high voltage	V <sub>S/S H</sub>	Input is CMOS level	4			V
S/S pin low voltage	V <sub>S/S L</sub>	Note) S/S pin V <sub>th</sub> = V <sub>CC2</sub> /2			1	V
Gain control 1 high voltage	V <sub>GC1 H</sub>	Input is at CMOS level.	4			V
Gain control 1 low voltage	V <sub>GC1 L</sub>	Note) GC1 pin V <sub>th</sub> = 2.0 V			1	V
Gain control 2 high voltage	V <sub>GC2 H</sub>	Input is at CMOS level.	4			V
Gain control 2 low voltage	V <sub>GC2 L</sub>	Note) GC2 pin V <sub>th</sub> = 2.0 V			1	V
S/S pin input current	I <sub>S/S</sub>	Input voltage = 5 V		50	100	μA
Gain control 1, 2 current	I <sub>GC</sub>	Input voltage = 5 V		53	110	μA
Rotation output saturation voltage	V <sub>(sat) H.FG</sub>	I <sub>O</sub> = -5 mA		0.24	0.5	V
Rotation output saturation sustaining voltage	V <sub>(sus) H.FG</sub>				7	V
Hall bias voltage	V <sub>H±</sub>	I <sub>O</sub> = 5 mA, R <sub>H</sub> = 200 Ω	0.7	0.97	1.2	V
CTRL pin high voltage	V <sub>CTRL H</sub>	Common for CTRL1 and CTRL2 input CMOS level	4			V
CTRL pin low voltage	V <sub>CTRL L</sub>	Note) CTRL pin V <sub>th</sub> = 2.5 V			1.0	V
CTRL input current	I <sub>CTRL</sub>	Input voltage = 5 V		53	110	μA
TSD operation voltage	TSD	Design target	150	180	210	°C
TSD hysteresis	ΔTSD	Design target		15		°C

Note) V<sub>th</sub> is a design target and not measured.

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## Mode Switching Truth Table

CTRL0	CTRL1	Mode
L	L	Control
L	H	Noncontrol
H	L	Acceleration
H	H	Deceleration

L = 0 to 1.0 V  
H = 4.0 V or more

## Hall Logic Truth Table

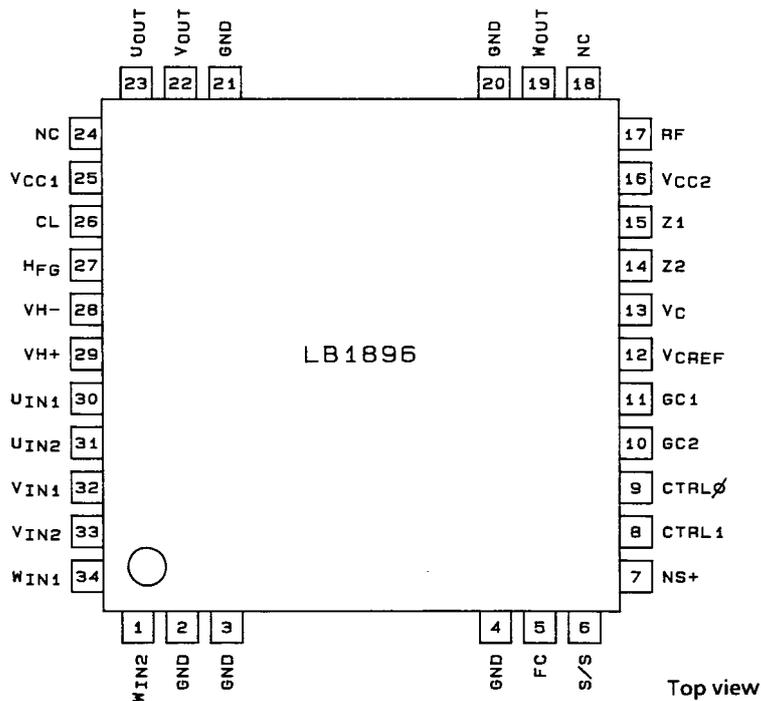
	Source → Sink	Hall input			F/R Control
		U <sub>IN</sub>	V <sub>IN</sub>	W <sub>IN</sub>	
1	W → V	H	H	L	Forward
	V → W				Reverse
2	W → U	H	L	L	Forward
	U → W				Reverse
3	V → W	L	L	H	Forward
	W → V				Reverse
4	U → V	L	H	L	Forward
	V → U				Reverse
5	V → U	H	L	H	Forward
	U → V				Reverse
6	U → W	L	H	H	Forward
	W → U				Reverse

An input is considered to be HIGH when  $U_{IN1} > U_{IN2}$ ,  $V_{IN1} > V_{IN2}$ , and  $W_{IN1} > W_{IN2}$  by 0.2 V or more.

Forward when  $V_C > V_{Cref}$

Reverse when  $V_C < V_{Cref}$

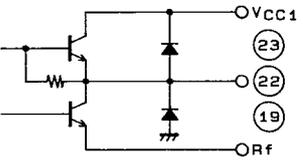
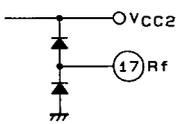
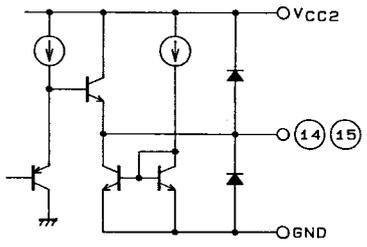
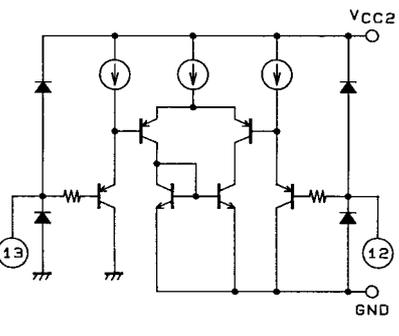
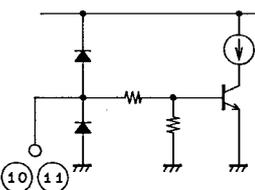
## Pin Assignment



A04487

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## Pin Functions

Pin No.	Pin Name	Pin Voltage	Equivalent Circuit Diagram	Pin Function
3, 4 20, 21	Frame GND			Frame GND. GND must be shared.
2	GND			GND
23 22 19	$U_{OUT}$ $V_{OUT}$ $W_{OUT}$		 <p style="text-align: right;">A04490</p>	Output pins. Motor connection
17	Rf		 <p style="text-align: right;">A04491</p>	Output Tr GND. A resistor can be connected between this pin and GND to sense the output current as a voltage drop to provide for overcurrent protection.
18, 24	NC			Idle pins.
16	$V_{CC2}$	4.3 to 6.5 V		<ul style="list-style-type: none"> <li>Power supply for blocks other than the output block.</li> <li>This supply should be kept stable to prevent ripple and noise from entering this pin.</li> </ul>
15 14	Z1 Z2		 <p style="text-align: right;">A04492</p>	<ul style="list-style-type: none"> <li>First-stage amplifier gain setting resistors.</li> <li>Z1 and Z2 normally range from several tens of <math>k\Omega</math> to several hundreds of <math>k\Omega</math>.</li> <li>The gain is about 6 dB.</li> </ul>
13 12	$V_C$ $V_{Cref}$	$V_{CC2}/2$ $\pm 1.0$	 <p style="text-align: right;">A04493</p>	<ul style="list-style-type: none"> <li><math>V_C</math> is the speed control pin. Forward when <math>V_C &gt; V_{Cref}</math>. Reverse when <math>V_C &lt; V_{Cref}</math>. <math>V_C</math> is used to control the output voltage.</li> <li><math>V_{Cref}</math> determines the motor control stop voltage. <math>V_{CC2}/2</math> in normal use.</li> </ul>
11 10	GC1 GC2	0 to $V_{CC2}$	 <p style="text-align: right;">A04494</p>	<ul style="list-style-type: none"> <li>Input/output gain switching pins.</li> <li>GC1 is for first-stage amplifier Z1/Z2 switching. When GC1 is LOW, Z1 is selected; when HIGH, Z2 is selected. GC2 is for next-stage amplifier switching.</li> </ul>

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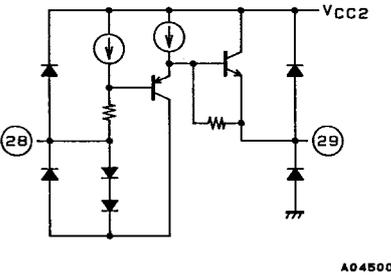
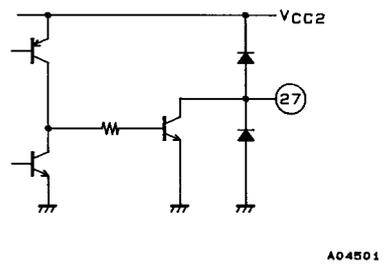
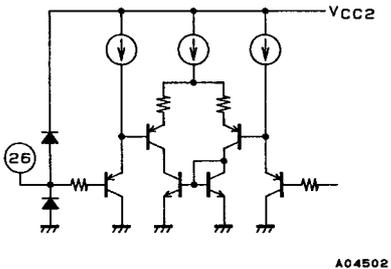
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Pin No.	Pin Name	Pin Voltage	Equivalent Circuit Diagram	Pin Function
9 8	CTRL $\phi$ CTRL1	0 to V <sub>CC2</sub>	<p style="text-align: right;">A04495</p>	<ul style="list-style-type: none"> <li>• Operation mode switching pins.</li> <li>• Refer to the Mode Switching Truth Table for selection of control, acceleration, or deceleration.</li> </ul>
7	NS+	0 to V <sub>CC2</sub> - 1 V	<p style="text-align: right;">A04496</p>	<ul style="list-style-type: none"> <li>• Input pin at noncontrol mode.</li> <li>• The input-output gain is 14 dB. (GC2: LOW)</li> <li>• Motor stops when V<sub>NS</sub> = 0 V.</li> </ul>
6	S/S	0 to V <sub>CC2</sub>	<p style="text-align: right;">A04497</p>	<ul style="list-style-type: none"> <li>• When the S/S pin is HIGH, START; when LOW, STOP.</li> <li>• The threshold is V<sub>CC2</sub>/2.</li> </ul>
5	FC		<p style="text-align: right;">A04498</p>	<ul style="list-style-type: none"> <li>• Connect a capacitor between this pin and GND to reduce the input/output gain frequency response and to stop the oscillator.</li> </ul>
1 34 33 32 31 30	W <sub>IN2</sub> W <sub>IN1</sub> V <sub>IN2</sub> V <sub>IN1</sub> U <sub>IN2</sub> U <sub>IN1</sub>	1.3 to 2.2 V	<p style="text-align: right;">A04499</p>	<p>W-phase Hall device input pins. Logic "H" represent W<sub>IN1</sub> &gt; W<sub>IN2</sub></p> <p>V-phase Hall device input pins. Logic "H" represent V<sub>IN1</sub> &gt; V<sub>IN2</sub></p> <p>U-phase Hall device input pins. Logic "H" represent U<sub>IN1</sub> &gt; U<sub>IN2</sub></p>

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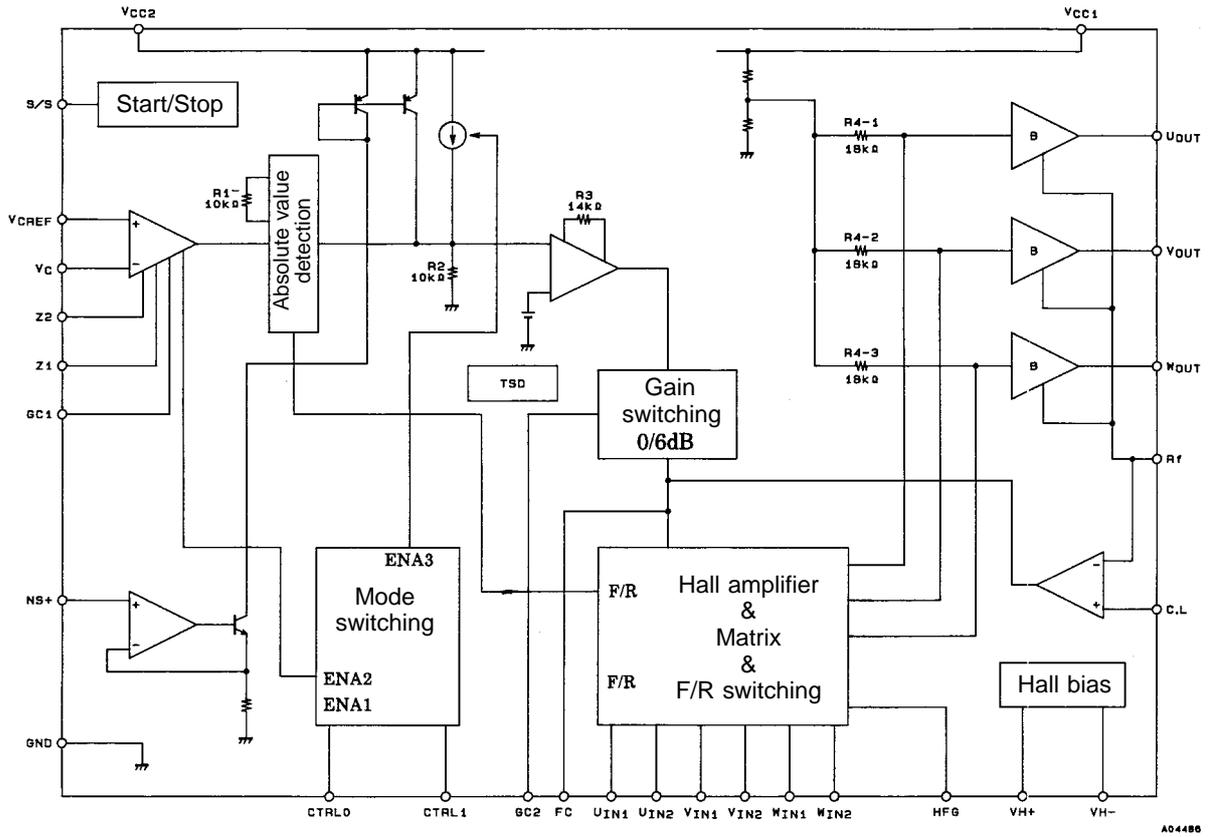
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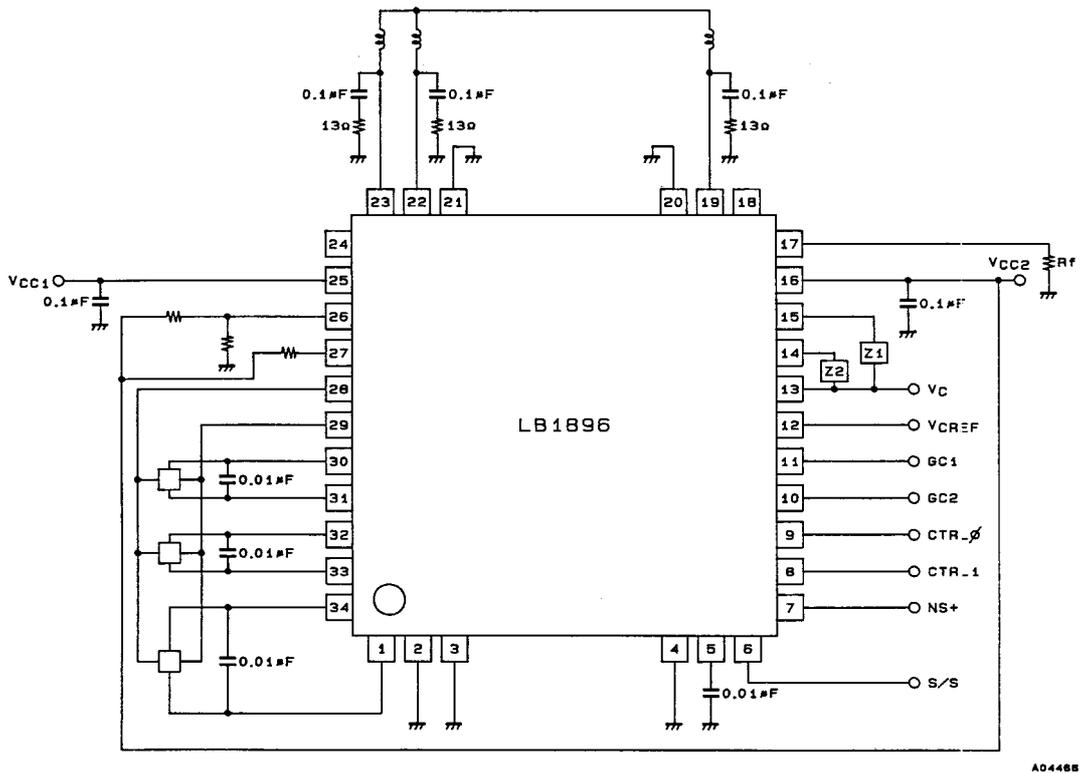
Pin No.	Pin Name	Pin Voltage	Equivalent Circuit Diagram	Pin Function
29 28	VH+ VH-	2.4 V 1.4 V	 <p style="text-align: right;">A04500</p>	<ul style="list-style-type: none"> <li>Hall device power supply pins.</li> <li>A voltage difference of 1.0 V is developed between VH+ and VH-.</li> </ul>
27	H.FG	0 to V <sub>CC2</sub>	 <p style="text-align: right;">A04501</p>	<ul style="list-style-type: none"> <li>Hall FG pin.</li> <li>The Hall waveform is converted into a pulse signal and then used as the FG pulse signal.</li> </ul>
26	CL	0 to V <sub>CC2</sub>	 <p style="text-align: right;">A04502</p>	<ul style="list-style-type: none"> <li>When the R<sub>f</sub> pin voltage becomes equal to the C<sub>L</sub> pin voltage, the current limiter operate. The C<sub>L</sub> voltage is determined externally.</li> </ul>
25	V <sub>CC1</sub>	5 to 18 V		<ul style="list-style-type: none"> <li>Power supply for output block.</li> <li>This supply should be kept stable to prevent ripple and noise from entering this pin.</li> </ul>

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## Block Diagram



## Sample Application Circuit



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