

**LC7456A**

## U.S. Closed Caption Signal Extraction IC

### Preliminary

#### Overview

The LC7456A receives the composite video signal from the V / C (Video Chroma) signal processor and extracts the closed caption data. This data and a clock signal, generated by an on-chip PLL, are then sent to the decoder IC. The LC7456A is a CMOS version of the LA7945 IC also currently in production. The differences between the LA7945 and the LC7456A are a change from Bipolar to CMOS technology, a smaller package size (22 pins to 16 pins), and a reduction in the external circuitry required.

An LC8640XX series microcontroller is needed to perform the decoding after the LC7456A has extracted the caption data from the composite video signal.

#### Features

- Low power consumption due to CMOS process
- Accurate caption signal extraction using a built-in pead hold circuit and digital technology.
- Power Requirement :  $5V \pm 10\%$
- Package : DIP16

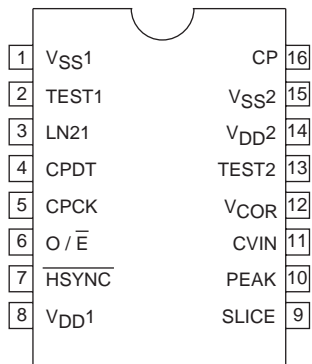
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## Pin Arrangement Diagram (DIP16)

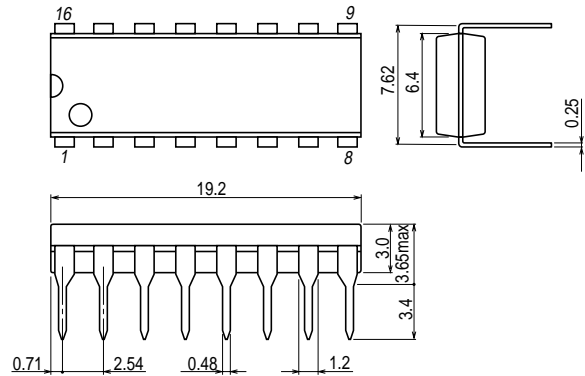


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## Package Dimensions

unit : mm

3006B

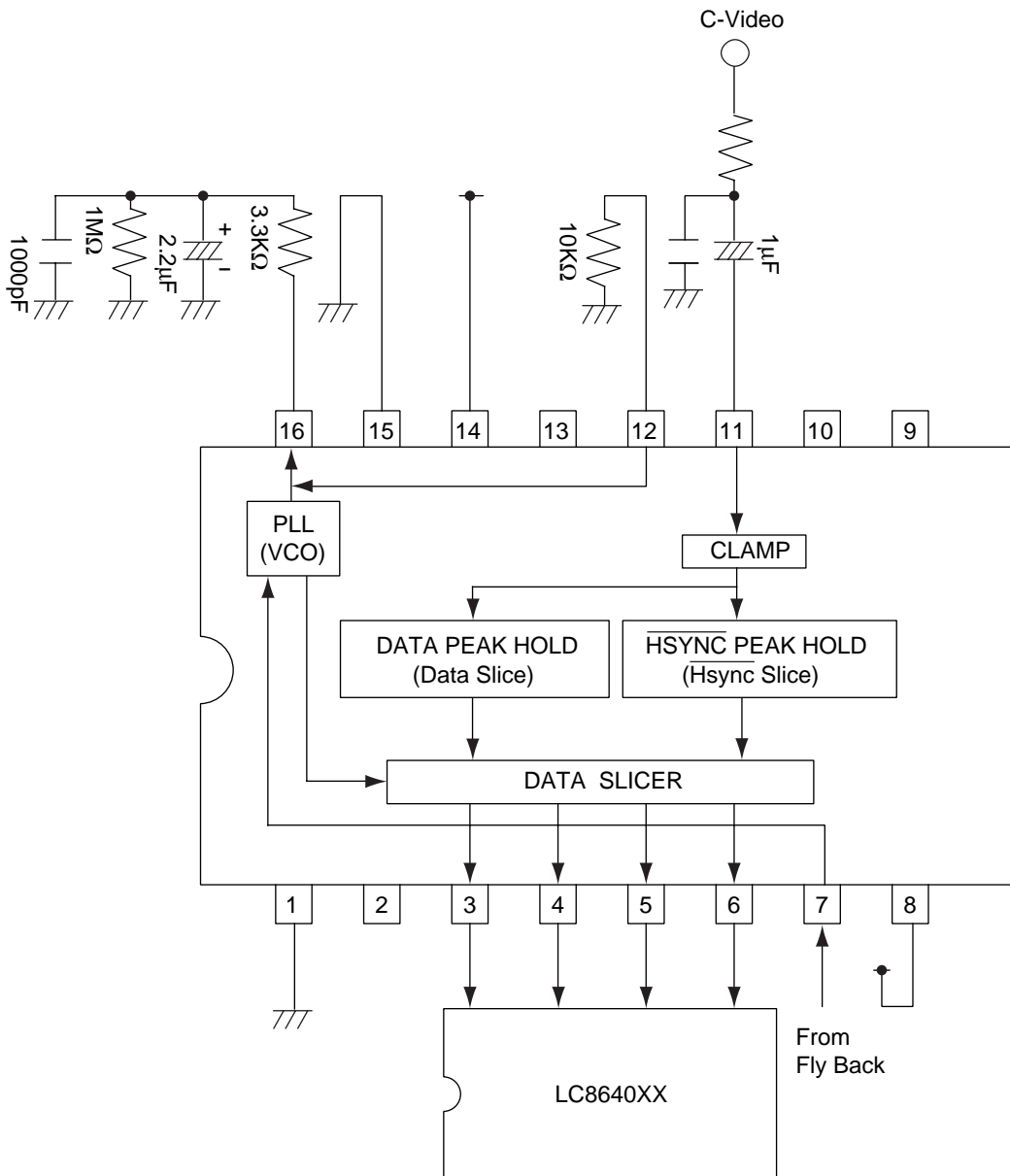


SANYO : DIP16(300mil)

## Pin Function

| Pin |       | Function                            |
|-----|-------|-------------------------------------|
| No. | Name  |                                     |
| 1   | VSS1  | GND                                 |
| 2   | TEST1 | Test pin, usually open              |
| 3   | LN21  | Line 21H pulse output               |
| 4   | CPDT  | Caption data output                 |
| 5   | CPCK  | Caption data latch clock output     |
| 6   | O/E   | Field determination output          |
| 7   | HSYNC | HSYNC input                         |
| 8   | VDD1  | Power supply                        |
| 9   | SILCE | Caption data slice level output     |
| 10  | PEAK  | Caption data peak hold level output |
| 11  | CVIN  | Composite video input               |
| 12  | VCOR  | Built-in VCO frequency control pin  |
| 13  | TEST2 | Test pin, usually open              |
| 14  | VDD2  | Power supply                        |
| 15  | VSS2  | GND                                 |
| 16  | CP    | Built-in PLL filter pin             |

System Block Diagram and Application



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### 1. Absolute Maximum Ratings at $V_{SS}=0V$ and $T_a=25^{\circ}C$

| Parameter                   | Symbol         | Pins                               | Conditions | Ratings |      |         | unit        |
|-----------------------------|----------------|------------------------------------|------------|---------|------|---------|-------------|
|                             |                |                                    |            | min.    | typ. | max.    |             |
| Supply voltage              | VDDMAX         | VDD1, VDD2                         | VDD1=VDD2  | -0.3    |      | +7.0    | V           |
| Input voltage               | V <sub>I</sub> | HSYNC, CVIN                        |            | -0.3    |      | VDD+0.3 |             |
| Output voltage              | V <sub>O</sub> | LN21, CPDT<br>CPCCK, O / $\bar{E}$ |            | -0.3    |      | VDD+0.3 |             |
| Maximum power dissipation   | Pdmax          | DIP16                              |            |         |      | 300     | mW          |
| Operating temperature range | Topr           |                                    |            | -30     |      | +70     | $^{\circ}C$ |
| Storage temperature range   | Tstg           |                                    |            | -55     |      | +150    |             |

\* VSS1 and VSS2 are same level.

VDD1 and VDD2 are also same level.

### 2. Recommended Operating Range at $V_{SS}=0V$ and $T_a= -30^{\circ}C$ to $+70^{\circ}C$

| Parameter                   | Symbol          | Pins       | Conditions      | VDD[V]     | Ratings   |       |           | unit |
|-----------------------------|-----------------|------------|-----------------|------------|-----------|-------|-----------|------|
|                             |                 |            |                 |            | min.      | typ.  | max.      |      |
| Operating supply voltage    | VDD             | VDD1, VDD2 | VDD1=VDD2       |            | 4.5       |       | 5.5       | V    |
| Input high voltage          | V <sub>IH</sub> | HSYNC      |                 | 4.5 to 5.5 | 0.85VDD   |       | VDD       |      |
| Input low voltage           | V <sub>IL</sub> | HSYNC      |                 | 4.5 to 5.5 | VSS       |       | 0.25VDD   |      |
| CVIN analog input range     | CVSYNC          | CVIN       | SYNC-WHITE=1.0V | 4.5 to 5.5 | 1Vp-p-3dB | 1Vp-p | 1Vp-p+3dB |      |
| HSYNC input frequency range | fH              | HSYNC      |                 | 4.5 to 5.5 | 15.60     | 15.73 | 15.90     | KHz  |

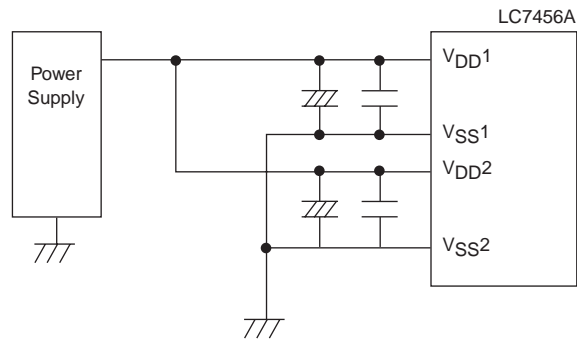
### 3. Electrical Characteristics at $V_{SS}=0V$ and $T_a= -30^{\circ}C$ to $+70^{\circ}C$

| Parameter           | Symbol          | Pins                               | Conditions             | VDD[V]     | Ratings |      |      | unit    |
|---------------------|-----------------|------------------------------------|------------------------|------------|---------|------|------|---------|
|                     |                 |                                    |                        |            | min.    | typ. | max. |         |
| Input high current  | I <sub>IH</sub> | HSYNC                              | V <sub>IN</sub> =VDD   | 4.5 to 5.5 |         |      | 1    | $\mu A$ |
| Input low current   | I <sub>IL</sub> | HSYNC                              | V <sub>IN</sub> =VSS   | 4.5 to 5.5 | -1      |      |      |         |
| Output high voltage | V <sub>OH</sub> | LN21, CPDT<br>CPCCK, O / $\bar{E}$ | I <sub>OH</sub> = -4mA | 4.5 to 5.5 | VDD-1.2 |      |      | V       |
| Output low voltage  | V <sub>OL</sub> | LN21, CPDT<br>CPCCK, O / $\bar{E}$ | I <sub>OL</sub> =10mA  | 4.5 to 5.5 |         |      | 1    |         |
| Input clamp voltage | VCLMP           | CVIN                               |                        | 5.0        | 2.3     | 2.5  | 2.7  |         |

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| Parameter            | Symbol | Pins      | Conditions | VDD[V]     | Ratings |      |      | unit |
|----------------------|--------|-----------|------------|------------|---------|------|------|------|
|                      |        |           |            |            | min.    | typ. | max. |      |
| Clamp input current  | CII    | CVIN      | CVIN=3V    | 5.0        | 5       | 10   | 18   | μA   |
| Clamp output current | COI    | CVIN      | CVIN=2V    | 5.0        | -120    | -70  | -30  |      |
| Current dissipation  | IDD    | VDD1,VDD2 |            | 4.5 to 5.5 |         | 6    | 15.0 | mA   |

\* VDD1 and VSS1 are the power pins for the digital circuits of the LC7456A, and VDD2 and VSS2 for the analog circuits. Connect like the following figure to reduce into the both circuits.



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