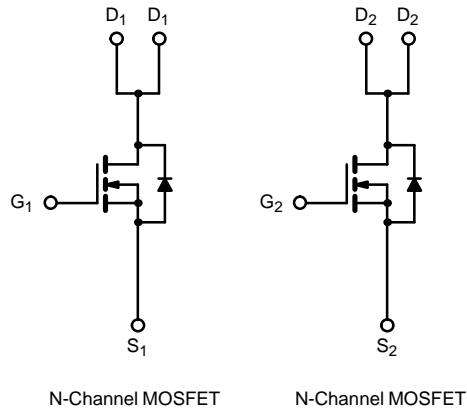
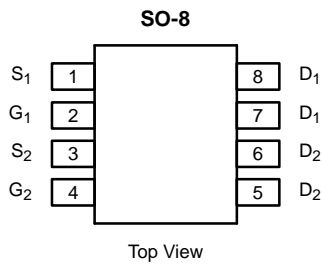




## Dual N-Channel Reduced Qg, Fast Switching MOSFET

**High-Efficiency**  
**PWM Optimized**

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
20	0.055 @ $V_{GS} = 4.5$ V	$\pm 4.5$
	0.075 @ $V_{GS} = 3.0$ V	$\pm 3.8$



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	20	V
Gate-Source Voltage		$V_{GS}$	$\pm 12$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	$\pm 4.5$	A
	$T_A = 70^\circ\text{C}$		$\pm 3.6$	
Pulsed Drain Current (10 $\mu\text{s}$ Pulse Width)		$I_{DM}$	$\pm 25$	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	$\pm 1.7$	
Maximum Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	2	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	62.5	$^\circ\text{C/W}$

Notes  
a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.



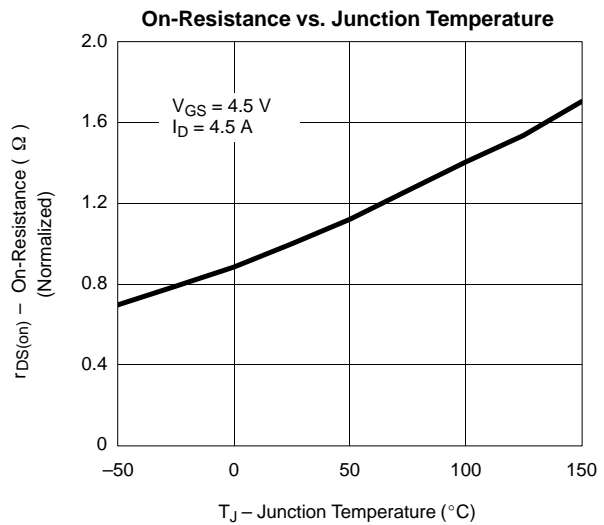
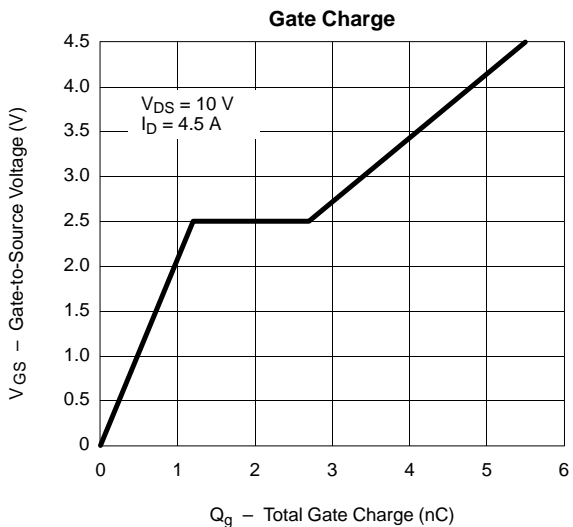
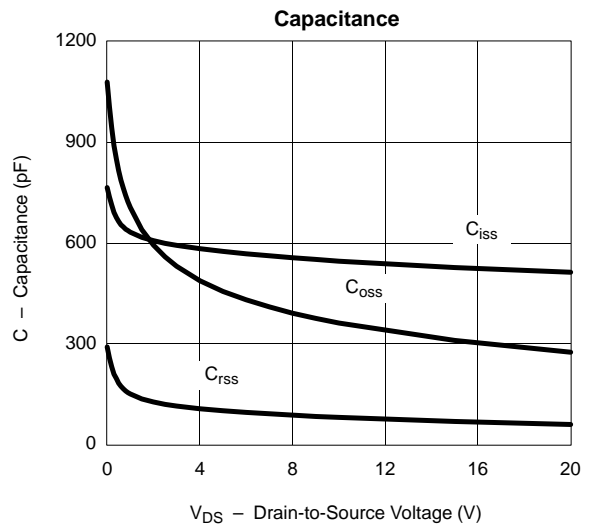
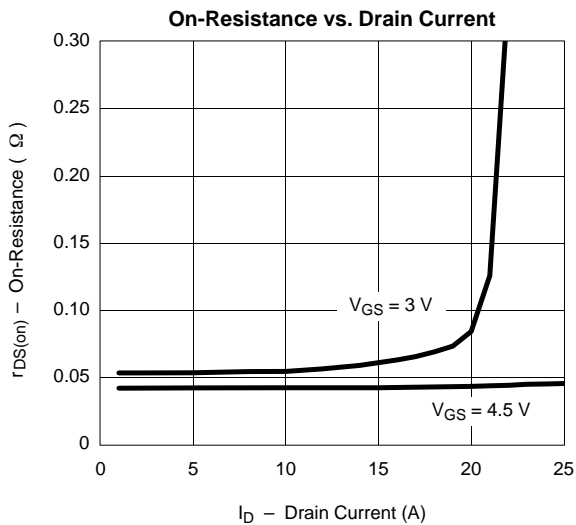
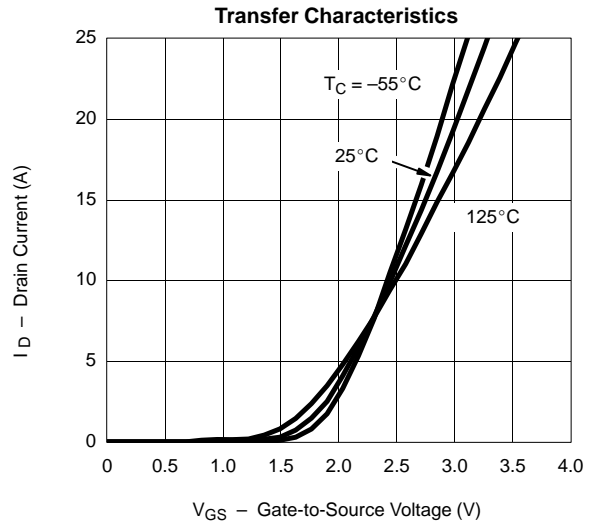
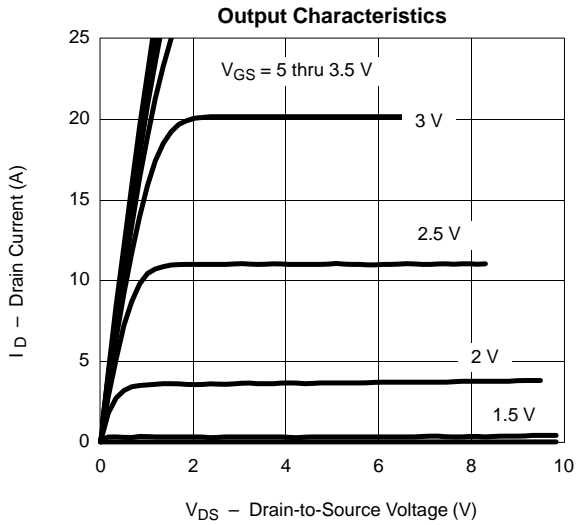
<b>SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)</b>						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.6			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 5 V	25			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.5 A		0.044	0.055	Ω
		V <sub>GS</sub> = 3.0 V, I <sub>D</sub> = 3.8 A		0.055	0.075	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.5 A		11.5		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.7 A, V <sub>GS</sub> = 0 V		0.73	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.5 A		5.5	10	nC
Gate-Source Charge	Q <sub>gs</sub>			1.2		
Gate-Drain Charge	Q <sub>gd</sub>			1.5		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 4.5 V, R <sub>G</sub> = 6 Ω		12	25	ns
Rise Time	t <sub>r</sub>			30	60	
Turn-Off Delay Time	t <sub>d(off)</sub>			23	50	
Fall Time	t <sub>f</sub>			9	20	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 1.7 A, di/dt = 100 A/μs		60	100	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

