Configuration EPROMs

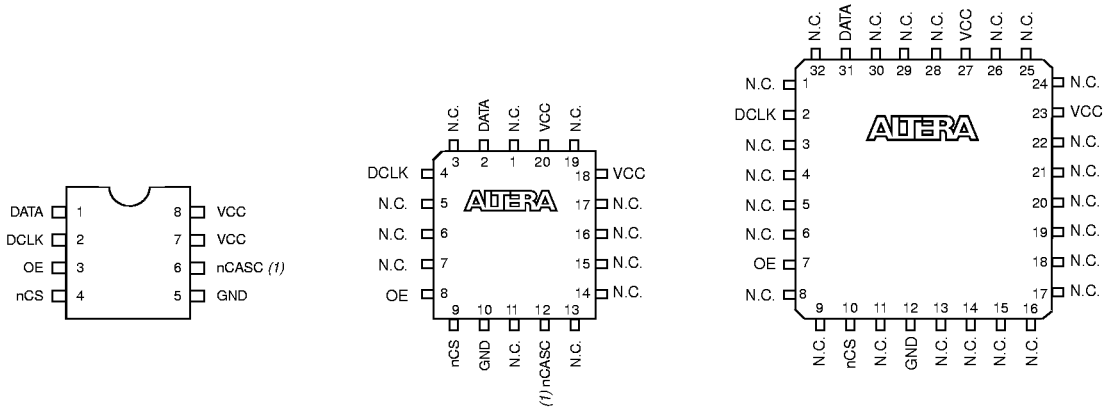
for FLEX Devices

October 1998, ver. 9 Data Sheet

Features

- Serial EPROM family for configuring FLEX® devices
- Easy-to-use 4-pin interface to FLEX devices
- Low current during configuration and near-zero standby current
- 5.0-V and 3.3-V operation
- Software design support with the Altera® MAX+PLUS® II development system for 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from Data I/O, BP Microsystems, and other manufacturers
- Available in compact plastic packages (see Figures 1 and 2)
  - 8-pin plastic dual in-line package (PDIP)
  - 20-pin plastic J-lead chip carrier (PLCC) package
  - 32-pin plastic thin quad flat pack (TQFP) package
- EPC2 has reprogrammable FLASH configuration memory
  - 5.0-V and 3.3-V in-system programmability (ISP) through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface
  - Built-in JTAG boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1
  - Supports programming through Serial Vector Format (**.svf**) files, Jam™ files, and the MAX+PLUS II software via the BitBlaster™, ByteBlaster™, or ByteBlasterMV™ download cable
  - `nINIT_CONF` pin allows a JTAG instruction to initiate FLEX configuration
  - Can be programmed with Programmer Object Files (**.pof**) for EPC1 and EPC1441 devices (except when configuring FLEX 8000 devices)
  - Available in 20-pin PLCC and 32-pin TQFP packages

Figure 1. EPC1, EPC1441, EPC1213, EPC1064 & EPC1064V Package Pin-Out Diagrams

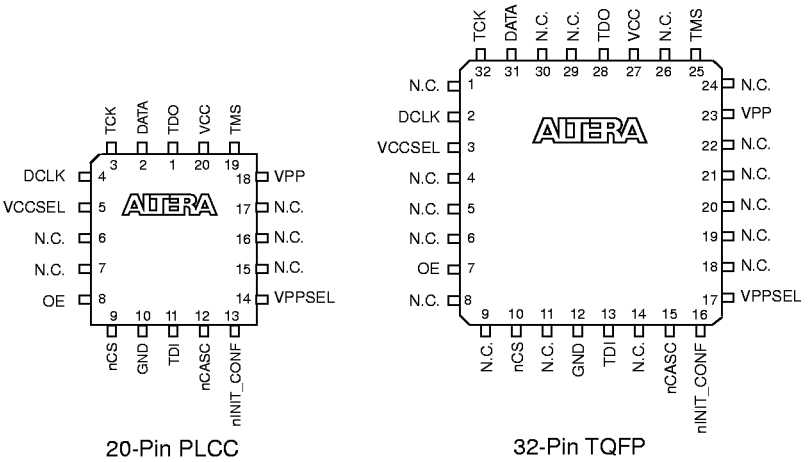


8-Pin PDIP	20-Pin PLCC	32-Pin TQFP
EPC1	EPC1	EPC1441
EPC1441	EPC1441	EPC1064
EPC1213	EPC1213	EPC1064V
EPC1064	EPC1064	
EPC1064V	EPC1064V	

Note:

(1) The nCASC pin is available on EPC1 and EPC1213 devices. On the EPC1064, EPC1064V, and EPC1441 devices, it is a reserved pin and should not be connected.

Figure 2. EPC2 Package Pin-Out Diagrams



Functional Description

With SRAM-based devices, configuration data must be reloaded each time the system initializes, or when new configuration data is needed. Altera Configuration EPROMs store configuration data for SRAM-based FLEX devices. Table 1 lists Altera's Configuration EPROMs.

Table 1. Configuration EPROMs

Device	Description
EPC2	1,695,680 × 1-bit device with 5.0-V or 3.3-V operation
EPC1	1,046,496 × 1-bit device with 5.0-V or 3.3-V operation
EPC1441	440,800 × 1-bit device with 5.0-V or 3.3-V operation
EPC1213	212,942 × 1-bit device with 5.0-V operation
EPC1064	65,536 × 1-bit device with 5.0-V operation
EPC1064V	65,536 × 1-bit device with 3.3-V operation

Table 2 lists the Configuration EPROM used with each FLEX device.

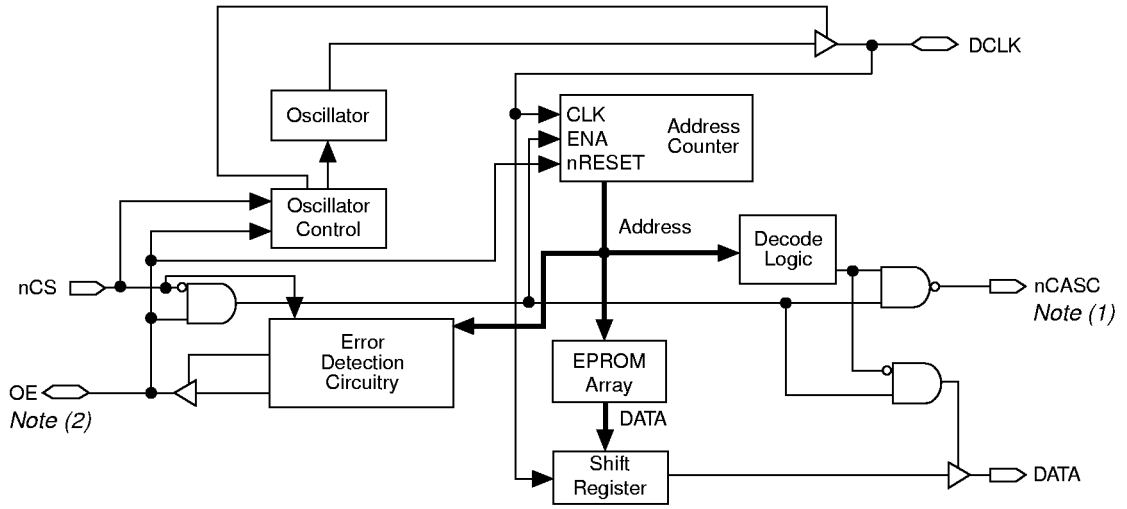
Table 2. Appropriate Configuration EPROM for FLEX Devices

FLEX Device	Configuration EPROM
EPF10K10, EPF10K10A	EPC2, EPC1, or EPC1441
EPF10K20	EPC2, EPC1, or EPC1441
EPF10K30, EPF10K30A, EPF10K30E	EPC2, EPC1, or EPC1441
EPF10K40	EPC2 or EPC1
EPF10K50, EPF10K50V, EPF10K50E	EPC2 or EPC1
EPF10K70	EPC2 or EPC1
EPF10K100, EPF10K100A, EPF10K100B, EPF10K100E	EPC2 or two EPC1 devices
EPF10K130V, EPF10K130E	EPC2 or two EPC1 devices
EPF10K200E	Two EPC2 or three EPC1 devices
EPF10K250A, EPF10K250E	Two EPC2 or four EPC1 devices
EPF8282A	EPC2, EPC1, EPC1441, or EPC1064
EPF8282AV	EPC2, EPC1, EPC1441, or EPC1064V
EPF8452A	EPC2, EPC1, EPC1441, or EPC1213
EPF8636A	EPC2, EPC1, EPC1441, or EPC1213
EPF8820A	EPC2, EPC1, EPC1441, or EPC1213
EPF81188A	EPC2, EPC1, EPC1441, or EPC1213
EPF81500A	EPC2, EPC1, or EPC1441
EPF6010A	EPC2, EPC1, or EPC1441
EPF6016, EPF6016A	EPC2, EPC1, or EPC1441
EPF6024A	EPC2, EPC1, or EPC1441

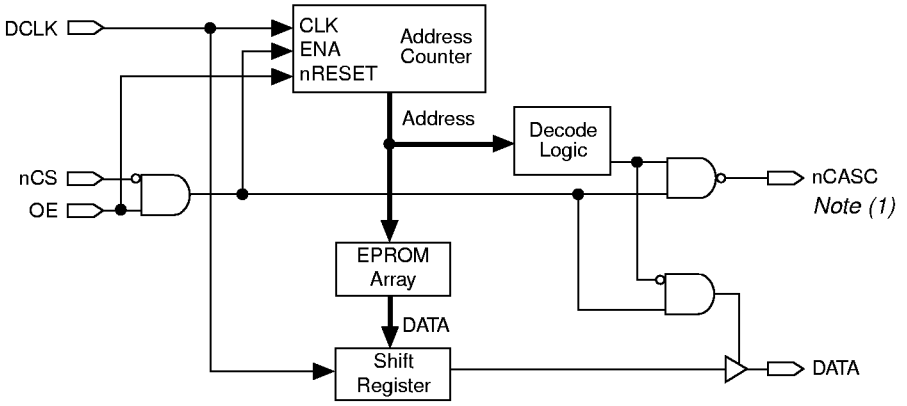
Figure 3 shows the Configuration EPROM block diagram.

Figure 3. Configuration EPROM Block Diagram

FLEX 10K & FLEX 6000 Device Configuration Using an EPC2, EPC1, or EPC1441
FLEX 8000 Device Configuration Using an EPC2



FLEX 8000 Device Configuration Using an EPC1, EPC1441, EPC1213, EPC1064, or EPC1064V



Notes:
(1) The EPC1441, EPC1064, and EPC1064V devices do not support data cascading. The EPC2, EPC1, and EPC1213 devices support data cascading.
(2) The OE pin is a bidirectional open-drain pin.

Device Configuration

The control signals for Configuration EPROMs—nCS, OE, and DCLK—interface directly with FLEX device control signals. All FLEX devices can be configured by a Configuration EPROM without requiring an external intelligent controller.

The Configuration EPROM's OE and nCS pins control the tri-state buffer on the DATA output pin, and enable the address counter (and the oscillator in EPC2, EPC1, and EPC1441 devices). When OE is driven low, the Configuration EPROM resets the address counter and tri-states its DATA pin. The nCS pin controls the output of the Configuration EPROM. If nCS is held high after the OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is driven low, the counter and DATA output pin are enabled. When OE is driven low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of nCS.

The EPC2, EPC1, and EPC1441 devices determine the operation mode and whether the FLEX 10K, FLEX 8000, or FLEX 6000 protocols should be used when OE is driven high.

When the Configuration EPROM has driven out all of its data and has driven nCASC low, the device tri-states the DATA pin to avoid contention with other Configuration EPROMs. Upon power-up, the address counter is reset automatically.

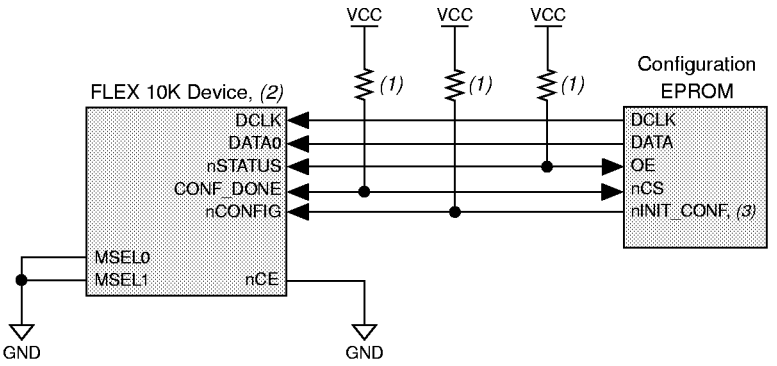
The EPC2 Configuration EPROM allows the user to initiate configuration of the FLEX device via an additional pin, called nINIT_CONF, which can be tied to the nCONFIG pin of the FLEX device(s) to be configured. A JTAG instruction causes the EPC2 device to drive nINIT_CONF low, which in turn pulls nCONFIG low. The EPC2 device then drives nINIT_CONF high to start FLEX configuration. When the JTAG state machine exits this state, nINIT_CONF releases nCONFIG and FLEX configuration is initiated.

An EPC2 device can be programmed with a POF generated for an EPC1 or EPC1441 device (except when configuring FLEX 8000 devices). In addition, an EPC1 device can be programmed using a POF generated for an EPC1441 device.

FLEX 10K & FLEX 6000 Device Configuration

FLEX 10K and FLEX 6000 devices can be configured with EPC2, EPC1, or EPC1441 devices. The EPC2, EPC1, or EPC1441 device stores configuration data in its EPROM array and serially clocks data out with an internal oscillator. The OE, nCS, and DCLK pins supply the control signals for the address counter and the output tri-state buffer. The EPC2, EPC1, or EPC1441 device sends a serial bitstream of configuration data to its DATA pin, which is routed to the DATA0 or DATA input pin on the FLEX 10K or FLEX 6000 device. One EPC1441 device can configure an EPF10K10, EPF10K20, or EPF10K30 device. Figure 4 shows a FLEX 10K or FLEX 6000 device configured with a single EPC2, EPC1, or EPC1441 device.

Figure 4. FLEX 10K or FLEX 6000 Device Configured with an EPC2, EPC1, or EPC1441 Configuration EPROM



Notes:

(1) All pull-up resistors are 1 kΩ. The `OE`, `nCS`, and `nINIT_CONF` pins on EPC2 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. This EPC2 feature is planned to be available in the MAX+PLUS II version 9.2 software, which is scheduled for release in the first quarter of 1999. In MAX+PLUS II version 9.1, this feature is not available and the internal pull-up resistors on these pins are disabled.

(2) The diagram shows a FLEX 10K device, which has `MSEL0` and `MSEL1` tied to ground. For FLEX 6000 devices, `MSEL` is tied to ground and the `DATA0` pin is named `DATA`. All other connections are the same for FLEX 10K and FLEX 6000 devices.

(3) The `nINIT_CONF` pin is available on EPC2 devices only. If `nINIT_CONF` is not available or not used, `nCONFIG` must be pulled to V_{CC} either directly or through a 1-kΩ resistor.

Table 3 describes EPC2, EPC1, and EPC1441 pin functions during FLEX 10K and FLEX 6000 device configuration.

Table 3. EPC2, EPC1 & EPC1441 Pin Functions During FLEX 10K & FLEX 6000 Configuration (Part 1 of 2)

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP *Note (1)*	20-Pin PLCC	32-Pin TQFP *Note (2)*		
DATA	1	2	31	Output	Serial data output. The DATA pin is tri-stated before configuration when its nCE pin is high, and after the Configuration EPROM finishes sending its configuration data. This operation is independent of the device's position in the cascade chain.
DCLK	2	4	2	I/O	DCLK is a clock output when configuring with a single Configuration EPROM or when the Configuration EPROM is the first device in a Configuration EPROM chain. DCLK is a clock input for subsequent Configuration EPROMs in a Configuration EPROM chain. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the OE input is held high, the nCS input is held low, and all configuration data has not been transferred to the target device. When configuring with the first EPC2 or EPC1 device in a Configuration EPROM chain or with a single EPC1441 device, the DCLK pin drives low after configuration is complete or when OE is low.
OE, *Note (3)*	3	8	7	I/O Open-drain	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count. If this pin is low (reset) during FLEX 10K or FLEX 6000 configuration, the internal oscillator becomes inactive and DCLK drives low. See "Error Detection Circuitry" on page 18.
nCS, *Note (3)*	4	9	10	Input	Chip select input (active low). A low input allows DCLK to increment the address counter and enables DATA to drive out. If the EPC1 or EPC2 is reset with nCS low, the device initializes as the first device in a configuration chain. If the EPC1 or EPC2 device is reset with nCS high, the device initializes as the subsequent device in the chain.
nCASC, *Notes (4), (5)*	6	12	15	Output	Cascade select output (active low). This output goes low when the address counter has reached its maximum value. In a chain of EPC1 or EPC2 devices, the nCASC pin of one device is connected to the nCS pin of the next device, which permits DCLK to clock data from the next EPC1 or EPC2 device in the chain.

Table 3. EPC2, EPC1 & EPC1441 Pin Functions During FLEX 10K & FLEX 6000 Configuration (Part 2 of 2)

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP *Note (1)*	20-Pin PLCC	32-Pin TQFP *Note (2)*		
nINIT_CONF, *Notes (3), (5), (6)*	–	13	16	Output Open-drain	Allows the INIT_CONF JTAG instruction to initiate configuration. This pin is connected to the nCONFIG pin of the FLEX device to initiate configuration from the EPC2 via a JTAG instruction. If a chain of EPC2 devices is used, only the first EPC2 has its nINIT_CONF pin tied to the FLEX device's nCONFIG pin. *Note (7)*
TDI, *Note (6)*	–	11	13	Input	JTAG data input pin. Connect this pin to V_{CC} if the JTAG circuitry is not used.
TDO, *Note (6)*	–	1	28	Output	JTAG data output pin. Do not connect this pin if the JTAG circuitry is not used.
TMS, *Note (6)*	–	19	25	Input	JTAG mode select pin. Connect this pin to V_{CC} if the JTAG circuitry is not used.
TCK, *Note (6)*	–	3	32	Input	JTAG clock pin. Connect this pin to ground if the JTAG circuitry is not used.
VCCSEL, *Note (6)*	–	5	3	Input	Mode select for V_{CC} supply. VCCSEL must be connected to ground if the device uses a 5.0-V power supply (i.e., V_{CC} = 5.0 V). VCCSEL must be connected to V_{CC} if the device uses a 3.3-V power supply (i.e., V_{CC} = 3.3 V).
VPPSEL, *Note (6)*	–	14	17	Input	Mode select for VPP. VPPSEL must be connected to ground if VPP uses a 5.0-V power supply (i.e., VPP = 5.0 V). VPPSEL must be connected to V_{CC} if VPP uses a 3.3-V power supply (i.e, VPP = 3.3 V).
VPP	–	18	23	Power	Programming power pin. For the EPC2 device, this pin is normally tied to V_{CC}. If the EPC2 V_{CC} is 3.3 V, VPP can be tied to 5.0 V to improve in-system programming times. For EPC1 and EPC1441 devices, VPP must be tied to V_{CC}.
VCC	7, 8	20	27	Power	Power pin.
GND	5	10	12	Ground	Ground pin. A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.

Notes:

(1) This package is available for EPC1 and EPC1441 devices only.
(2) This package is available for EPC2 and EPC1441 devices only.
(3) The OE, nCS, and nINIT_CONF pins on EPC2 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. This EPC2 feature is planned to be available in the MAX+PLUS II version 9.2 software, which is scheduled for release in the first quarter of 1999. In MAX+PLUS II version 9.1, the internal pull-up resistors on these pins are disabled.
(4) The EPC1441 device does not support data cascading. EPC2 and EPC1 devices support data cascading.
(5) The nCASC and nINIT_CONF pins are planned to be supported for EPC2 devices in the MAX+PLUS II version 9.2 software.
(6) This pin applies to EPC2 devices only.
(7) This instruction is planned to be supported in the MAX+PLUS II version 9.2 software.

FLEX 10K & FLEX 6000 Configuration with Multiple EPC2 or EPC1 Configuration EPROMs

When configuration data for FLEX 10K or FLEX 6000 devices exceeds the capacity of a single EPC2 or EPC1 device, multiple EPC2 or EPC1 devices can be cascaded together. (The EPC1441 device does not support data cascading.) If multiple EPC2 or EPC1 devices are required, the nCASC and nCS pins provide handshaking between the devices.

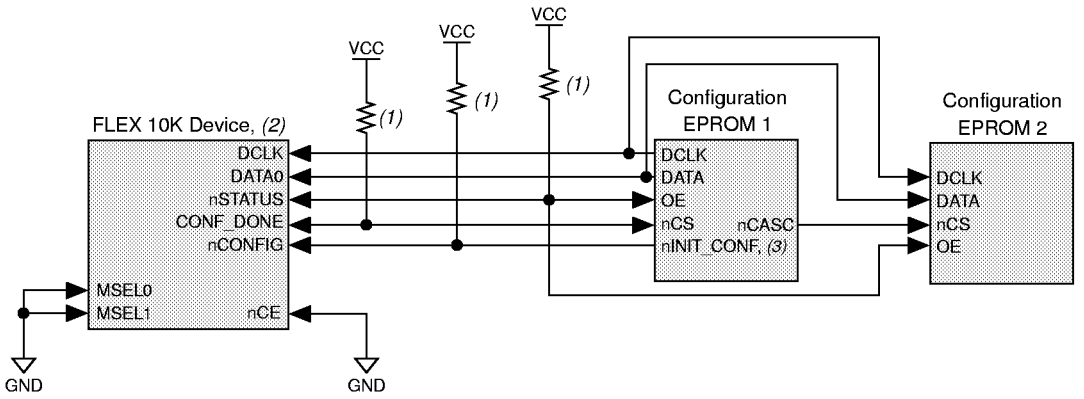
When configuring FLEX 10K or FLEX 6000 devices with cascaded EPC2 or EPC1 devices, the position of the EPC2 or EPC1 device in the chain determines its operation. When the first or master device in a Configuration EPROM chain is powered up or reset and the nCS pin is driven low, the master device controls FLEX configuration. The master device supplies all clock pulses to one or more FLEX devices and to any subsequent slave devices during configuration. The master EPC2 or EPC1 device also provides the first stream of data to the FLEX devices during multi-device configuration. After the master EPC2 or EPC1 device finishes sending configuration data, it drives its nCASC pin low, which drives the nCS pin of the first slave EPC2 or EPC1 device low. This action causes the slave EPC2 or EPC1 device to send configuration data to the FLEX devices.

The master EPC2 or EPC1 device clocks all subsequent slave devices until configuration is complete. Once all configuration data is transferred and the nCS pin on the master EPC2 or EPC1 device is driven high by the FLEX device's CONF_DONE pin, the master EPC2 or EPC1 device clocks 16 additional cycles to initialize the FLEX device(s). The master EPC2 or EPC1 device then goes into zero-power (idle) state. If nCS on the master EPC2 or EPC1 device is driven high before all configuration data is transferred, or if nCS is not driven high after all configuration data is transferred, the master EPC2 or EPC1 device drives the FLEX device's nSTATUS pin low, indicating a configuration error.

Configuration automatically restarts if the project is compiled with the *Auto-Restart Configuration on Frame Error* option turned on in the MAX+PLUS II software's **Global Project Device Options** dialog box (Assign menu). Figure 5 shows a FLEX 10K or FLEX 6000 device configured with two EPC2 or EPC1 devices. Additional EPC2 or EPC1 devices can be added by connecting nCASC to nCS of the subsequent slave EPC2 or EPC1 device in the chain and connecting DCLK, DATA, and OE in parallel.

FLEX 10K, FLEX 10KA, FLEX 10KE, and 5.0-V and 3.3-V FLEX 6000 devices can all be configured in the same chain. See "Configuration Chain with Multiple Voltage Levels" on page 20.

Figure 5. FLEX 10K or FLEX 6000 Device Configured with Two EPC2 or EPC1 Configuration EPROMs



Notes:

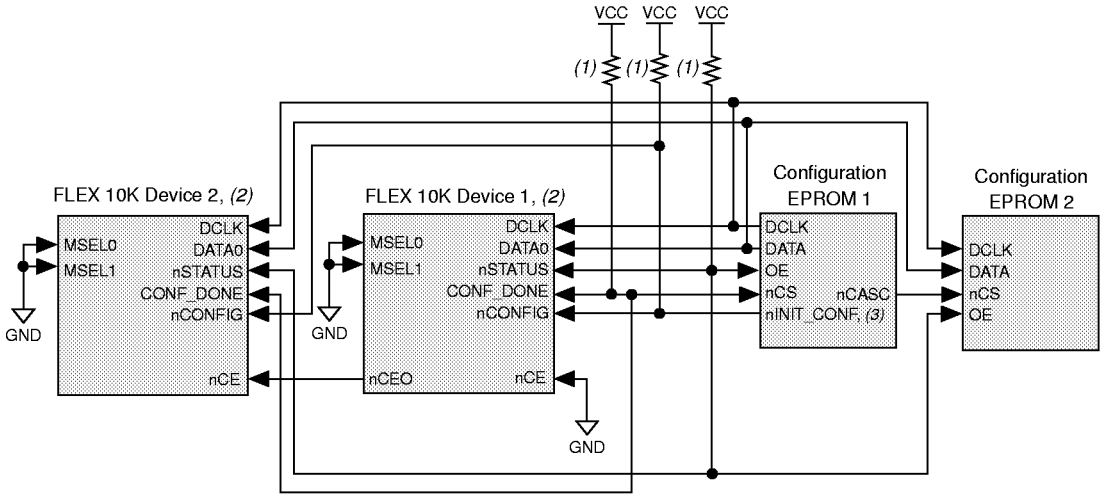
(1) All pull-up resistors are 1 kΩ. The OE, nCS, and nINIT_CONF pins on EPC2 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. This EPC2 feature is planned to be available in the MAX+PLUS II version 9.2 software, which is scheduled for release in the first quarter of 1999. In MAX+PLUS II version 9.1, this feature is not available and the internal pull-up resistors on these pins are disabled.

(2) The diagram shows a FLEX 10K device, which has MSEL0 and MSEL1 tied to ground. For FLEX 6000 devices, MSEL is tied to ground and the DATA0 pin is named DATA. All other connections are the same for FLEX 10K and FLEX 6000 devices.

(3) The nINIT_CONF pin is available on EPC2 devices only. If nINIT_CONF is not available or not used, nCONFIG must be pulled to V_{CC} either directly or through a 1-kΩ resistor.

Figure 6 shows two FLEX 10K or FLEX 6000 devices configured with two EPC2 or EPC1 devices.

Figure 6. Two FLEX 10K or FLEX 6000 Devices Configured with Two EPC2 or EPC1 Configuration EPROMs



Notes:

(1) All pull-up resistors are 1 kΩ. The OE, nCS, and nINIT_CONF pins on EPC2 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. This EPC2 feature is planned to be available in the MAX+PLUS II version 9.2 software, which is scheduled for release in the first quarter of 1999. In MAX+PLUS II version 9.1, this feature is not available and the internal pull-up resistors on these pins are disabled.

(2) The diagram shows a FLEX 10K device, which has MSEL0 and MSEL1 tied to ground. For FLEX 6000 devices, MSEL is tied to ground and the DATA0 pin is named DATA.

(3) The nINIT_CONF pin is available on EPC2 devices only. If nINIT_CONF is not available or not used, nCONFIG must be pulled to V_{CC} either directly or through a 1-kΩ resistor.

For more information on FLEX 10K or FLEX 6000 device configuration, go to the following documents:

- *Application Note 59 (Configuring FLEX 10K Devices)*
- *Application Note 87 (Configuring FLEX 6000 Devices)*

FLEX 8000 Device Configuration

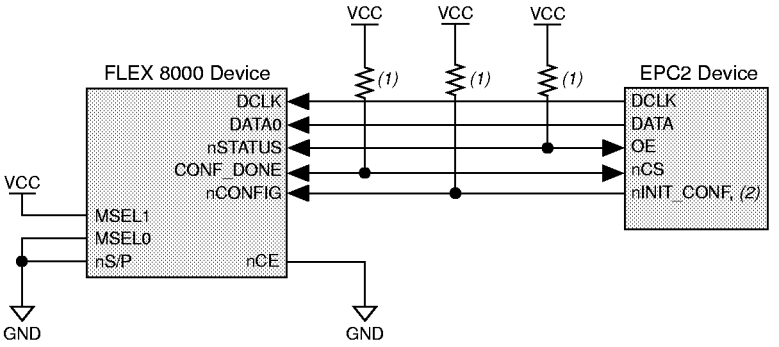
FLEX 8000 devices differ from FLEX 10K and FLEX 6000 devices in that they have internal oscillators that can provide a DCLK signal to the Configuration EPROM. The Configuration EPROM sends configuration data out as a serial bitstream on the DATA output pin. This data is routed into the FLEX 8000 device via the DATA0 input pin. The EPC1, EPC1441, EPC1213, EPC1064, and EPC1064V Configuration EPROMs support this type of configuration.

The EPC1 and EPC1441 can replace the EPC1213, EPC1064, and EPC1064V Configuration EPROMs. The EPC1 or EPC1441 device automatically emulates the EPC1213, EPC1064, or EPC1064V when it is programmed with the appropriate POF. When the EPC1 or EPC1441 device is programmed with an EPC1213, EPC1064, or EPC1064V POF, the FLEX 8000 device drives the EPC1 or EPC1441 device's OE pin high and clocks the EPC1 or EPC1441 device. One EPC1 device can store more configuration data than the EPC1064, EPC1064V, EPC1213, or EPC1441 device. Therefore, designers can use one type of Configuration EPROM for all FLEX devices. In addition, a single EPC1 or EPC1441 device can configure any FLEX 8000 device.

The EPC2 Configuration EPROM can also configure FLEX 8000 devices. EPC2 configuration of FLEX 8000 devices is identical to that of FLEX 10K and FLEX 6000 devices because the EPC2 generates the configuration clock signal. For FLEX 8000 devices, the EPC2 is POF-compatible with the EPC1 but not with the EPC1441, EPC1213, and EPC1064 Configuration EPROMs. To use the EPC2 to configure FLEX 8000 devices, an EPC2 POF can be generated using the **Convert SRAM Object Files** dialog box (File menu) in the MAX+PLUS II Programmer.

For multi-device configuration of FLEX 8000 devices, the nCASC and nCS pins provide handshaking between multiple Configuration EPROMs, allowing several cascaded EPC2, EPC1, or EPC1213 devices to serially configure multiple FLEX 8000 devices. The EPC1441, EPC1064, and EPC1064V do not support data cascading. Figure 7 shows a FLEX 8000 device configured with a single EPC2 Configuration EPROM.

Figure 7. FLEX 8000 Device Configured with an EPC2 Configuration EPROM



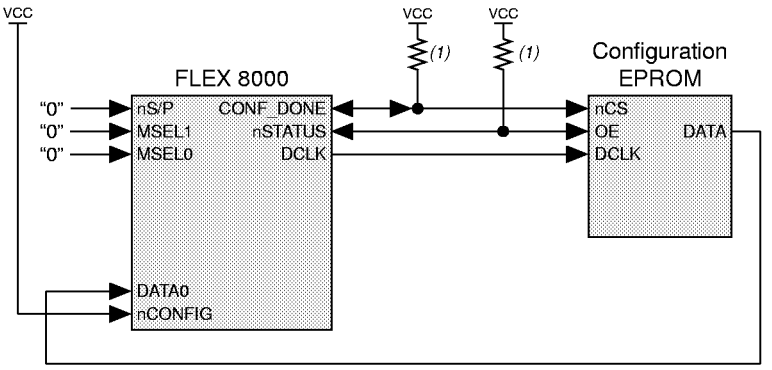
Notes:

(1) All pull-up resistors are 1 kΩ. The OE, nCS, and nINIT_CONF pins on EPC2 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. This EPC2 feature is planned to be available in the MAX+PLUS II version 9.2 software, which is scheduled for release in the first quarter of 1999. In MAX+PLUS II version 9.1, this feature is not available and the internal pull-up resistors on these pins are disabled.

(2) If nINIT_CONF is not used, nCONFIG must still be pulled to V_{CC} either directly or though a 1-kΩ resistor.

Figure 8 shows a FLEX 8000 device configured with a single EPC1, EPC1441, EPC1213, EPC1064, or EPC1064V Configuration EPROM.

Figure 8. FLEX 8000 Device Configured with an EPC1, EPC1441, EPC1213, EPC1064, or EPC1064V Configuration EPROM

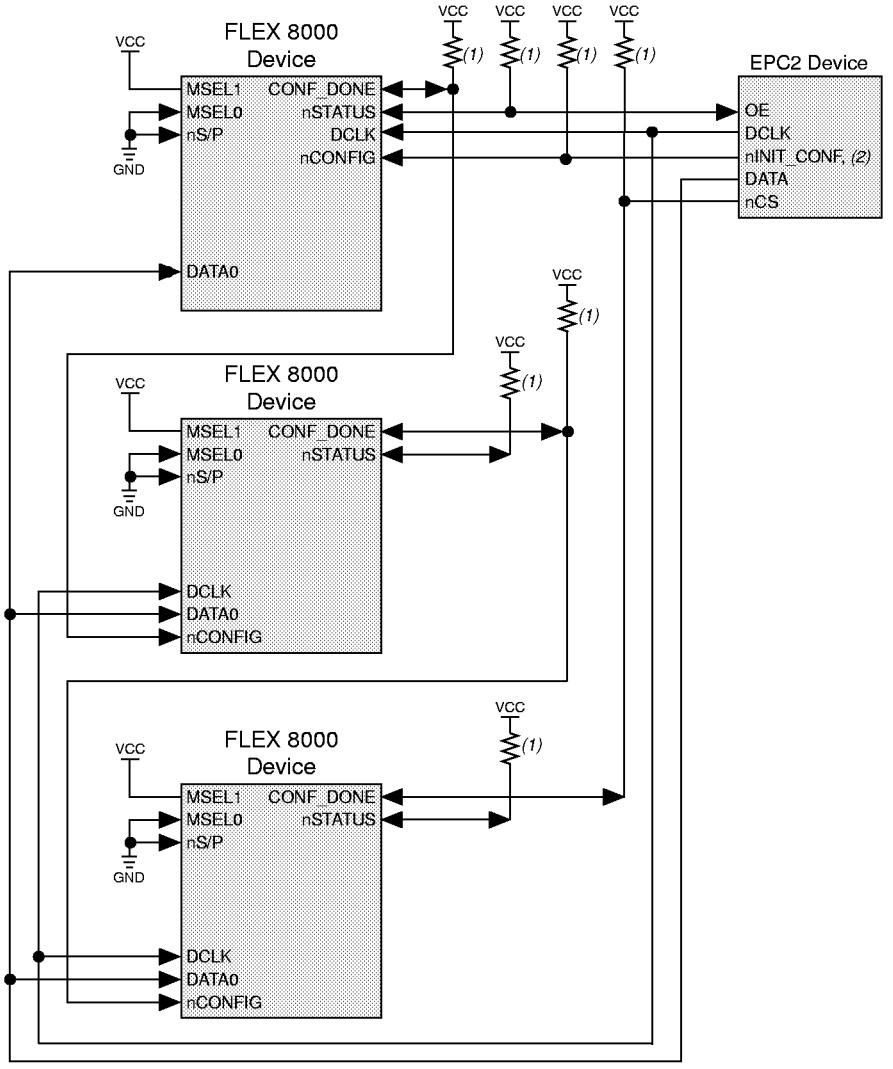


Note:

(1) All pull-up resistors are 1 kΩ.

Figure 9 shows three FLEX 8000 devices configured with a single EPC2 Configuration EPROM.

Figure 9. FLEX 8000 Multi-Device Configuration with an EPC2 Configuration EPROM



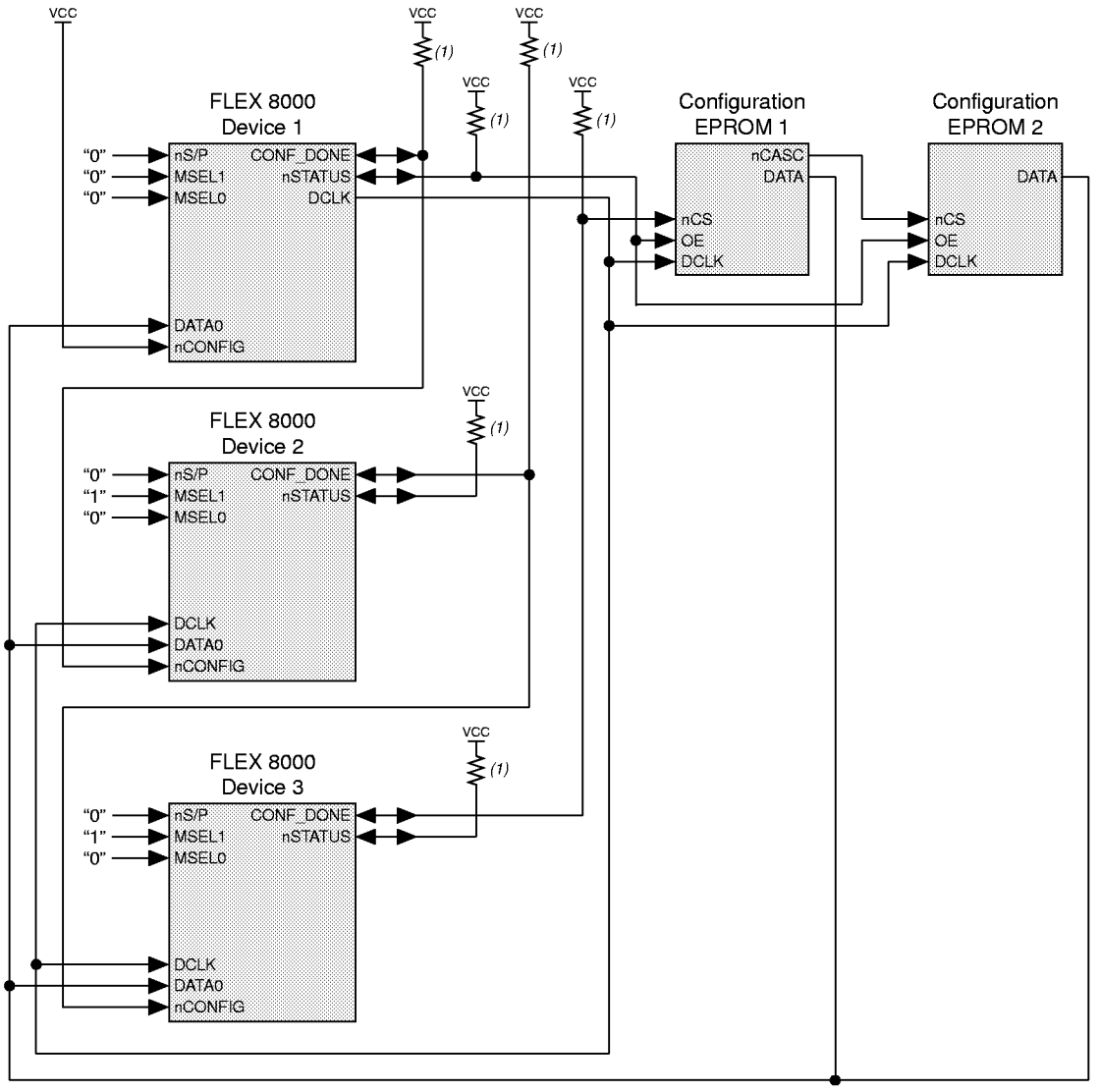
Notes:

(1) All pull-up resistors are 1 kΩ. The `OE`, `nCS`, and `nINIT_CONF` pins on EPC2 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. This EPC2 feature is planned to be available in the MAX+PLUS II version 9.2 software, which is scheduled for release in the first quarter of 1999. In MAX+PLUS II version 9.1, this feature is not available and the internal pull-up resistors on these pins are disabled.

(2) If `nINIT_CONF` is not used, `nCONFIG` must still be pulled to V_{CC} either directly or through a 1-kΩ resistor.

Figure 10 shows three FLEX 8000 devices configured with two EPC1 or EPC1213 Configuration EPROMs.

Figure 10. FLEX 8000 Multi-Device Configuration with Two EPC1 or EPC1213 Configuration EPROMs



Note:
(1) All pull-up resistors are 1 kΩ.

Table 4 describes the pin functions of all Configuration EPROMs during FLEX 8000 device configuration.

Table 4. Configuration EPROM Pin Functions During FLEX 8000 Device Configuration (Part 1 of 2)

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP *Note (1)*	20-Pin PLCC	32-Pin TQFP *Note (2)*		
DATA	1	2	31	Output	Serial data output. The DATA pin is tri-stated before configuration when its nCE pin is high and after the Configuration EPROM finishes sending its configuration data. This operation is independent of the device's position in the cascade chain.
DCLK	2	4	2	Input	Clock output when configuring with a single EPC2 device or when the EPC2 is the first device in a Configuration EPROM chain. DCLK is a clock input for subsequent EPC2 devices in a Configuration EPROM chain. DCLK is a clock input when using EPC1, EPC1213, EPC1064, and EPC1064V Configuration EPROMs. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the OE input is held high, the nCS input is held low, and all configuration data has not been transferred to the target device. When configuring with a single EPC2 device or with the first EPC2 device in a Configuration EPROM chain, the EPC2 DCLK pin drives low after configuration is complete or when OE is low.
OE, *Note (3)*	3	8	7	Input	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count.
nCS, *Note (4)*	4	9	10	Input	Chip-select input (active low). A low input allows DCLK to increment the address counter and enables DATA.
nCASC, *Notes (3), (5)*	6	12	15	Output	Cascade-select output (active low). This output goes low when the address counter has reached its maximum value. The nCASC output is usually connected to the nCS input of the next device in a configuration chain, so the next DCLK clocks data out of the next device.
nINIT_CONF, *Notes (3), (5), (6)*	–	13	16	Output	Allows the INIT_CONF JTAG instruction to initiate configuration. This pin is connected to the nCONFIG pin of the FLEX device to initiate configuration from the EPC2 via a JTAG instruction. If a chain of EPC2 devices is used, only the first EPC2 has its nINIT_CONF pin tied to the FLEX device's nCONFIG pin. *Note (7)*

Table 4. Configuration EPROM Pin Functions During FLEX 8000 Device Configuration (Part 2 of 2)

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP *Note (1)*	20-Pin PLCC	32-Pin TQFP *Note (2)*		
TDI, *Note (6)*	–	11	13	Input	JTAG data input pin. Connect this pin to V_{CC} if the JTAG circuitry is not used.
TDO, *Note (6)*	–	1	28	Output	JTAG data output pin. Do not connect this pin if the JTAG circuitry is not used.
TMS, *Note (6)*	–	19	25	Input	JTAG mode select pin. Connect this pin to V_{CC} if the JTAG circuitry is not used.
TCK, *Note (6)*	–	3	32	Input	JTAG clock pin. Connect this pin to ground if the JTAG circuitry is not used.
VCCSEL, *Note (6)*	–	5	3	Input	Mode select for V_{CC} supply. VCCSEL must be connected to ground if the device uses a 5.0-V power supply (i.e., V_{CC} = 5.0 V). VCCSEL must be connected to V_{CC} if the device uses a 3.3-V power supply (i.e., V_{CC} = 3.3 V).
VPPSEL, *Note (6)*	–	14	17	Input	Mode select for VPP. VPPSEL must be connected to ground if VPP operates off of a 5.0-V power supply (i.e., VPP = 5.0 V). VPPSEL must be connected to V_{CC} if VPP uses a 3.3-V power supply (i.e., VPP = 3.3 V).
VPP	–	18	23	Power	Programming power pin. For the EPC2 device, this pin is normally tied to V_{CC}. If the EPC2 V_{CC} is a 3.3-V supply, VPP can be tied to 5.0 V to improve in-system programming times. For all other Configuration EPROMs, VPP must be tied to V_{CC}.
VCC	7, 8	20	27	Power	Power pin.
GND	5	10	12	Ground	Ground pin. A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.

Notes:

(1) This package is available for EPC1, EPC1441, EPC1213, EPC1064, and EPC1064V devices only.
(2) This package is available for EPC2, EPC1441, EPC1064, and EPC1064V devices only.
(3) The OE, nCS, and nINIT_CONF pins on EPC2 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. This EPC2 feature is planned to be available in the MAX+PLUS II version 9.2 software, which is scheduled for release in the first quarter of 1999. In MAX+PLUS II version 9.1, the internal pull-up resistors on these pins are disabled.
(4) The EPC1441, EPC1064, and EPC1064V devices do not support data cascading. The EPC2, EPC1, and EPC1213 devices support data cascading for FLEX 8000 devices.
(5) The nCASC and nINIT_CONF pins are planned to be supported for EPC2 devices in the MAX+PLUS II version 9.2 software.
(6) This pin applies to EPC2 devices only.
(7) This instruction is planned to be supported in the MAX+PLUS II version 9.2 software.

For more information on FLEX 8000 device configuration, go to the following documents:

- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

Power & Operation

The following section describes Power-On Reset (POR) delay, error detection, and 3.3-V and 5.0-V operation of Altera Configuration EPROMs.

Power-On Reset

During initial power-up, a POR delay occurs to permit voltage levels to stabilize. When configuring a FLEX 10K or FLEX 6000 device with an EPC2, EPC1, or EPC1441 device, the POR delay occurs inside the Configuration EPROM. However, when configuring a FLEX 8000 device with an EPC1213, EPC1064, or EPC1064V device, the POR delay occurs inside the FLEX 8000 device. In either case, the POR delay is typically 100 ms, with a maximum of 200 ms.

Error Detection Circuitry

The EPC2, EPC1, and EPC1441 Configuration EPROMs have built-in error detection circuitry. The EPC2 Configuration EPROM's error-detection circuitry functions with all FLEX devices, whereas the EPC1 and EPC1441 Configuration EPROM's error-detection circuitry only functions when configuring FLEX 10K and FLEX 6000 devices.

Built-in error-detection circuitry uses the nCS pin of the Configuration EPROM, which monitors the CONF_DONE pin on the FLEX device. An error condition occurs if the CONF_DONE pin does not go high after all the configuration data has been sent, or if the CONF_DONE pin goes high before the Configuration EPROM has completed sending configuration data. When an error condition occurs, the Configuration EPROM drives its OE pin low, which drives the FLEX device's nSTATUS pin low, indicating an error. After an error, configuration automatically restarts if the *Auto-Restart Configuration on Frame Error* option is turned on in the **Global Project Device Options** dialog box (Assign menu) in the MAX+PLUS II software.

In addition, if the FLEX device detects a cyclic redundancy code (CRC) error in the received data, it may also flag the error by driving nSTATUS low. This low signal on nSTATUS resets the Configuration EPROM, allowing reconfiguration. CRC checking is performed when configuring all FLEX devices.

3.3-V or 5.0-V Operation

EPC2, EPC1, and EPC1441 devices can configure FLEX devices with either a 5.0-V, 3.3-V, or 2.5-V supply voltage. For each Configuration EPROM, an option must be set for 5.0-V or 3.3-V operation. For EPC1 and EPC1441 Configuration EPROMs, the *Use Low-Voltage Configuration EPROM* option in the **Global Project Device Options** dialog box (Assign menu) in the MAX+PLUS II software sets this parameter. For EPC2 devices, this option is set externally by the VCCSEL pin. In addition, the EPC2 device has an externally controlled option, set by the VPPSEL pin, to adjust the programming voltage to 5.0 V or 3.3 V.

The functions of the VCCSEL and VPPSEL pins are described below.

- VCCSEL pin—For EPC2 Configuration EPROMs, 5.0-V or 3.3-V operation is controlled by the VCCSEL option pin. The device functions in 5.0-V mode when VCCSEL is connected to GND; the device functions in 3.3-V mode when VCCSEL is connected to V_{CC}.

- VPPSEL pin—The EPC2 VPP programming power pin is normally tied to V_{CC}. For EPC2 devices operating with a 3.3-V supply, it is possible to improve EPC2 in-system programming times by providing VPP with a 5.0-V supply. For all other EPROMs, VPP must be tied to V_{CC}. The EPC2 device's VPPSEL pin must be set in accordance with the EPC2 VPP pin. If the VPP pin is supplied by a 5.0-V supply, VPPSEL must be connected to GND; if the VPP pin is supplied by a 3.3-V power supply, VPPSEL must be connected to V_{CC}.

Table 5 describes the relationship between the V_{CC} and V_{PP} voltage levels and the required logic level for VCCSEL and VPPSEL (i.e., high or low logic level).

Table 5. VCCSEL & VPPSEL Pin Functions on the EPC2

V_{CC} Voltage Level (V)	V_{PP} Voltage Level (V)	VCCSEL Pin Logic Level	VPPSEL Pin Logic Level
3.3	3.3	High	High
3.3	5.0	High	Low
5.0	5.0	Low	Low

For EPC1 and EPC1441 Configuration EPROMs, 3.3-V or 5.0-V operation is controlled by a programming bit in the POF. The programming bit value is determined by the core supply voltage of the targeted device during design compilation with the MAX+PLUS II software. For example, EPC1 devices are programmed automatically to operate in 3.3-V mode when configuring FLEX 10KA devices, which have a V_{CC} voltage of 3.3 V. In this example, the EPC1 device's VCC pin is connected to a 3.3-V power supply.

Designers may choose to set the Configuration EPROM for low voltage when using the MultiVolt™ feature, which allows a FLEX device to bridge between systems operating with different voltages. When compiling for 3.3-V FLEX 6000 devices, set the Configuration EPROM for low-voltage operation. To set the EPC1 and EPC1441 Configuration EPROMs for low-voltage operation, turn on the *Low-Voltage I/O* option in the **Global Project Device Options** dialog box (Assign menu) in the MAX+PLUS II software.

Configuration Chain with Multiple Voltage Levels

An EPC2 or EPC1 device can configure a chain of FLEX devices with multiple voltage levels. All 3.3-V and 2.5-V FLEX devices can be driven by higher-voltage signals.

When configuring a mixed-voltage chain of FLEX devices, the devices' VCCINT and VCCIO pins may be connected to 2.5 V, 3.3 V, or 5.0 V, depending upon the device. The Configuration EPROM may be powered at 3.3 V or 5.0 V. If an EPC1, EPC1441, EPC1213, EPC1064, or EPC1064V Configuration EPROM is powered at 3.3 V, the nSTATUS and CONF_DONE pull-up resistors must be connected to 3.3 V. If these Configuration EPROMs are powered at 5.0 V, the nSTATUS and CONF_DONE pull-up resistors can be connected to 3.3 V or 5.0 V.

At 3.3-V operation, all EPC2 inputs are 5.0-V tolerant, except DATA, DCLK, nCASC, and TDO. The DATA, DCLK, and nCEO pins are used only to interface between the EPC2 and the FLEX device it is configuring; TDO is an output only. The voltage tolerances of all EPC2 pins at 5.0 V and 3.3 V are listed in Table 6.

Table 6. EPC2 Input & Bidirectional Pin Voltage Tolerance

Pin	5.0-V Operation		3.3-V Operation	
	5.0-V Tolerant	3.3-V Tolerant	5.0-V Tolerant	3.3-V Tolerant
DATA	✓	✓		✓
DCLK	✓	✓		✓
nCASC	✓	✓		✓
OE	✓	✓	✓	✓
nCS	✓	✓	✓	✓
VCCSEL	✓	✓	✓	✓
VPPSEL	✓	✓	✓	✓
nINIT_CONF	✓	✓	✓	✓
TDI	✓	✓	✓	✓
TMS	✓	✓	✓	✓
TCK	✓	✓	✓	✓
TDO	✓	✓		✓

For more information on FLEX 10K, FLEX 8000, and FLEX 6000 devices, go to the following documents:

- *FLEX 10K Embedded Programmable Logic Family Data Sheet*
- *FLEX 10KE Embedded Programmable Logic Family Data Sheet*
- *FLEX 8000 Programmable Logic Device Family Data Sheet*
- *FLEX 6000 Programmable Logic Device Family Data Sheet*

MAX+PLUS II Programming & Configuration File Support

The MAX+PLUS II development system provides programming support for Altera Configuration EPROMs. The MAX+PLUS II software automatically generates a POF to program each Configuration EPROM in a project. In a multi-device project, the MAX+PLUS II software can combine the programming files for multiple FLEX devices into one or more Configuration EPROMs. The MAX+PLUS II software allows you to select the appropriate Configuration EPROM to most efficiently store the data for each FLEX device. Moreover, when compiling for FLEX 10KA or FLEX 10KE devices, the MAX+PLUS II software automatically defaults to generate the EPC1 or EPC1441 POF with the programming bit set for 3.3-V operation.

All of Altera's Configuration EPROMs are programmable using Altera programming hardware in conjunction with the MAX+PLUS II software. In addition, many manufacturers offer programming hardware that supports other Altera Configuration EPROMs.

The EPC2 Configuration EPROM can be programmed in-system through its industry-standard 4-pin JTAG interface. ISP capability in the EPC2 provides ease in prototyping and updating FLEX device functionality. The EPC2 Configuration EPROM can be programmed in-system via test equipment using SVF Files, Jam Files (**.jam**), or Jam Byte-Code Files (**.jbc**), embedded processors using the Jam programming and test language, and the MAX+PLUS II software via the ByteBlasterMV, ByteBlaster, or BitBlaster download cables. When programming multiple EPC2 devices in a JTAG chain, the MAX+PLUS II software and other programming methods employ concurrent programming to simultaneously program multiple devices and reduce programming time.

After programming an EPC2 device in-system, FLEX device configuration can be initiated by including the EPC2 JTAG configuration instruction. See Table 7 on page 23.

For more information, go to the following documents:

- *Altera Programming Hardware Data Sheet*
- *Programming Hardware Manufacturers*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *ByteBlaster Parallel Port Download Cable Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*

IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing

The EPC2 provides JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. The EPC2 supports the JTAG instructions shown in Table 7.

Table 7. EPC2 JTAG Instructions

JTAG Instruction	Description	Instruction
SAMPLE/PRELOAD	Allows a snapshot of a signal at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.	0001010101
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing results at the input pins.	0000000000
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.	1111111111
IDCODE	Selects the device IDCODE register and places it between TDI and TDO, allowing the device IDCODE to be serially shifted out of TDO. The device IDCODE for the EPC2 is shown below: 0000 0001 0000 0000 0010 00001101110 0	0001011001
UESCODE	Selects the UESCODE register and places it between TDI and TDO, allowing the UESCODE to be serially shifted out of TDO. The 32-bit UESCODE is a programmable user-defined pattern.	0001111001
ISP Instructions	These instructions are used when programming an EPC2 device via JTAG ports with a ByteBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam File (**.jam**), Jam Byte-Code File (**.jbc**), or SVF File via an embedded processor.	–
INIT_CONF	This function allows the user to initiate the FLEX configuration process by tying nINIT_CONF to the FLEX device(s) nCONFIG pin(s). After this instruction is updated, the nINIT_CONF pin is driven low. When the Initiate Configuration instruction is cleared, nINIT_CONF is released, which starts the FLEX device configuration.	0001100001

For more information, go to the following documents:

- *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *ByteBlaster Parallel Port Download Cable Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*

Figure 11 shows the timing requirements for the JTAG signals.

Figure 11. EPC2 JTAG Waveforms

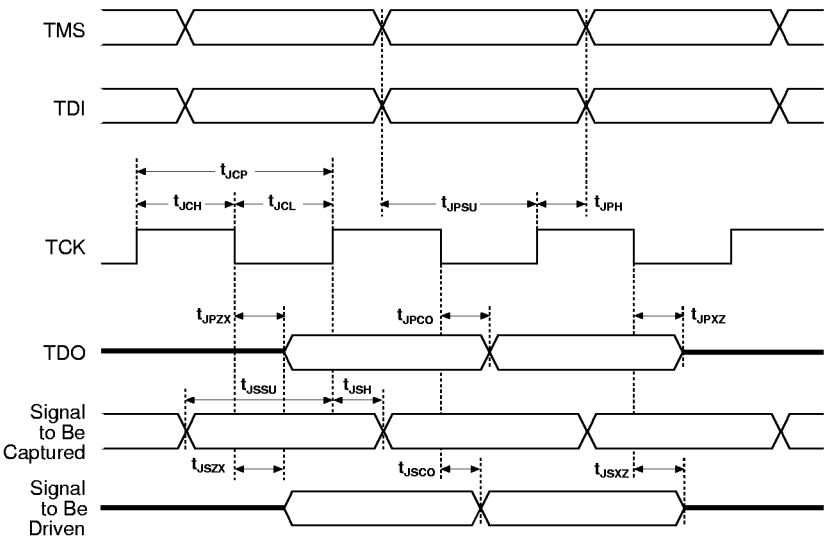


Table 8 shows the timing parameters and values for Configuration EPROM devices.

Table 8. JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high-impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

Operating Conditions

The following tables provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for Configuration EPROM devices.

Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground, *Note (2)*	–2.0	7.0	V
V_I	DC input voltage	With respect to ground, *Note (2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or ground current			50	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			250	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage for 5.0-V operation	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for 3.3-V operation	*Notes (3), (4)*	3.0 (3.0)	3.6 (3.6)	V
V_I	Input voltage	With respect to ground, *Note (2)*	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns

DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V mode high-level TTL output voltage	I_{OH} = –4 mA DC, *Note (7)*	2.4		V
	3.3-V mode high-level CMOS output voltage	I_{OH} = –0.1 mA DC, *Note (7)*	V_{CC} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (7)*		0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or ground	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or ground	–10	10	µA

EPC1213, EPC1064 & EPC1064V Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			100	200	µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 6 MHz		10	50	mA

EPC2 Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)	V_{CC} = 5.0 V or 3.3 V		50	100	µA
I_{CC1}	V_{CC} supply current (during configuration)	V_{CC} = 5.0 V or 3.3 V		18	50	mA

EPC1 Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			50	100	µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 10 MHz, *Note (8)* V_{CC} = 5.0 V		30	50	mA
I_{CC2}	V_{CC} supply current (during configuration)	DCLK = 5 MHz, *Note (8)* V_{CC} = 3.3 V		10	16.5	mA

EPC1441 Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			30	60	µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 10 MHz, *Note (8)* V_{CC} = 5.0 V		15	30	mA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 5 MHz, *Note (8)* V_{CC} = 3.3 V		5	10	mA

Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

FLEX 10K & FLEX 6000 Device Configuration Parameters Using EPC2, EPC1 & EPC1441 Devices
FLEX 8000 Device Configuration Parameters Using EPC2 Devices

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CE}	OE high to first clock delay				200	ns
t_{OEZX}	OE high to data output enabled				160	ns
t_{CO}	DCLK to data out delay				30	ns
t_{MCH}	DCLK high time for the first device in the configuration chain		30	50	150	ns
t_{MCL}	DCLK low time for the first device in the configuration chain		30	50	150	ns
t_{SCH}	DCLK high time for subsequent devices		30			ns
t_{SCL}	DCLK low time for subsequent devices		30			ns
t_{CASC}	CLK rising edge to nCASC				20	ns
t_{CCA}	nCS to nCASC cascade delay				10	ns
f_{CDOE}	CLK to data enable/disable				30	ns
t_{OEC}	OE low to CLK disable delay				45	ns
t_{NRCAS}	OE low (reset) to nCASC delay				25	ns
t_{NRR}	OE low time (reset) minimum		100			ns

FLEX 8000 Device Configuration Parameters Using EPC1, EPC1441, EPC1213, EPC1064 & EPC1064V Devices

			EPC1064V		EPC1064 EPC1213		EPC1 EPC1441		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{OEZX}	OE high to DATA output enabled			75		50		50	ns
t_{CSZX}	nCS low to DATA output enabled			75		50		50	ns
t_{CSXZ}	nCS high to DATA output disabled			75		50		50	ns
t_{CSS}	nCS low setup time to first DCLK rising edge		150		100		50		ns
t_{CSH}	nCS low hold time after DCLK rising edge		0		0		0		ns
t_{DSU}	Data setup time before rising edge on DCLK		75		50		50		ns
t_{DH}	Data hold time after rising edge on DCLK		0		0		0		ns
t_{CO}	DCLK to DATA out delay			100		75		75	ns
t_{CK}	Clock period		240		160		100		ns
f_{CK}	Clock frequency			4		6		8	MHz
t_{CL}	DCLK low time		120		80		50		ns
t_{CH}	DCLK high time		120		80		50		ns
t_{XZ}	OE low or nCS high to DATA output disabled			75		50		50	ns
t_{OEW}	OE pulse width to guarantee counter reset		150		100		100		ns
t_{CASC}	Last DCLK + 1 to nCASC low delay			90		60		50	ns
t_{CKXZ}	Last DCLK + 1 to DATA tri-state delay			75		50		50	ns
t_{CEOUT}	nCS high to nCASC high delay			150		100		100	ns

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified under "Recommended Operating Conditions" on page 25.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(8) Maximum DCLK for EPC2, EPC1, and EPC1441 devices is 8 MHz when V_{CC} is 5.0 V, and 5 MHz when V_{CC} is 3.3 V.
(9) Capacitance is sample-tested only.

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Figure 1. 8-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 764 of this data sheet for dimension formats.

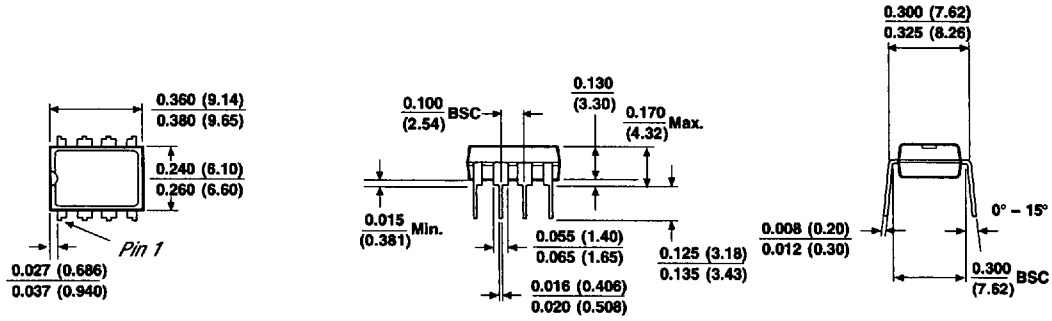
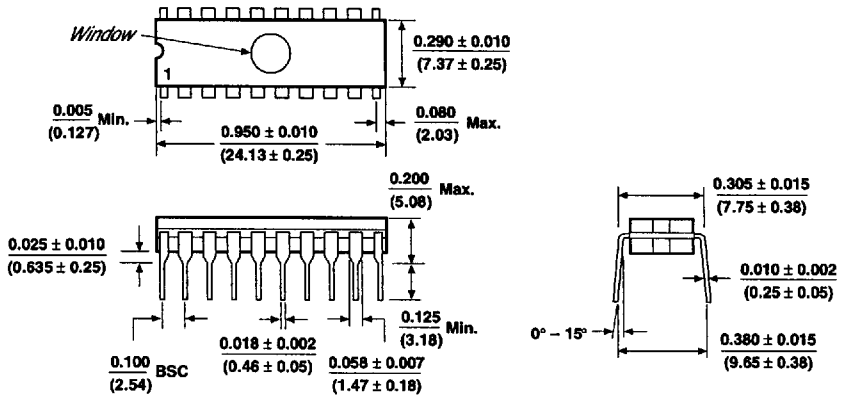


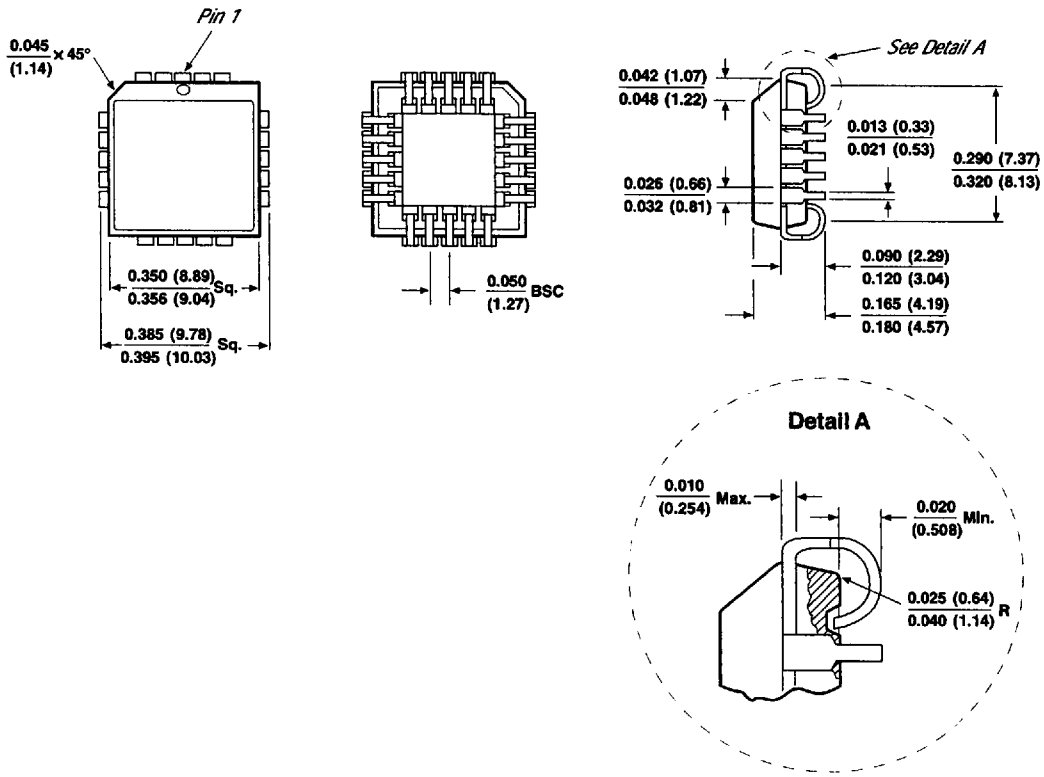
Figure 2. 20-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 764 of this data sheet for dimension formats.



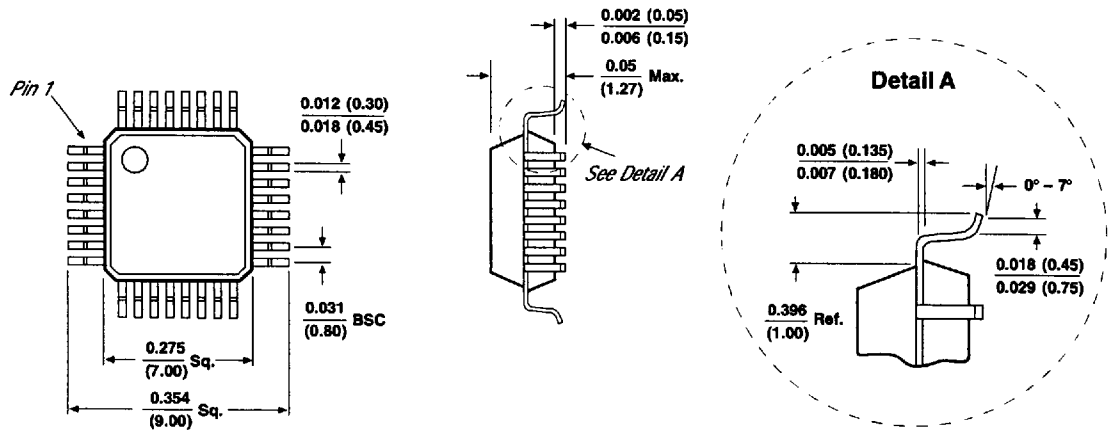
20-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 764 of this data sheet for dimension formats.



32-Pin Plastic Thin Quad Flat Pack (TQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 764 of this data sheet for dimension formats



40-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 764 of this data sheet for dimension formats.