SIEMENS

HYB 514100BJ/BT -50/-60/-70
4 194 304 x 1 - Bit Dynamic RAM

HYB 514400BJ/BT -50/-60/-70
1 048 576 x 4 - Bit Dynamic RAM

INFORMATION NOTE

Soft Error Sensitivity (SER)

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This information note is intended to provide technical information on the SIEMENS 4M x 1 and 1M x 4 bit dynamic access memories HYB 514100BJ/BT and HYB 514400BJ/BT.

DEFINITION OF SOFT ERRORS

Soft errors are spurious fails of Integrated Circuits especially known with memory products. They are ultimately caused by α - particles originating from materials used to fabricate the component, e.g. moulding compound, chip carrier or the aluminium on the die itself.

The functional failure is strictly temporary than permanent and does not influence the long term reliability of the product.

PHYSICAL FAILURE MECHANISM

Alpha particles (α's) are doubly charged helium nuclei emitted in the radioactive decay of heavy elements. Naturally occurring α's range in energy from about 2 to 9 MeV and are treated as classical particles.

An α interacts electronically with silicon creating a track of electron - hole pairs along the 25 μm straight line path of the particles.

The SIEMENS 4Mx1 and 1Mx4 DRAMS are new generation dynamic RAMS using a triple polysilicon gate CMOS process and trench-type memory cells.

The digital information is stored as charge on the trench-capacitor and must be periodically refreshed as usual.

Whether or not sufficient charge is collected from the track to upset either cells or sensing depends on the total stored charge, noise margins, α - particle energy and collection efficiency.

DESIGN FOR LOW SOFT ERROR RATE

The memory cell array is built up with trench-type storage capacitors with a capacitance higher than 40 femtoFarads. Molybdenum silicide is used as the main bitline material to further reduce α - particle sensitivity due to significant reduction of charge collection efficiency.

The chip is additionally coated with a thin Polyimid layer and a low stress moulding compound with low radiation is used.

Consequently much care has to be taken to control the radioactivity from process materials as aluminium or silicides. Periodic sampling of all materials used in the process guarantees comparable low contamination.

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SOFT ERROR TESTING METHODS

Two practical methods to test for Soft Error Sensitivity are known:

1. Soft Error Lifetest

Hundreds of finished memory parts are run in a Dynamic Monitoring Burn-In System for a total of several million device hours under realistic operation conditions. As a result the specific Soft Error Rate (SER) can be given in FIT (events per 10^9 device hours).

2. Accelerated Soft Error Test

Few chips with partial removed compound and without Polyimid die coat are submitted to the irradiation of an artificial α - source while the functionality of the device is continuously monitored by an automated test equipment.

As a result only relative comparison between different parts can be obtained. However this test can also be used to derive the Accelerated Soft Error Rate (ASER) and accelerating factors for different voltages, temperatures, cycle times, data pattern or other operation parameters.

SOFT ERROR RATE DEFINITION

SIEMENS defines the Soft Error Rate for dynamic MOS memories as the failure rate in a monitoring burn-in system derated to the following standard conditions :

$$
\begin{aligned}
t_{RC} &= 1\mu s & \text{memory cycle time} \\
VCC &= 5.0 \text{ Volts} & \text{standard supply voltage} \\
T_a &= 40 \text{ deg.C} & \text{ambient temperature}
\end{aligned}
$$

Since SER's of modern DRAM are extremely low it is often too expensive and time consuming to actually run the test under these conditions. Therefore the following accelerated conditions are frequently applied :

short cycle time	e.g. 500 ns
lower supply voltage	e.g. 4.5 Volts

The actual derated SER is then calculated using the results from accelerated soft error studies with artificial α - sources.

3

SER RESULTS OF 4Mx1 and 1MX4 DRAM ("third generation")

1. A typical Soft Error Test was carried out with 2048 parts randomly selected from three different production lots run for 1091 hours (2,235 millions device hours) at 40°C , VCC=4.5V and cycle time of t_{RC} = 500 ns. An unscrambled checkerboards data pattern has been used for this test.

   Three soft errors were observed during this time resulting in a gross SER of **1342** FIT or an SER of **1870** when calculating with an 60% confidence level (fig.1).

Field Soft Error Test
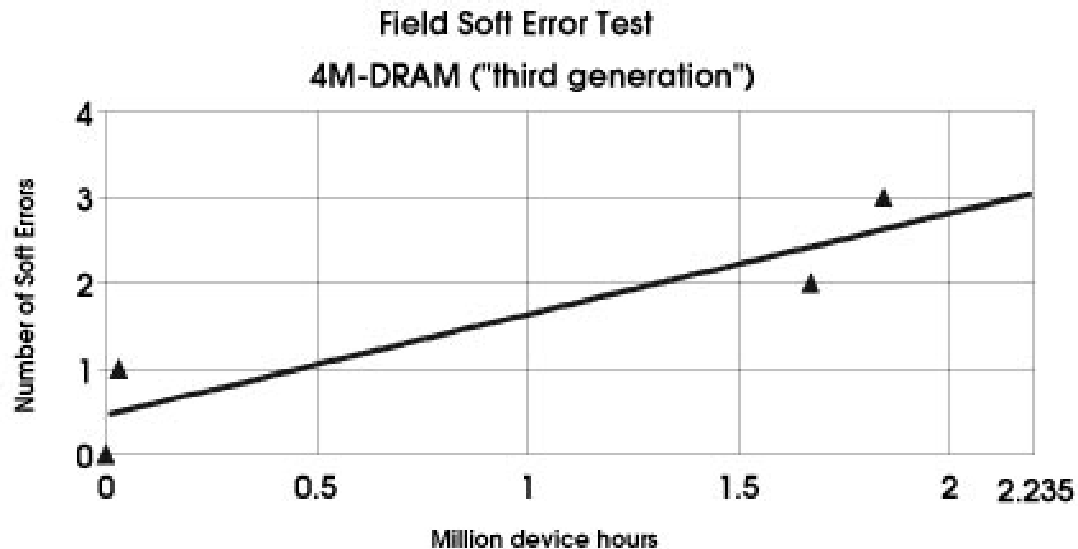### 4M-DRAM ("third generation")

Million device hours

fig.1

2. Accelerated soft error rate (ASER) tests with an unscrambled checkerboard data pattern shows a factor of 5 for a Radium - 226 source between tests at 500ns / 4.5 Volts and standard conditions .

3. The SER for standard conditions (VCC = 5V and t_{RC} = 1 µs) now becomes:

$$SER = 270 \ FIT$$

   and **SER** < **380** FIT when a 60% confidence level is taken into account.

4. As discussed before the SER consists of cell hits and bitline hits due to α - particles. As shown in fig. 2 and 3 the accelerated soft error rate for a stored "1" - information is nearly independent from cycle time in the range of 200ns to 10µs. (Since the memory chips are decapsulated during this test and no refresh was performed the ASER-rate for the stored "1" - information slightly increased). The stored "0" - information can only be destroys within few nanoseconds in evvery memory cycle. Therefore the ASER-rate for the stored "0" - decreases more than one magnitudes between 200ns and 10µs cycle time.
   The more realistic situation with a checkerboard data pattern therefore also shows a decrease of ASER-rate with cycle time.
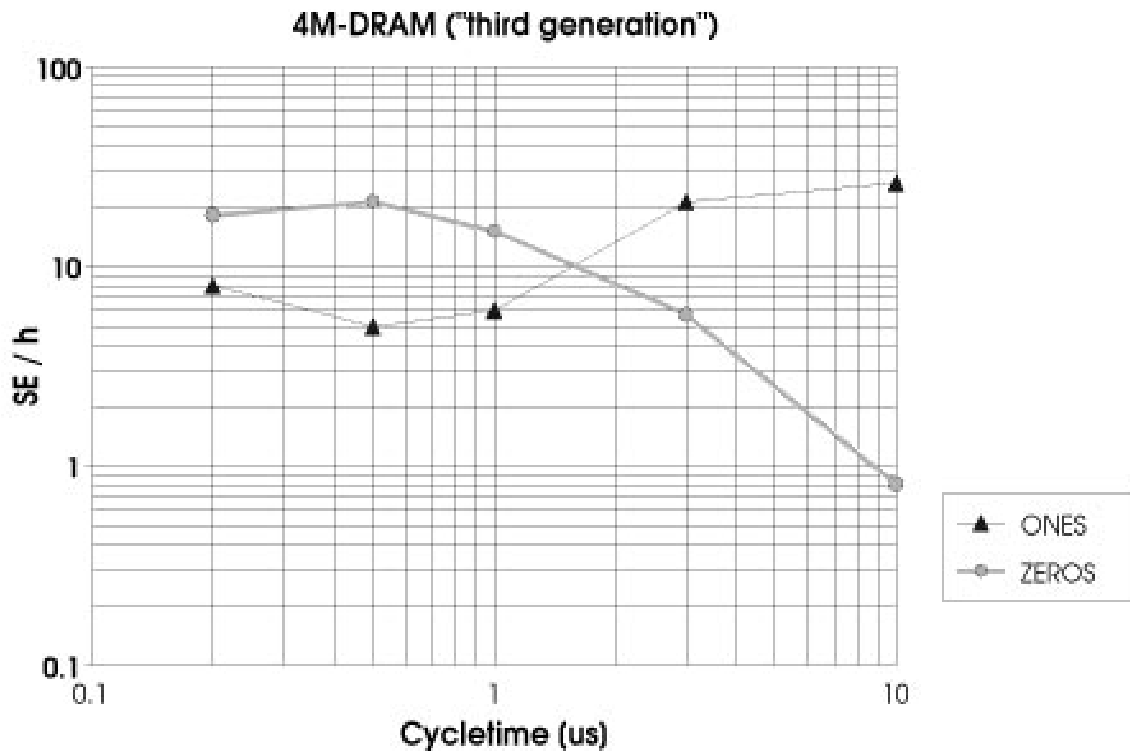
4M-DRAM ("third generation")

fig.2 Cycletime dependence of ASER-rate (VCC=4.5V,R.T.,RA226-source)
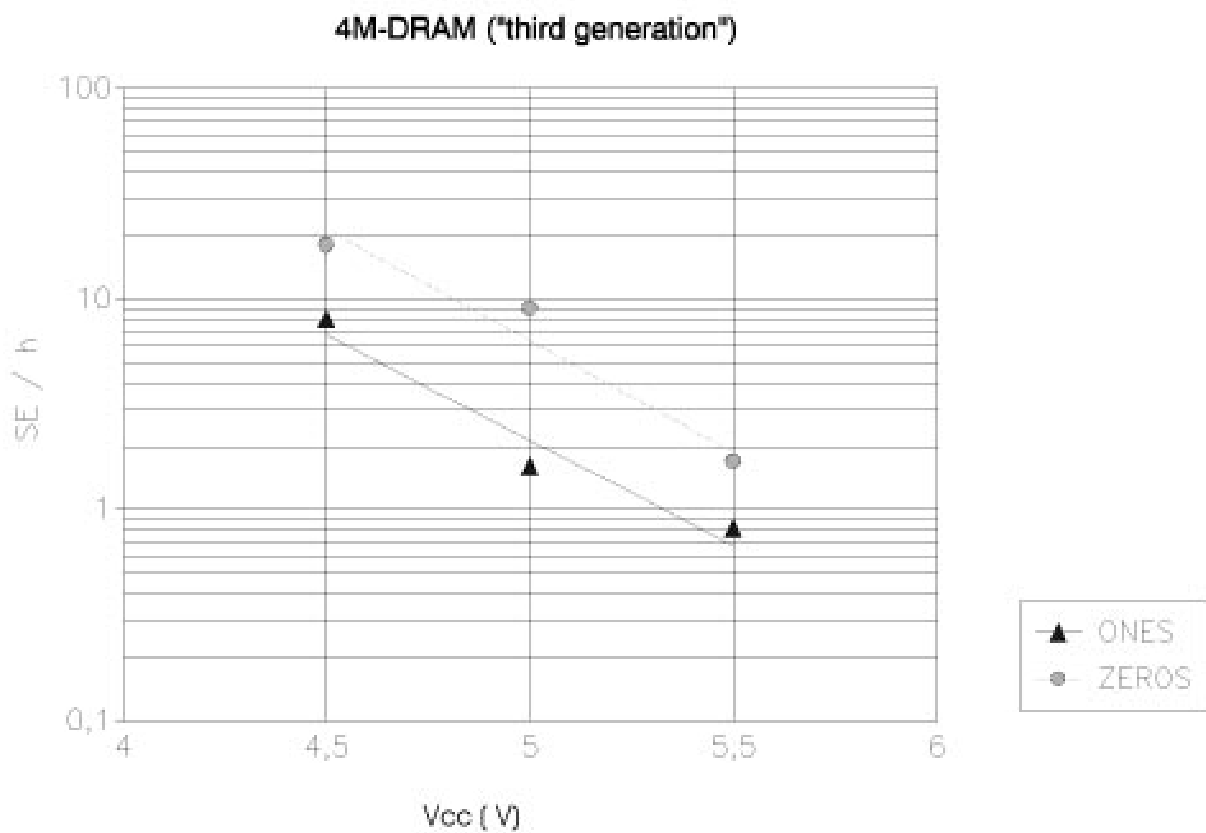
4M-DRAM ("third generation")

fig.3 Voltage dependence of ASER-rate (tc = 200 ns , R.T., RA 226-source)

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**4M-DRAM Design Step B
"third generation"
FIELD SOFT ERROR TEST**

Testequipment :   Monitoring Burn-in System (Aehr Test)

No. of devices :   2048 HYB 514100 BJ   (4Mx1 DRAMS)

Testconditions :   VCC   =   4.5 Volts
                          t_{RC} =   500 ns
                          Data Pattern=   Checkerboard (unscrambled)
                          Test Pattern =   Read Only
                          T_{AMB} =   40 ^{o}C

Testresult :   3 Soft Erros within
                          2,235 million device hours

SER_{test} < 1870 FIT (60% confidence level)

Normalized to nominal conditions :
 (5 Volts / 1.0 μs)

SER   < 380 FIT   (60% confidence level)

Field Soft Error Rate