



Integrated Device Technology, Inc.

128K x 32 CMOS STATIC RAM MODULES

IDT7MP4060
IDT7MP4095

FEATURES:

- High density 4 megabit static RAM modules
- Low profile 64-pin ZIP (Zig-zag In-line vertical Package), 64-lead, 72-lead SIMMs (Single In-line Memory Modules)
- Fast access time: 15ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V ($\pm 10\%$) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible
- Gold plated fingers on the SIMM version

PIN CONFIGURATION – 7MP4095

	1	GND	PD ₀ - OPEN
PD ₀	2	3	PD ₁ - OPEN
I/O ₀	4	5	I/O ₈
I/O ₁	6	7	I/O ₉
I/O ₂	8	9	I/O ₁₀
I/O ₃	10	11	I/O ₁₁
VCC	12	13	A ₀
A ₇	14	15	A ₁
A ₈	16	17	A ₂
A ₉	18	19	I/O ₁₂
I/O ₄	20	21	I/O ₁₃
I/O ₅	22	23	I/O ₁₄
I/O ₆	24	25	I/O ₁₅
I/O ₇	26	27	GND
\overline{WE}	28	29	A ₁₅
A ₁₄	30	31	\overline{CS}_2
\overline{CS}_1	32		
\overline{CS}_3	33	\overline{CS}_4	
A ₁₆	34	35	NC
GND	36	37	\overline{OE}
I/O ₁₆	38	39	I/O ₂₄
I/O ₁₇	40	41	I/O ₂₅
I/O ₁₈	42	43	I/O ₂₆
I/O ₁₉	44	45	I/O ₂₇
A ₁₀	46	47	A ₃
A ₁₁	48	49	A ₄
A ₁₂	50	51	A ₅
A ₁₃	52	53	VCC
I/O ₂₀	54	55	A ₆
I/O ₂₁	56	57	I/O ₂₈
I/O ₂₂	58	59	I/O ₂₉
I/O ₂₃	60	61	I/O ₃₀
GND	62	63	I/O ₃₁
	64		

**ZIP, SIMM
TOP VIEW**

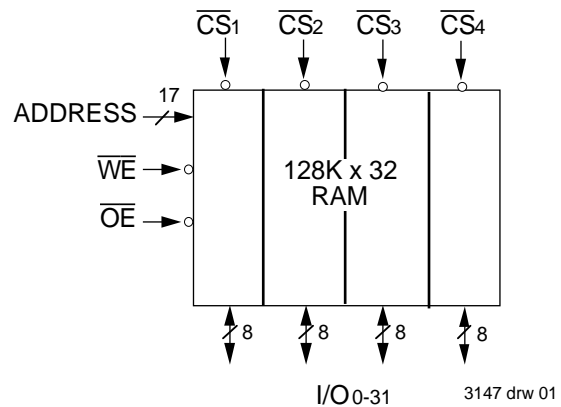
DESCRIPTION:

The IDT7MP4095/7MP4060 are 128K x 32 static RAM modules constructed on an epoxy laminate (FR-4) substrate using four 128K x 8 static RAMs in plastic SOJ packages. The IDT7MP4095/7MP4060 are available with access times as fast as 15ns with minimal power consumption.

The IDT7MP4095 is packaged in a 64-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64-lead SIMM (Single In-line Memory Module). The IDT7MP4060 is packaged in a 72-lead SIMM. The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.21 inches thick. At only 0.60 inches high, this low-profile package is ideal for systems with minimum board spacing, while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4095/7MP4060 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₆	Addresses
\overline{CS}_1-4	Chip Selects
\overline{WE}	Write Enable
\overline{OE}	Output Enable
VCC	Power
GND	Ground
NC	No Connect

3147 tbl 01

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COMMERCIAL TEMPERATURE RANGE

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For latest information contact IDT's web site at www.idt.com or fax-on-demand at 408-492-8391. **7.09**

DSC-3147/7

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PIN CONFIGURATION – 7MP4060

NC	2	1	NC
PD3	4	3	PD2
PD0	6	5	GND
I/O0	8	7	PD1
I/O1	10	9	I/O8
I/O2	12	11	I/O9
I/O3	14	13	I/O10
VCC	16	15	I/O11
A7	18	17	A0
A8	20	19	A1
A9	22	21	A2
I/O4	24	23	I/O12
I/O5	26	25	I/O13
I/O6	28	27	I/O14
I/O7	30	29	I/O15
WE	32	31	GND
A14	34	33	A15
CS1	36	35	CS2
CS3	38	37	CS4
A16	40	39	NC
GND	42	41	OE
I/O16	44	43	I/O24
I/O17	46	45	I/O25
I/O18	48	47	I/O26
I/O19	50	49	I/O27
A10	52	51	A3
A11	54	53	A4
A12	56	55	A5
A13	58	57	VCC
I/O20	60	59	A6
I/O21	62	61	I/O28
I/O22	64	63	I/O29
I/O23	66	65	I/O30
GND	68	67	I/O31
NC	70	69	NC
NC	72	71	NC

PD0 - OPEN
PD1 - OPEN
PD2 - OPEN
PD3 - GND

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**SIMM
TOP VIEW**

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN(D)	Input Capacitance (Data and CS)	V(IN) = 0V	12	pF
CIN(A)	Input Capacitance (Address, WE, OE)	V(IN) = 0V	40	pF
COUT	Output Capacitance	V(OUT) = 0V	12	pF

NOTE: 3147 tbl 04
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	5.8	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE: 3147 tbl 05
1. VIL (min) = -3.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5.0V ± 10%

3147 tbl 06

TRUTH TABLE

Mode	CS	OE	WE	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DATAOUT	Active
Write	L	X	L	DATAIN	Active
Read	L	H	H	High-Z	Active

3147 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

NOTES: 3147 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$ I_{LI} $	Input Leakage (Data and \overline{CS})	$V_{CC} = \text{Max.}; V_{IN} = \text{GND to } V_{CC}$	—	10	μA
$ I_{LI} $	Input Leakage (Address, \overline{WE} , and \overline{OE})	$V_{CC} = \text{Max.}; V_{IN} = \text{GND to } V_{CC}$	—	40	μA
$ I_{LO} $	Output Leakage	$V_{CC} = \text{Max.}; \overline{CS} = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	—	10	μA
V_{OL}	Output Low	$V_{CC} = \text{Min.}, I_{OL} = 8\text{mA}$	—	0.4	V
V_{OH}	Output High	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	2.4	—	V

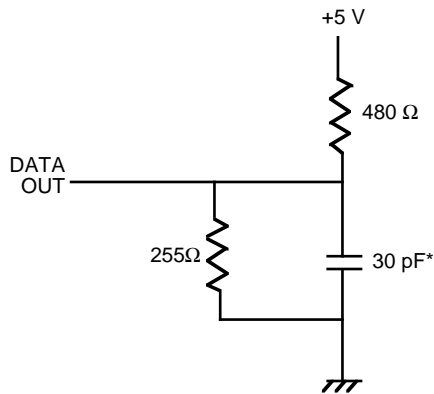
Symbol	Parameter	Test Conditions	Max.	Unit
I_{CC}	Dymanic Operating Current	$f = f_{MAX}; \overline{CS} = V_{IL}$ $V_{CC} = \text{Max.}; \text{Output Open}$	760	mA
I_{SB}	Standby Supply Current	$\overline{CS} \geq V_{IH}, V_{CC} = \text{Max.}$ Outputs Open, $f = f_{MAX}$	160	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC} - 0.2V; f = 0$ $V_{IN} > V_{CC} - 0.2V$ or $< 0.2V$	60	mA

3147 tbl 07

AC TEST CONDITIONS

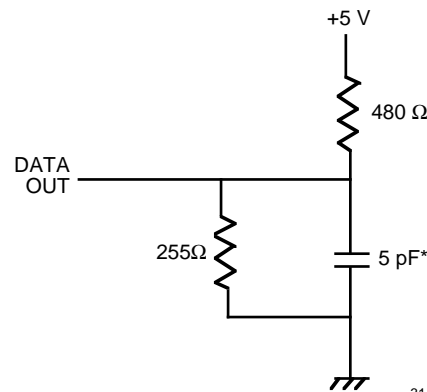
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

3147 tbl 08



* Includes scope and jig.

Figure 1. Output Load



3147 drw 03

Figure 2. Output Load
(for t_{OLZ} , t_{OHZ} , t_{CHZ} , t_{CLZ} ,
 t_{WHZ} , t_{OW})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

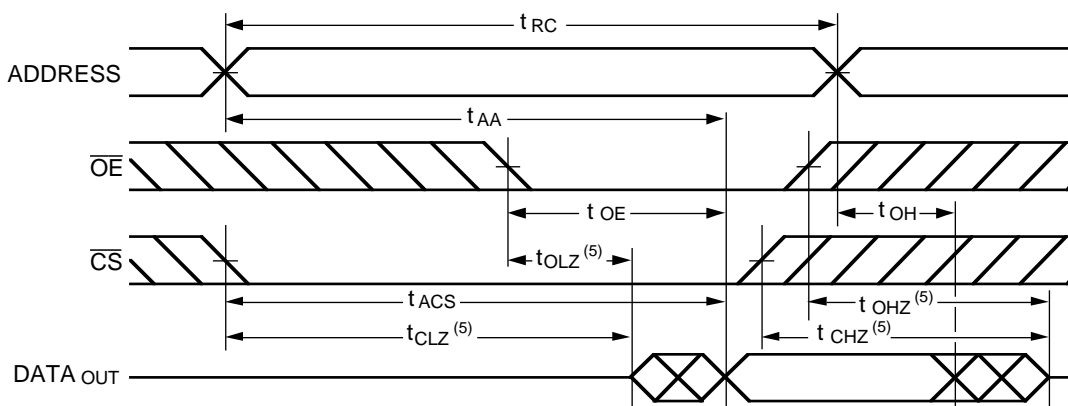
Symbol	Parameter	-15		-20		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	15	—	20	—	ns
t _{AA}	Address Access Time	—	15	—	20	ns
t _{ACS}	Chip Select Access Time	—	15	—	20	ns
t _{CLZ} ⁽¹⁾	Chip Select to Output in Low Z	3	—	3	—	ns
t _{OE}	Output Enable to Output Valid	—	8	—	10	ns
t _{OLZ} ⁽¹⁾	Output Enable to Output in Low Z	0	—	0	—	ns
t _{CHZ} ⁽¹⁾	Chip Deselect to Output in High Z	—	8	—	12	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output in High Z	—	8	—	12	ns
t _{OH}	Output Hold from Address Change	3	—	3	—	ns
t _{PU} ⁽¹⁾	Chip Select to Power-Up Time	0	—	0	—	ns
t _{PD} ⁽¹⁾	Chip Deselect to Power-Down Time	—	15	—	20	ns
Write Cycle						
t _{WC}	Write Cycle Time	15	—	20	—	ns
t _{CW}	Chip Select to End of Write	12	—	18	—	ns
t _{AW}	Address Valid to End of Write	12	—	18	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	ns
t _{WP}	Write Pulse Width	12	—	18	—	ns
t _{WR}	Write Recovery Time	0	—	3	—	ns
t _{WHZ} ⁽¹⁾	Write Enable to Output in High Z	—	8	—	13	ns
t _{DW}	Data to Write Time Overlap	10	—	12	—	ns
t _{DH}	Data Hold from Write Time	0	—	0	—	ns
t _{OW} ⁽¹⁾	Output Active from End of Write	3	—	3	—	ns

NOTE:

1. This parameter is guaranteed by design, but not tested.

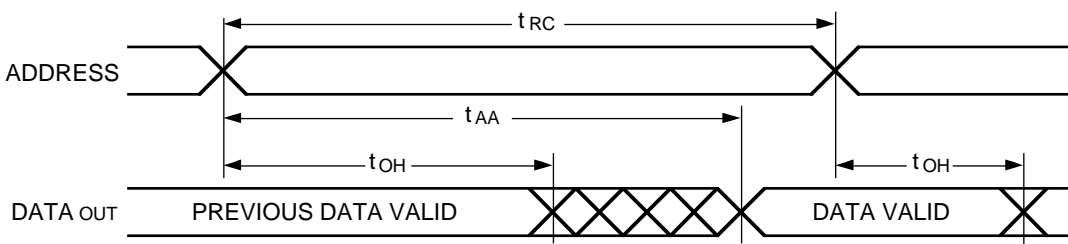
3147 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



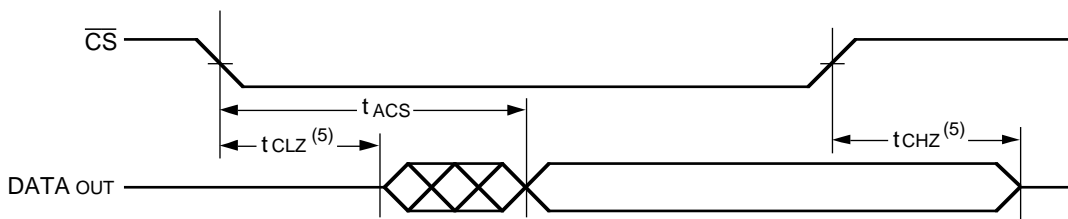
3147 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2^(1,2,4)



3147 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 3^(1,3,4)

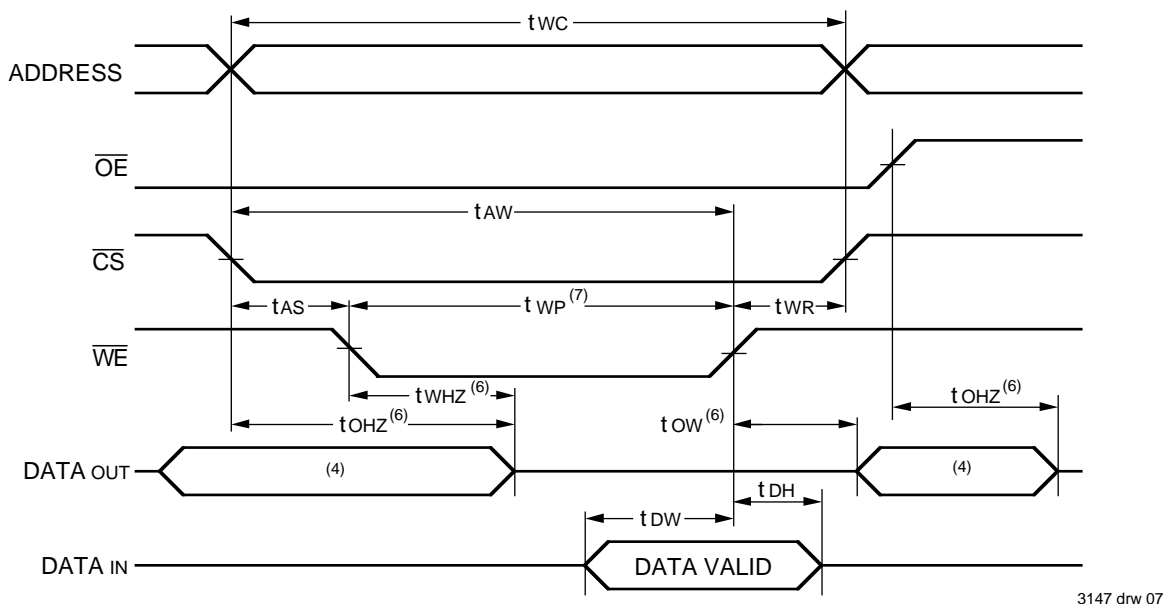


3147 drw 06

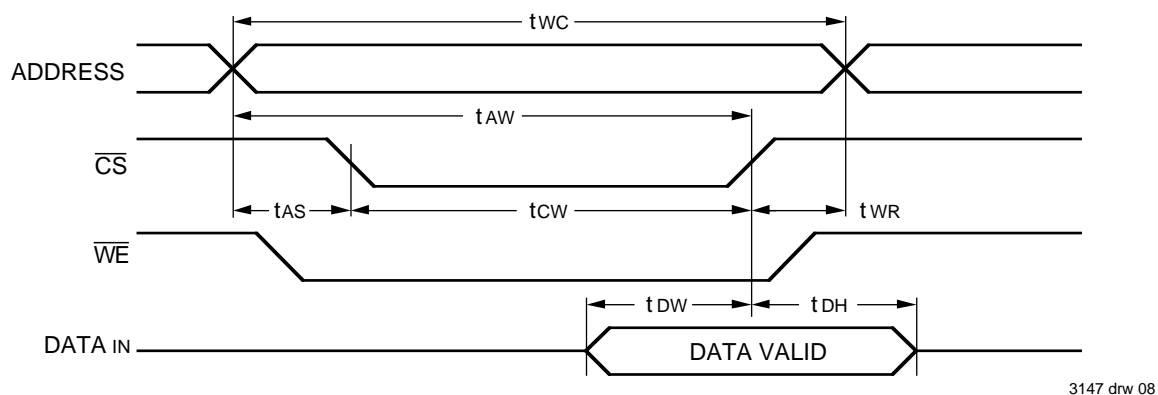
NOTES:

1. \overline{WE} is High for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with \overline{CS} transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 200mV$ from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED TIMING)^(1, 2, 3, 7)



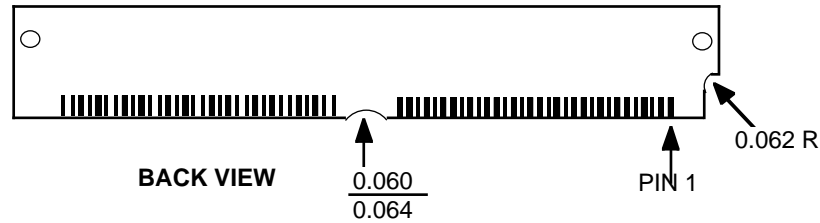
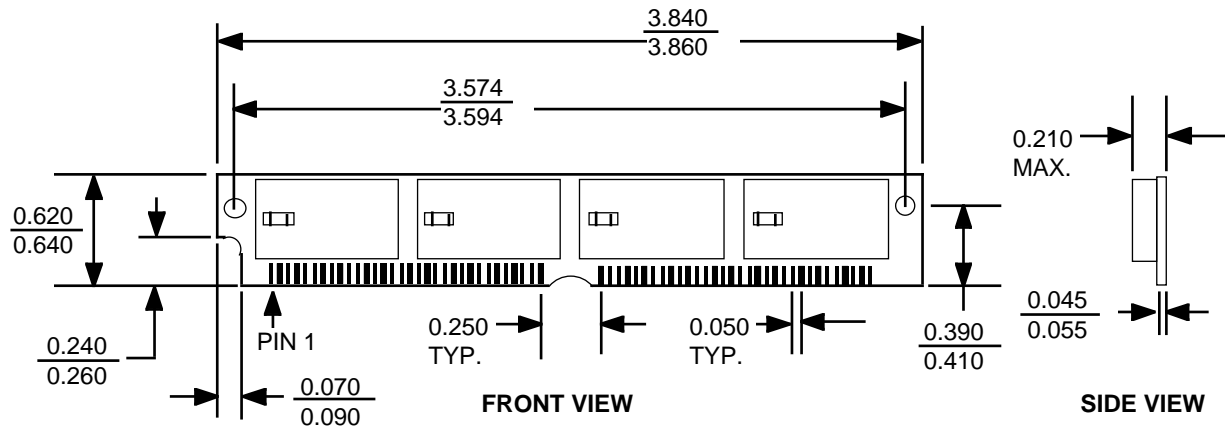
TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED TIMING)^(1, 2, 3, 5)



NOTES:

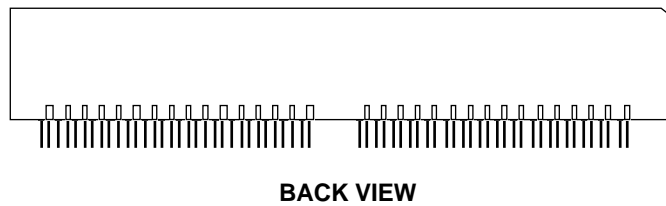
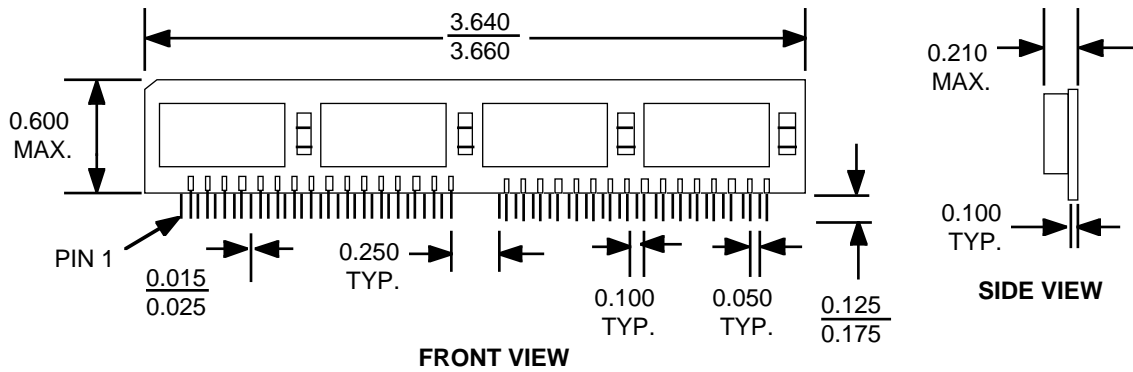
1. \overline{WE} or \overline{CS} must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CS} low transition occurs simultaneously with or after the \overline{WE} low transition, the outputs remain in a high impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If \overline{OE} is low during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$).

PACKAGE DIMENSIONS – IDT7MP4095
SIMM VERSION



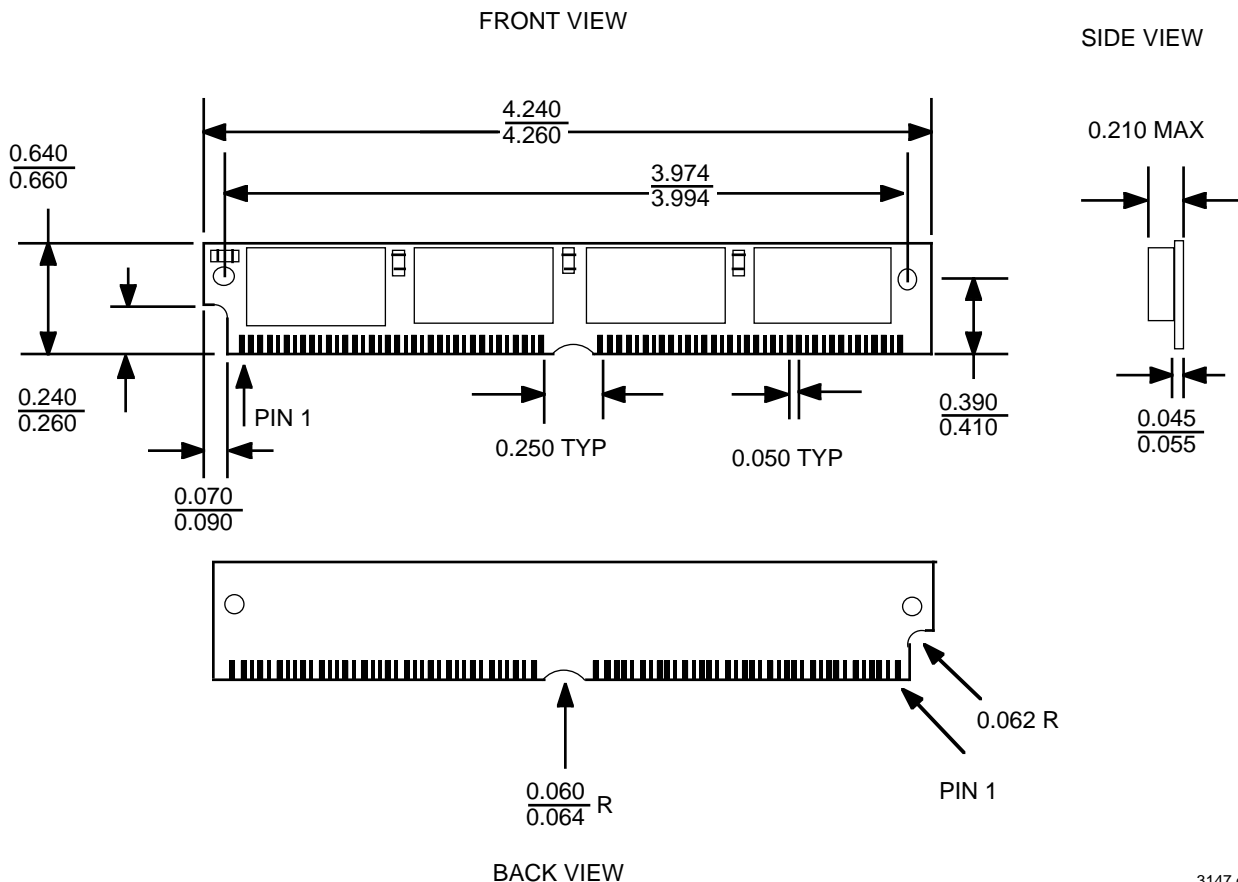
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ZIP VERSION



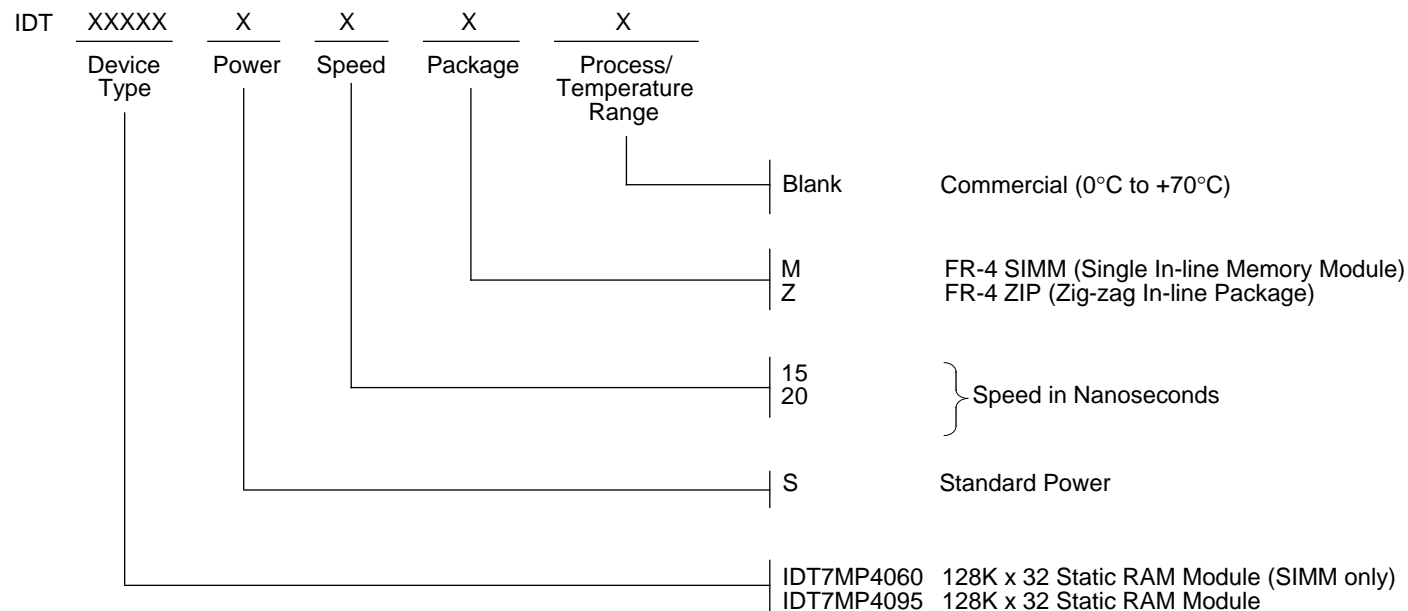
3147 drw 10

PACKAGE DIMENSIONS – IDT7MP4060



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ORDERING INFORMATION



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