

DESCRIPTION

The 7510 group is the 8-bit microcomputer based on the 740 family core technology.

This microcomputer is equipped with added functions such as a dot matrix type LCD controller/driver built in a contrast controller and UART.

FEATURES

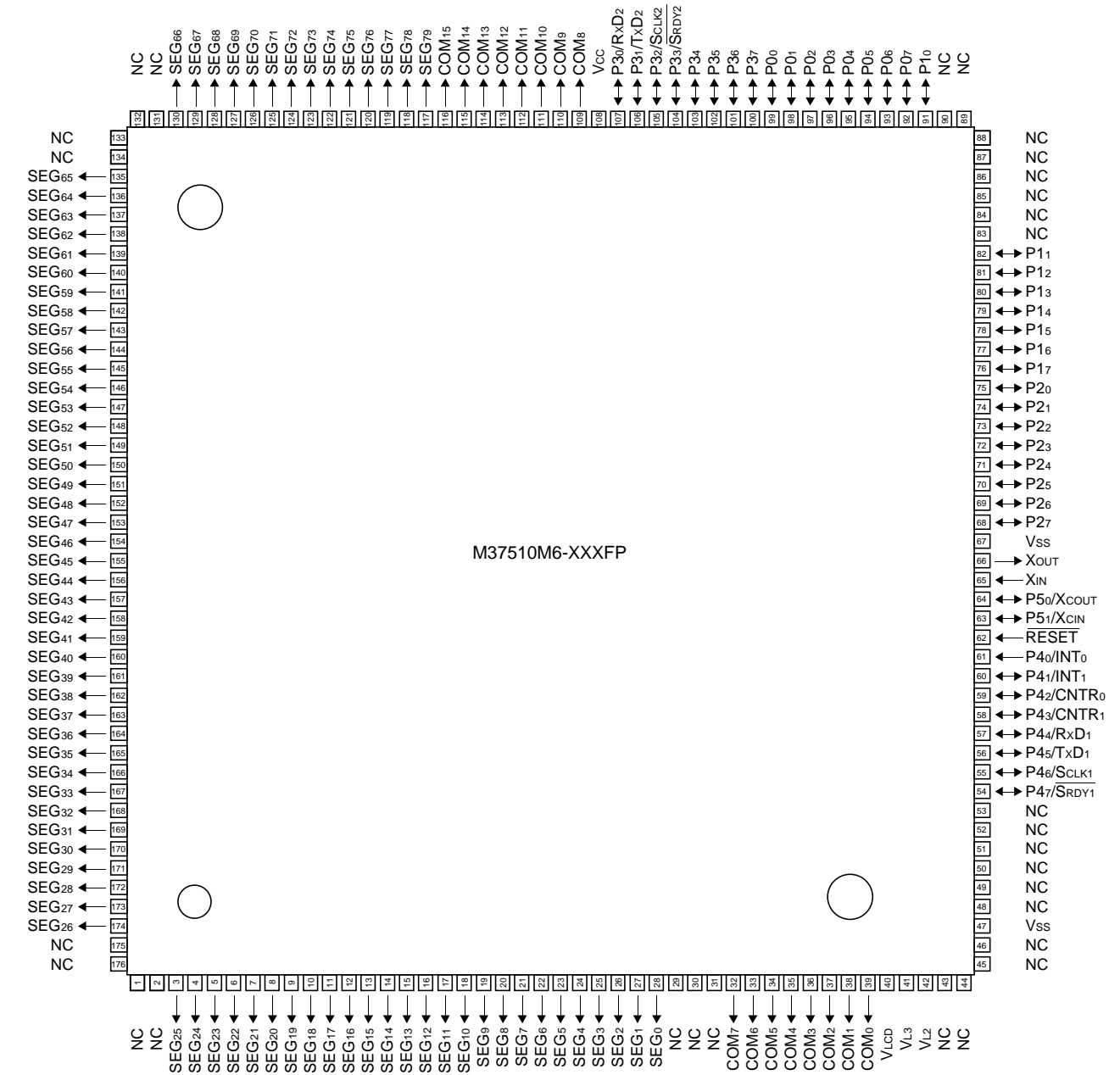
- Basic machine-language instructions 71
- The minimum instruction execution time 0.5 μ s
(at 8.0 MHz oscillation frequency)
- RAM for LCD display 160 bytes
- Programmable input/output ports 41
- Interrupts 15 sources, 15 vectors
(includes key-on wake up)
- Timers 8-bit X 3, 16-bit X 2
- Serial I/O 8-bit X 2 (UART or clock-synchronized)
- LCD controller/driver Bias 1/4, 1/5 bias
 - Duty ratio 1/8, 1/11, 1/16 duty
 - Common output 16
 - Segment output 80
 - Built-in an LCD contrast controller
(capable of 32-step contrast adjustment)

- 2 Clock generating circuit
(Connect to external ceramic resonator or quartz-crystal.)
- Power source voltage
 - In high-speed mode 4.0 to 5.5 V
 - In middle-speed mode 2.5 to 5.5 V
 - In low-speed mode 2.5 to 5.5 V
- Power dissipation
 - In high-speed mode 32 mW
(at 8.0 MHz oscillation frequency)
 - In low-speed mode 60 μ W
(at 32 kHz oscillation frequency and 3.0 V power source voltage)
 - In wait mode 9 μ W
(at 32 kHz oscillation frequency and 3.0 V power source voltage)
- Operating temperature range -20 to +85°C

APPLICATION

Cellular radio telephones, business telephones, facsimiles, and other portable equipment that need a large capacity of LCD display.

PIN CONFIGURATION (TOP VIEW)

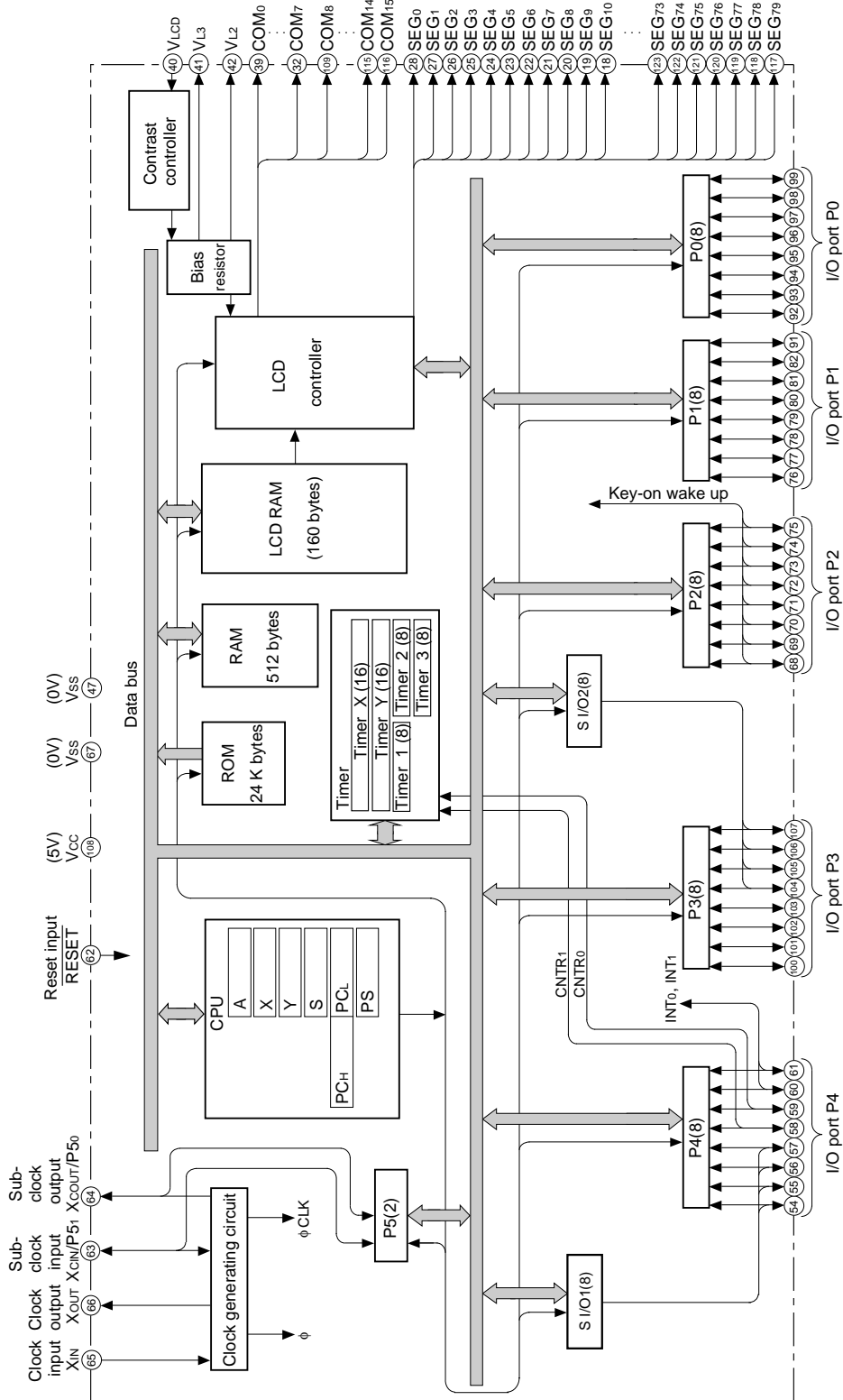


M37510M6-XXXXP

Package type : 176P6D-A
176-pin plastic-molded QFP

NC : No connect

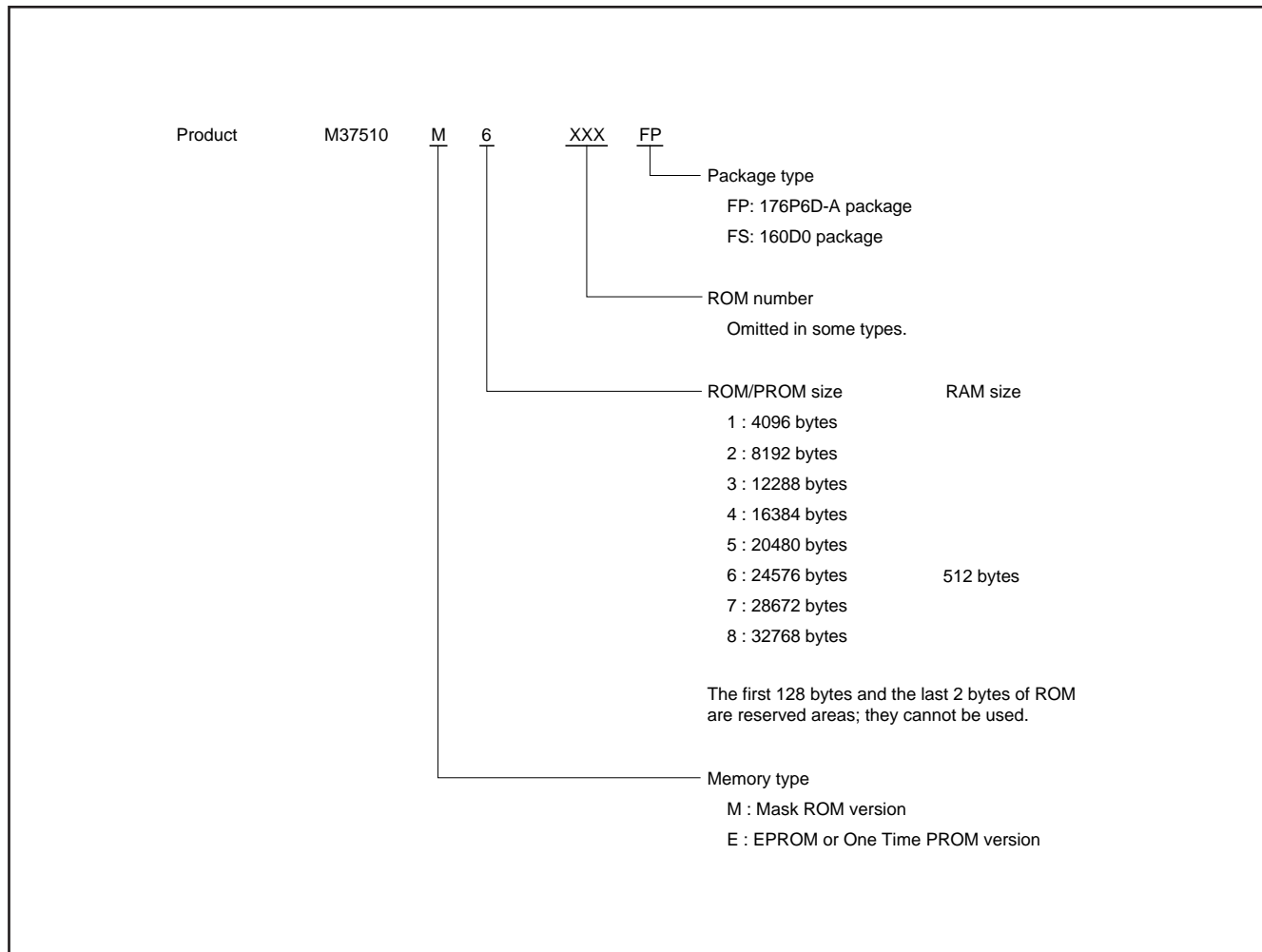
M37510M6-XXXXFP BLOCK DIAGRAM



PIN DESCRIPTION

| Pin | Name | Function | Function except a port function |
|----------------------------------------------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|
| | | | |
| VCC, VSS | Power source | Apply voltage of 4.0 to 5.5 V to VCC, and 0 V to VSS (in high-speed mode). | |
| $\overline{\text{RESET}}$ | Reset input | Reset input pin for active "L". | |
| XIN | Clock input | Input and output pins for the main clock generating circuit. Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillating frequency. If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. | |
| XOUT | Clock output | | |
| VLCD | LCD voltage source | This pin is used as voltage supply input for LCD driver. Input $V_{\text{LCD}} \leq V_{\text{CC}}$ voltage. | |
| VL2, VL3 | LCD bias control pin | When the LCD is operated at 1/5 bias, leave these pins open. When the LCD is operated at 1/4 bias, connect these pins externally. | |
| COM0–COM15 | Common output | LCD common output pins. | |
| SEG0–SEG79 | Segment output | LCD segment output pins. | |
| P00–P07 | I/O port P0 | An 8-bit I/O port. The output structure of this port is CMOS 3-state, and the input levels are CMOS compatible. The port direction register allows each pin to be individually programmed as either input or output. | |
| P10–P17 | I/O port P1 | | |
| P20–P27 | I/O port P2 | | |
| P30/RXD2, P31/TXD2, P32/ SCLK2, P33/SRDY2 | I/O port P3 | Key input (Key-on wake-up) interrupt input pins. | |
| P34–P37 | | Serial I/O2 function pins | |
| P40/INT0 | Input port P4 | A 1-bit CMOS level input port. | External interrupt input pins |
| P41/INT1 | I/O port P4 | A 7-bit I/O port with the same function as port P0. The port direction register allows each pin to be individually programmed as either input or output. | |
| P42/CNTR0, P43/CNTR1 | | | Timer X, Timer Y function pins External interrupt input pins |
| P44/RXD1, P45/TXD1, P46/ SCLK1, P47/SRDY1 | | | Serial I/O1 function pins |
| P50/XCOUT, P51/XCIN | I/O port P5 | A 2-bit I/O port with the same function as port P0. The port direction register allows each pin to be individually programmed as either input or output. | I/O pins for the internal sub clock generating circuit. Connect an oscillator. |

PART NUMBERING



Currently supported products are listed below.

As of May 1996

| Product name | (P) ROM size (bytes) | RAM size (bytes) | Package | Remarks |
|----------------|----------------------|------------------|----------|-------------------------------|
| M37510M6-XXXFP | 24K | 512 | 176P6D-A | Mask ROM version |
| M37510E6-XXXFP | | | | One Time PROM version |
| M37510E6FP | | | | One Time PROM version (blank) |
| M37510E6FS | | | 160D0 | EPROM version |

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 7510 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

- The FST and SLW instruction are not available for use.
- The STP, WIT, MUL, and DIV instruction can be used.

CPU MODE REGISTER

The CPU mode register is allocated at address 003B₁₆.

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

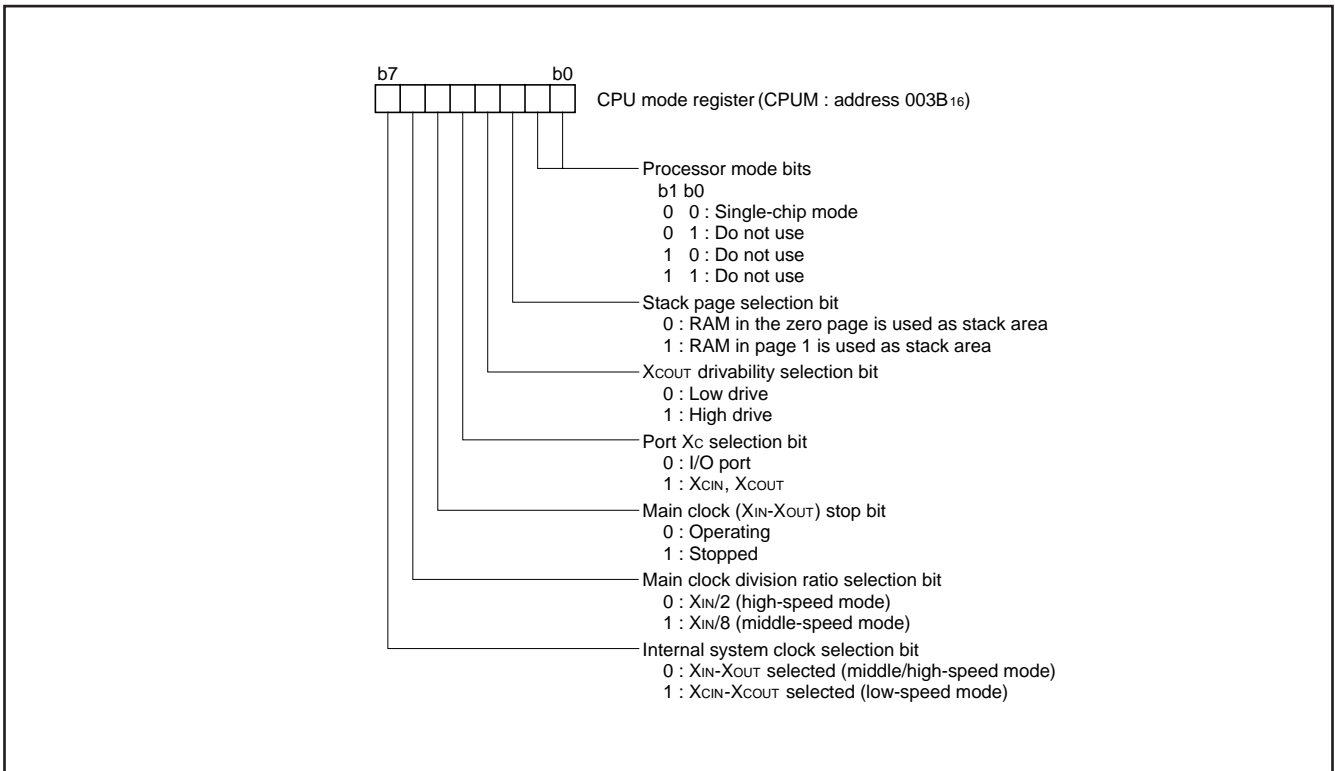


Fig. 1 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.

RAM

RAM is used for data storage as well for stack area.

ROM

The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

This dedicated zero page addressing mode enables access to this area with only 2 bytes.

Special Page

This dedicated special page addressing mode enables access to this area with only 2 bytes.

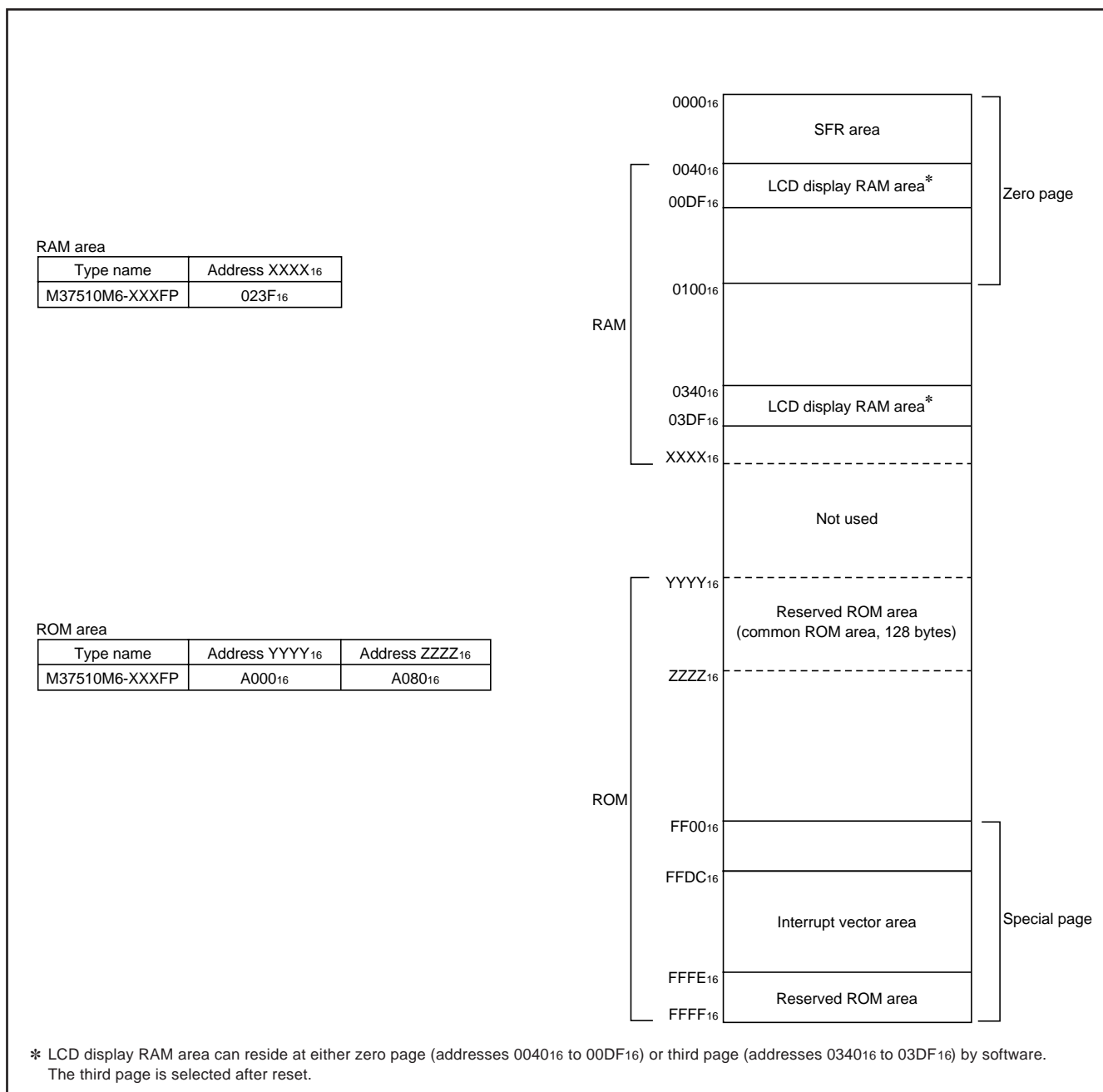


Fig. 2 Memory map diagram

| | | | |
|--------------------|----------------------------------------------|--------------------|----------------------------------------------|
| 0000 ₁₆ | Port P0 (P0) | 0020 ₁₆ | Timer X (low) (TXL) |
| 0001 ₁₆ | Port P0 direction register (P0D) | 0021 ₁₆ | Timer X (high) (TXH) |
| 0002 ₁₆ | Port P1 (P1) | 0022 ₁₆ | Timer Y (low) (TYL) |
| 0003 ₁₆ | Port P1 direction register (P1D) | 0023 ₁₆ | Timer Y (high) (TYH) |
| 0004 ₁₆ | Port P2 (P2) | 0024 ₁₆ | Timer 1 (T1) |
| 0005 ₁₆ | Port P2 direction register (P2D) | 0025 ₁₆ | Timer 2 (T2) |
| 0006 ₁₆ | Port P3 (P3) | 0026 ₁₆ | Timer 3 (T3) |
| 0007 ₁₆ | Port P3 direction register (P3D) | 0027 ₁₆ | Timer X mode register (TXM) |
| 0008 ₁₆ | Port P4 (P4) | 0028 ₁₆ | Timer Y mode register (TYM) |
| 0009 ₁₆ | Port P4 direction register (P4D) | 0029 ₁₆ | Timer 123 mode register (T123M) |
| 000A ₁₆ | Port P5 (P5) | 002A ₁₆ | |
| 000B ₁₆ | Port P5 direction register (P5D) | 002B ₁₆ | |
| 000C ₁₆ | Port P0 pull-up control register (PULLP0) | 002C ₁₆ | |
| 000D ₁₆ | Port P1 pull-up control register (PULLP1) | 002D ₁₆ | |
| 000E ₁₆ | Port P2 pull-up control register (PULLP2) | 002E ₁₆ | |
| 000F ₁₆ | Port P3 pull-up control register (PULLP3) | 002F ₁₆ | |
| 0010 ₁₆ | Port P4 pull-up control register (PULLP4) | 0030 ₁₆ | Transmit/receive buffer register 2 (TB2/RB2) |
| 0011 ₁₆ | Port P5 pull-up control register (PULLP5) | 0031 ₁₆ | Serial I/O2 status register (SIO2STS) |
| 0012 ₁₆ | | 0032 ₁₆ | Serial I/O2 control register (SIO2CON) |
| 0013 ₁₆ | | 0033 ₁₆ | UART2 control register (UART2CON) |
| 0014 ₁₆ | | 0034 ₁₆ | Baud rate generator 2 (BRG2) |
| 0015 ₁₆ | | 0035 ₁₆ | |
| 0016 ₁₆ | | 0036 ₁₆ | |
| 0017 ₁₆ | | 0037 ₁₆ | LCD contrast control register (LC) |
| 0018 ₁₆ | Transmit/receive buffer register 1 (TB1/RB1) | 0038 ₁₆ | |
| 0019 ₁₆ | Serial I/O1 status register (SIO1STS) | 0039 ₁₆ | LCD mode register (LM) |
| 001A ₁₆ | Serial I/O1 control register (SIO1CON) | 003A ₁₆ | Interrupt edge selection register (INTEDGE) |
| 001B ₁₆ | UART1 control register (UART1CON) | 003B ₁₆ | CPU mode register (CPUM) |
| 001C ₁₆ | Baud rate generator 1 (BRG1) | 003C ₁₆ | Interrupt request register 1 (IREQ1) |
| 001D ₁₆ | | 003D ₁₆ | Interrupt request register 2 (IREQ2) |
| 001E ₁₆ | | 003E ₁₆ | Interrupt control register 1 (ICON1) |
| 001F ₁₆ | | 003F ₁₆ | Interrupt control register 2 (ICON2) |

Fig. 3 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The 7510 group has 41 programmable I/O pins arranged in six I/O ports (ports P0 to P5). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating and can read the value of the pin itself. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Port Pull-up Control Registers

The 7510 group is equipped with internal pull-ups that can be enabled by software. Each I/O port of ports P0–P5 has an port Pi (i= 0 to 5) pull-up control register (addresses 000C16 to 001116). Each bit of the pull-up control register controls a corresponding bit of the port. The value written to each individual bit determines whether the pull-up of the corresponding pin is either enabled or disabled.

When "0" is written to the pull-up control register, the pull up on the pin is disabled. When "1" is written to the pull-up control register, the pull-up on the pin is enabled.

After reset, all the pull-up control registers are initialized to "0016", disabling all the internal pull-ups.

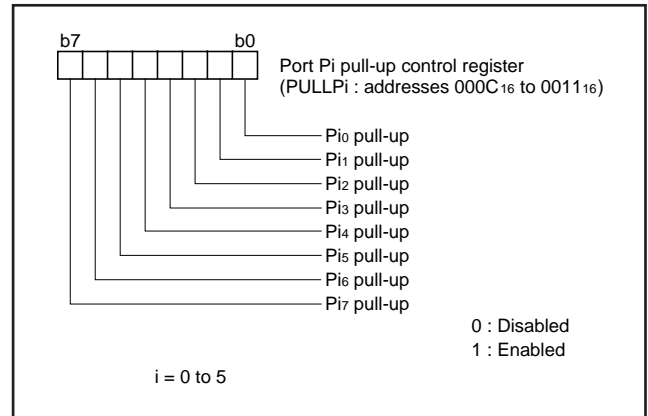


Fig. 4 Structure of port Pi pull-up control register

| Pin | Name | Input/Output | I/O Format | Non-Port Function | Related SFRs | Ref. No. | |
|---------------------------------------------------------------|---------|-------------------------------|----------------------------------------------------|----------------------------------------------|------------------------------|------------------------------|-----|
| P00–P07 | Port P0 | Input/output, individual bits | CMOS compatible input level CMOS 3-state output | | | (1) | |
| P10–P17 | Port P1 | Input/output, individual bits | CMOS compatible input level CMOS 3-state output | | | (1) | |
| P20–P27 | Port P2 | Input/output, individual bits | CMOS compatible input level CMOS 3-state output | Key-on wake up interrupt input | Interrupt control register 2 | (2) | |
| P30/RXD2, P31/TXD2, P32/ SCLK2, P33/SRDY2 P34–P37 | Port P3 | Input/output, individual bits | CMOS compatible input level CMOS 3-state output | Serial I/O2 function I/O | Serial I/O2 control register | (3) | |
| | | | | | Serial I/O2 status register | (4) | |
| | | | | | UART control register 2 | (5) | |
| | | | | | | (6) | |
| P40/INT0 | Port P4 | Input | CMOS compatible input level | External interrupt input | | (7) | |
| P41/INT1 | | | | | | (8) | |
| P42/CNTR0, P43/CNTR1 | | Input/output, individual bits | CMOS compatible input level CMOS 3-state output | Timer X function I/O Timer Y function I/O | Timer X mode register | (9) | |
| P44/RXD1, P45/TXD1, P46/ SCLK1, P47/SRDY1 | | | | | Serial I/O1 function I/O | Serial I/O1 control register | (3) |
| | | | | | | Serial I/O1 status register | (4) |
| | | | | | | UART1 control register | (5) |
| | | | | UART1 control register | (6) | | |
| P50/XCOUT, P51/XCIN | Port P5 | Input/output, individual bits | CMOS compatible input level CMOS 3-state output | Sub-clock generating circuit I/O | CPU mode register | (1) | |
| COM0–COM15 | Common | Output | LCD common output | | LCD mode register | | |
| SEG0–SEG79 | Segment | Output | LCD segment output | | | | |

Notes 1: For details of how to use double-function ports as function I/O ports, refer to the applicable sections.

2: Make sure that the input level at each pin is either 0 V or Vcc during execution of the STP instruction.

When an input level is at an intermediate potential, a current will flow from Vcc to Vss through the input-stage gate.

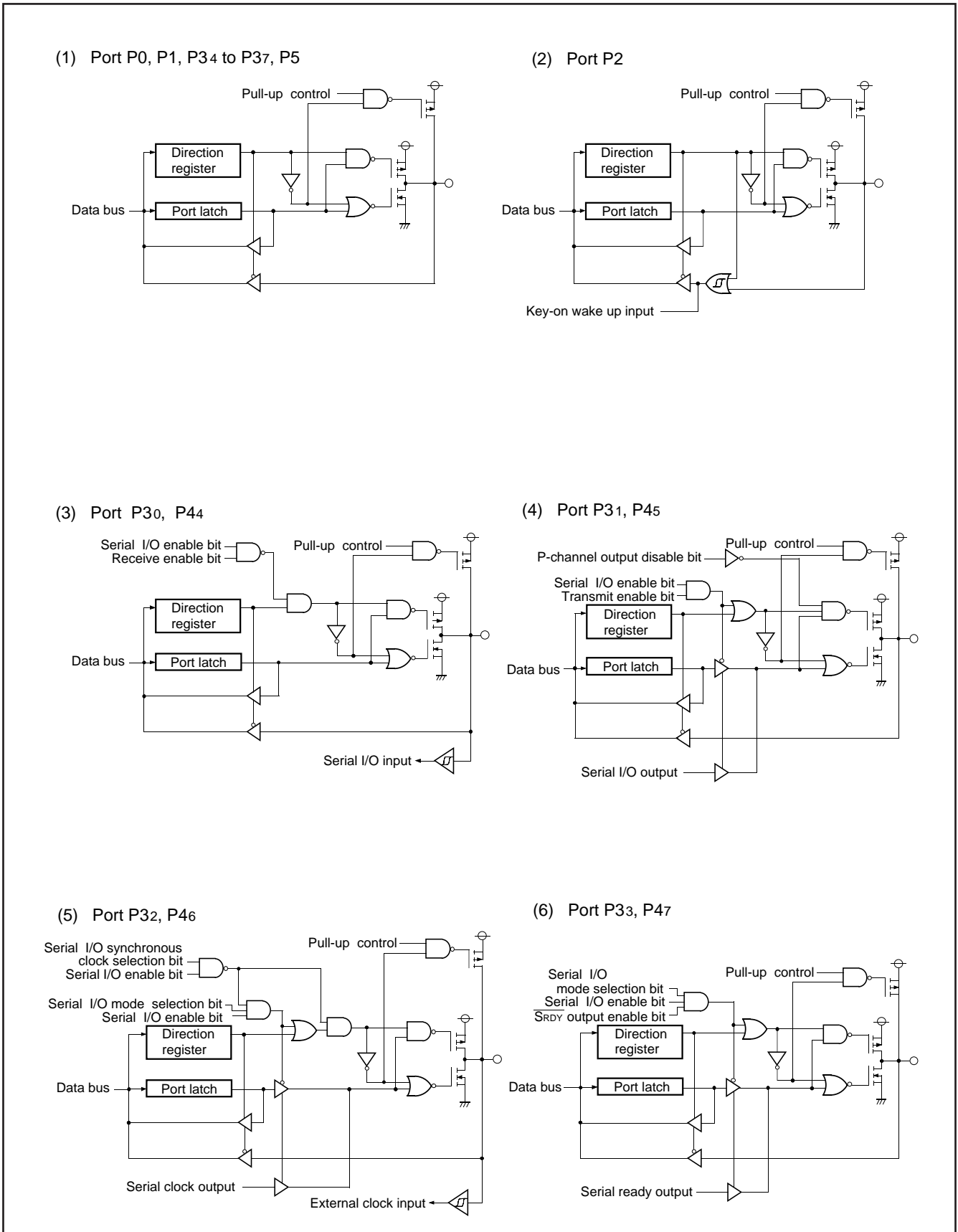


Fig. 5 Port block diagram (1)

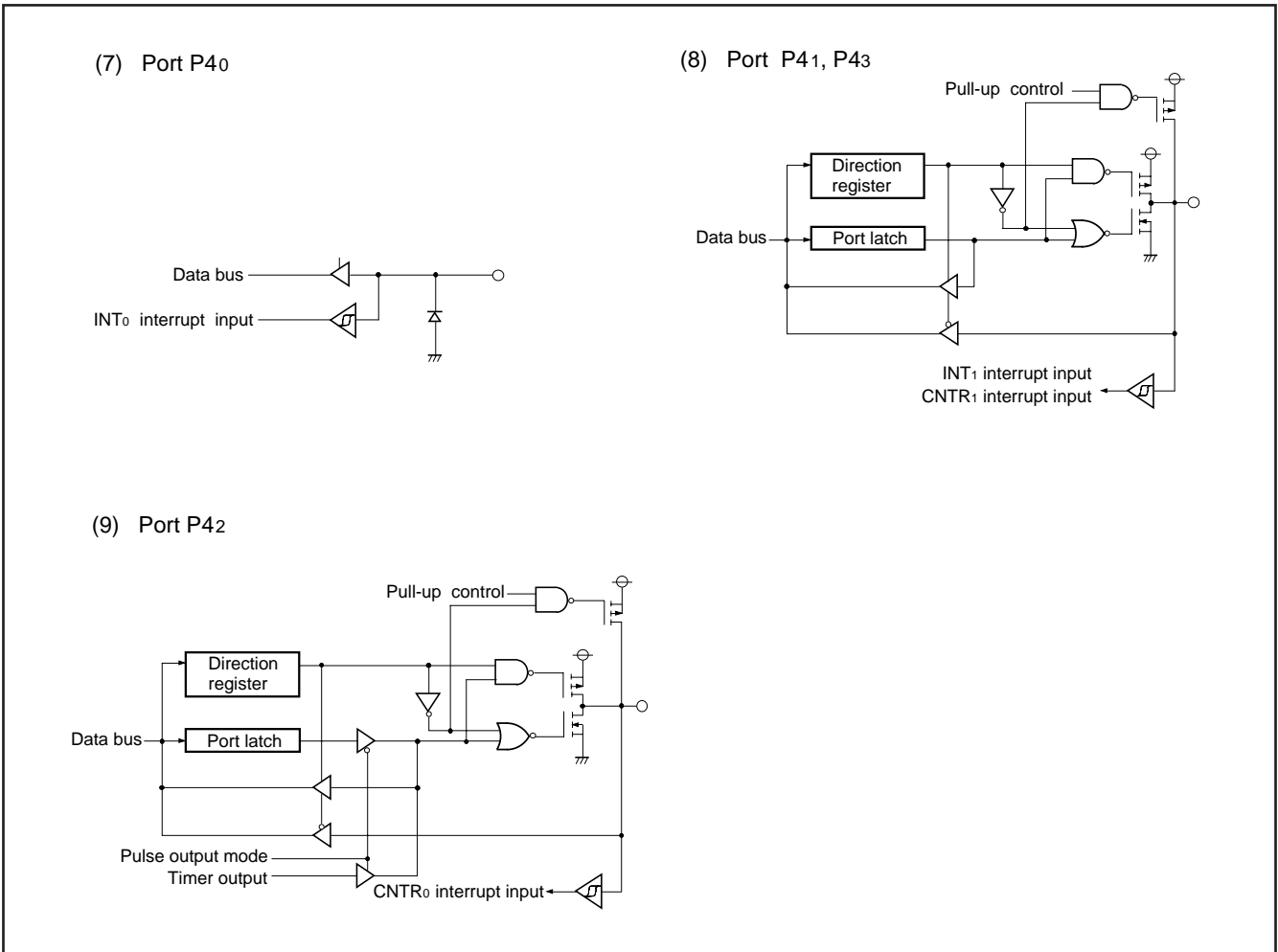


Fig. 6 Port block diagram (2)

INTERRUPTS

A total of 15 sources can generate interrupts: 5 external, 9 internal, and 1 software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The reset and BRK instruction can not be disabled with any flag or bit.

The I flag disables all interrupts except for the BRK instruction interrupt and the reset.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

Notes on Use

When the active edge of an external interrupt (INT₀, INT₁, CNTR₀, or CNTR₁) is changed, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;

- (1) Disable the external interrupt which is selected.
- (2) Change the active edge selection.
- (3) Clear interrupt request which is selected to "0".
- (4) Enable the external interrupt which is selected.

Table 1 Interrupt vector addresses and priority

| Interrupt source | Priority | Vector addresses (Note 1) | | Interrupt request generating conditions | Remarks |
|--------------------------|----------|---------------------------|--------------------|---------------------------------------------------------------------------|---------------------------------------------------------|
| | | High | Low | | |
| Reset (Note 2) | 1 | FFFD ₁₆ | FFFC ₁₆ | At reset | Non-maskable |
| INT ₀ | 2 | FFFB ₁₆ | FFFA ₁₆ | At detection of either rising or falling edge of INT ₀ input | External interrupt (active edge selectable) |
| INT ₁ | 3 | FFF9 ₁₆ | FFF8 ₁₆ | At detection of either rising or falling edge of INT ₁ input | External interrupt (active edge selectable) |
| Serial I/O1 reception | 4 | FFF7 ₁₆ | FFF6 ₁₆ | At end of serial I/O1 data reception | Valid when serial I/O1 is selected |
| Serial I/O1 transmission | 5 | FFF5 ₁₆ | FFF4 ₁₆ | At end of serial I/O1 transfer shift or when transmission buffer is empty | Valid when serial I/O1 is selected |
| Timer X | 6 | FFF3 ₁₆ | FFF2 ₁₆ | At timer X underflow | |
| Timer Y | 7 | FFF1 ₁₆ | FFF0 ₁₆ | At timer Y underflow | |
| Timer 2 | 8 | FFEF ₁₆ | FFEE ₁₆ | At timer 2 underflow | |
| Timer 3 | 9 | FFED ₁₆ | FFEC ₁₆ | At timer 3 underflow | |
| Serial I/O2 reception | 10 | FFEB ₁₆ | FFEA ₁₆ | At end of serial I/O2 data reception | Valid when serial I/O2 is selected |
| Serial I/O2 transmission | 11 | FFE9 ₁₆ | FFE8 ₁₆ | At end of serial I/O2 transfer shift or when transmission buffer is empty | Valid when serial I/O2 is selected |
| CNTR ₀ | 12 | FFE7 ₁₆ | FFE6 ₁₆ | At detection of either rising or falling edge of CNTR ₀ input | External interrupt (active edge selectable) |
| CNTR ₁ | 13 | FFE5 ₁₆ | FFE4 ₁₆ | At detection of either rising or falling edge of CNTR ₁ input | External interrupt (active edge selectable) |
| Timer 1 | 14 | FFE3 ₁₆ | FFE2 ₁₆ | At timer 1 underflow | |
| Key-on wake up | 15 | FFE1 ₁₆ | FFE0 ₁₆ | At falling of conjunction of input logic level for port P2 (at input) | External interrupt (valid when an "L" level is applied) |
| BRK instruction | 16 | FFDD ₁₆ | FFDC ₁₆ | At BRK instruction execution | Non-maskable software interrupt |

Notes 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

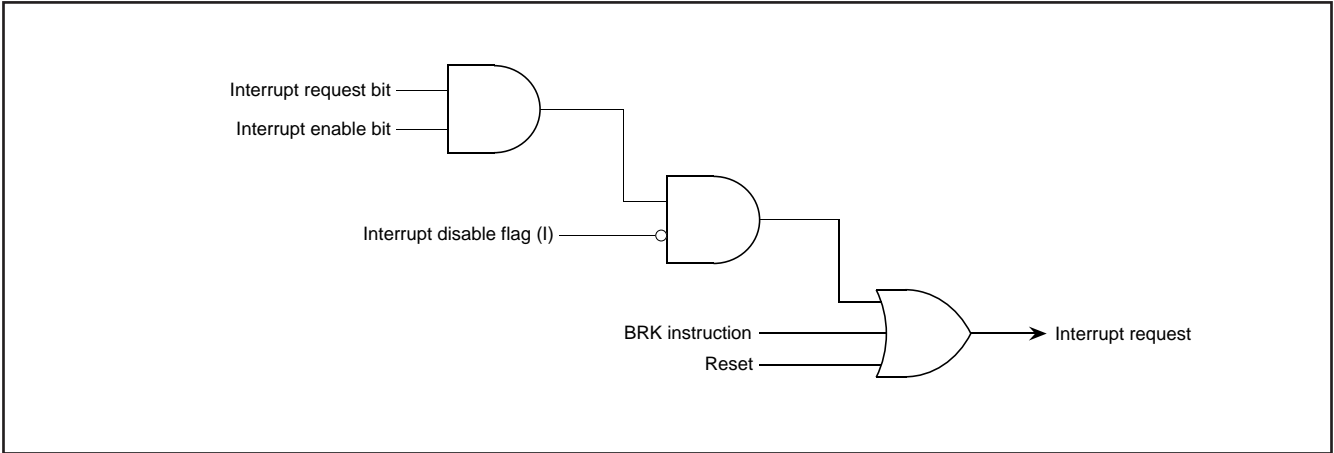


Fig. 7 Interrupt control

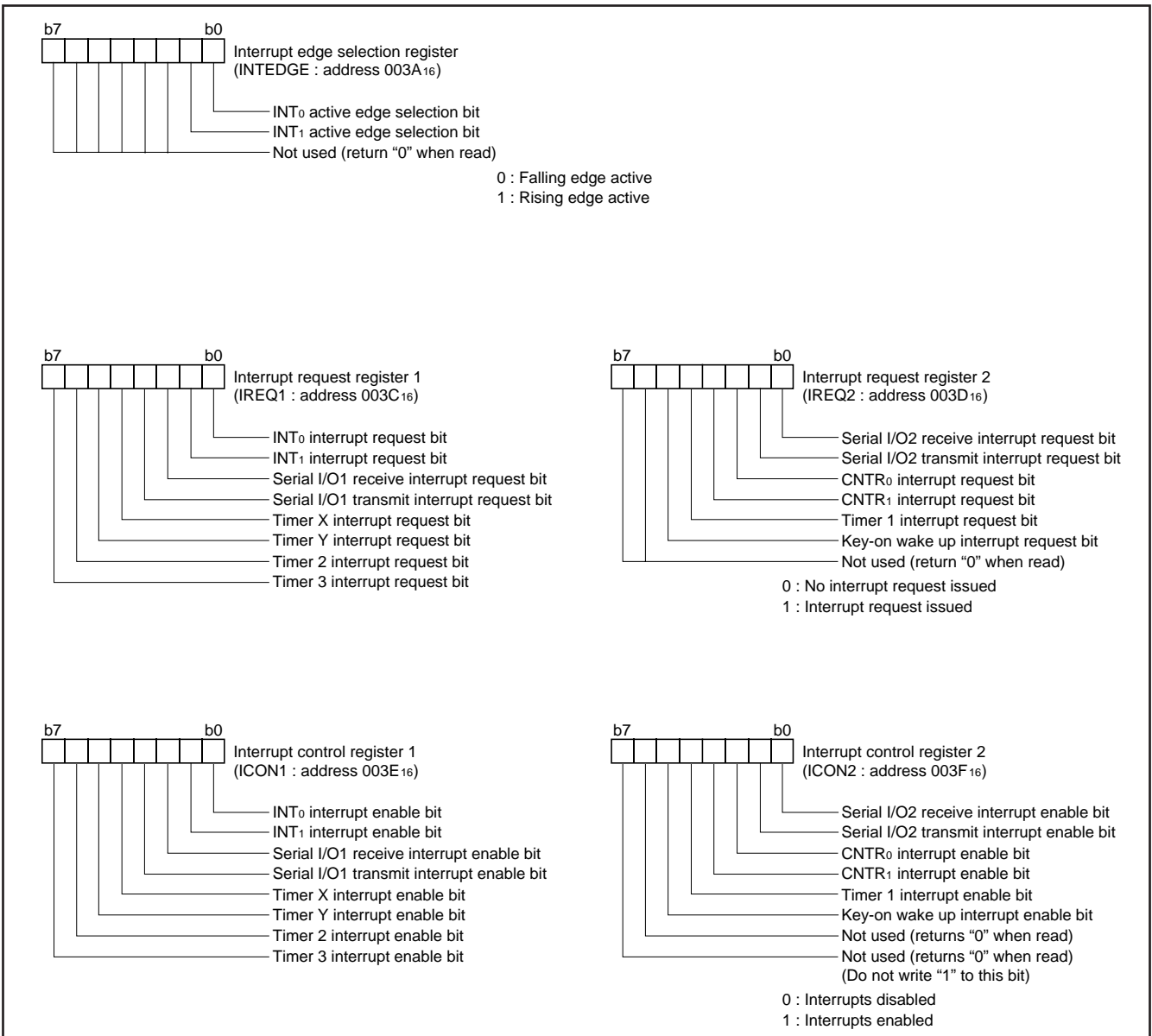


Fig. 8 Structure of interrupt-related registers

TIMERS

The 7510 group has five built-in timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, whereas timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "0016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit cor-

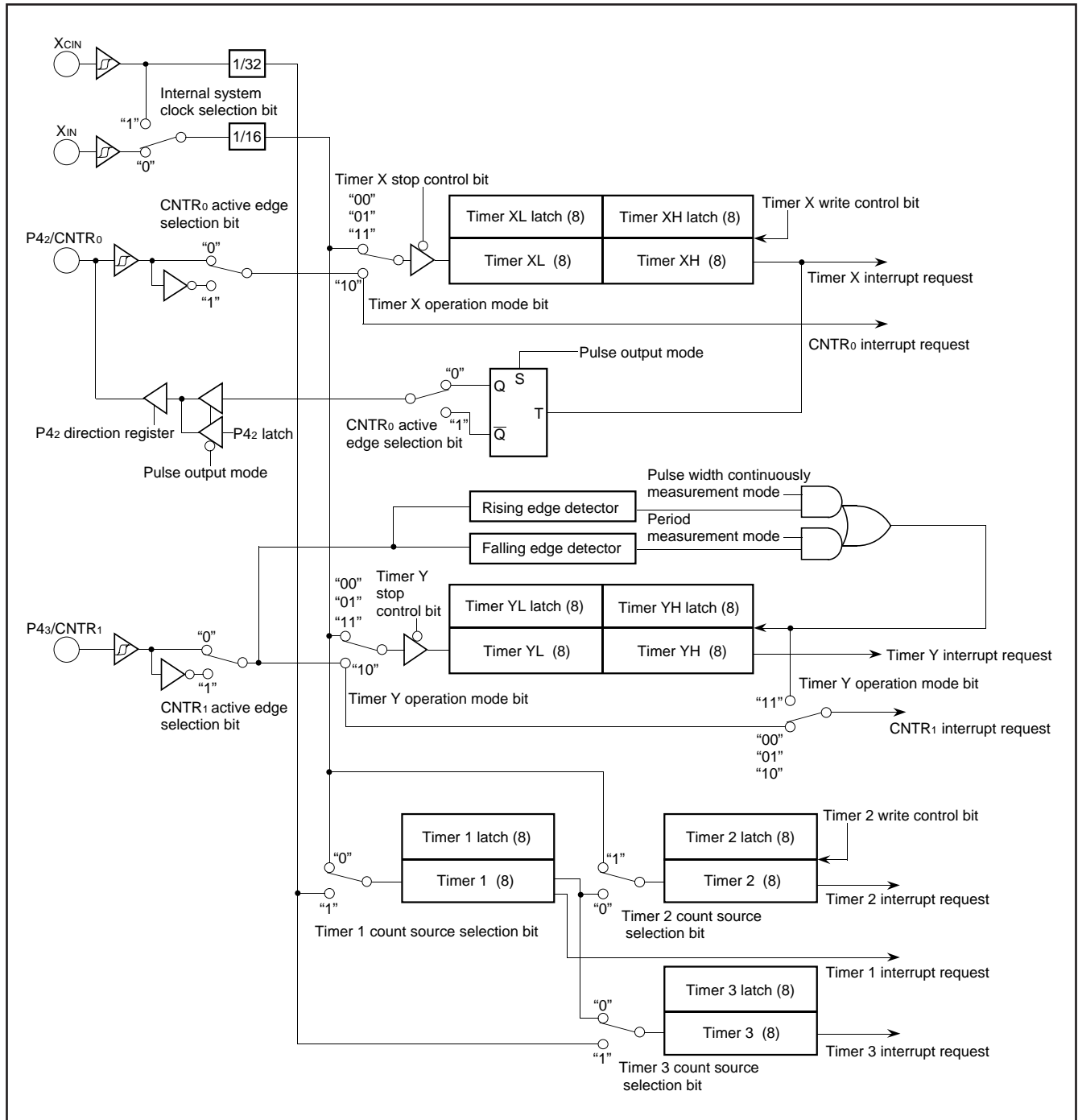


Fig. 9 Block diagram of Timer

responding to that timer is set to "1".

Read and write operation on 16-bit timer must be performed for both high and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write by setting the timer X mode register.

Timer mode

The timer counts $f(XIN)/16$ (or $f(XCIN)/16$, if the selected system clock ϕ is $f(XCIN)/2$).

Pulse output mode

Each time the timer underflows, a signal output from the CNTR0 pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P42 direction register to output mode.

Event counter mode

The timer counts signals input through the CNTR0 pin. Except for this, the operation in event counter mode is the same as in timer mode.

Pulse width measurement mode

The count source is $f(XIN)/16$ (or $f(XCIN)/16$, if the selected system clock ϕ is $f(XCIN)/2$). If CNTR0 active edge selection bit is "0", the timer counts while the input signal of CNTR0 pin is at "H". If it is "1", the timer counts while the input signal of CNTR0 pin is at "L".

Timer X Write Control

If the timer X write control bit is "0", when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.

If the timer X write control bit is "1", when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.

If the value is written in latch only, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

Note on CNTR0 Interrupt Active Edge Selection

CNTR0 interrupt active edge depends on the CNTR0 active edge selection bit.

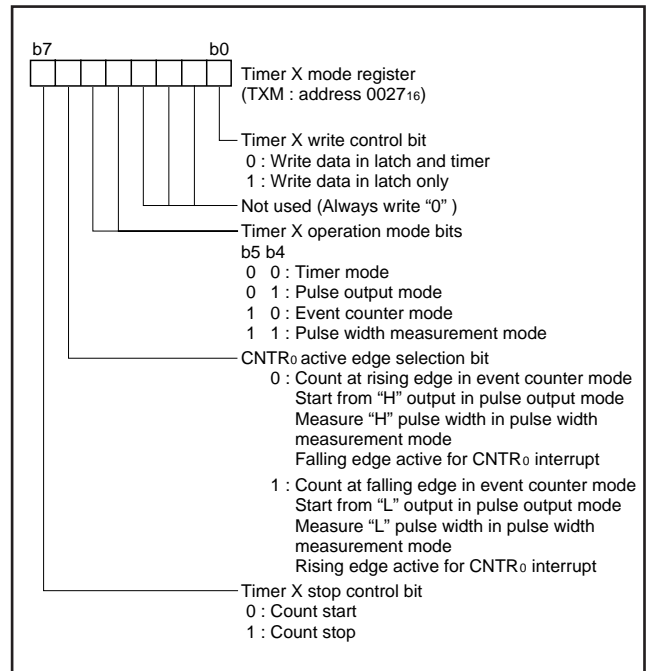


Fig. 10 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

Timer mode

The timer counts $f(XIN)/16$ (or $f(XCIN)/16$, if the selected system clock ϕ is $f(XCIN)/2$).

Period measurement mode

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR1 pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR1 pin input signal is found by CNTR1 interrupt.

Event counter mode

The timer counts signals input through the CNTR1 pin. Except for this, the operation in event counter mode is the same as in timer mode.

Pulse width HL continuously measurement mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode.

Note on CNTR1 Interrupt Active Edge Selection

CNTR1 interrupt active edge depends on the CNTR1 active edge selection bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge selection bit.

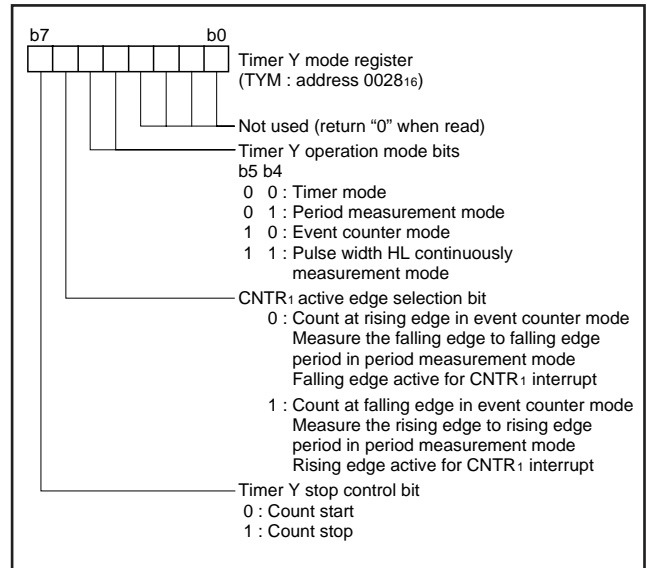


Fig. 11 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer.

Therefore, rewrite the value of timer whenever the count source is changed.

Timer 2 Write Control

If the timer 2 write control bit is "0", when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is "1", when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

Note on Timer 1 to Timer 3

When the count source of timer 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer. If the count source of timer 2 or timer 3 is connected to timer 1 output, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

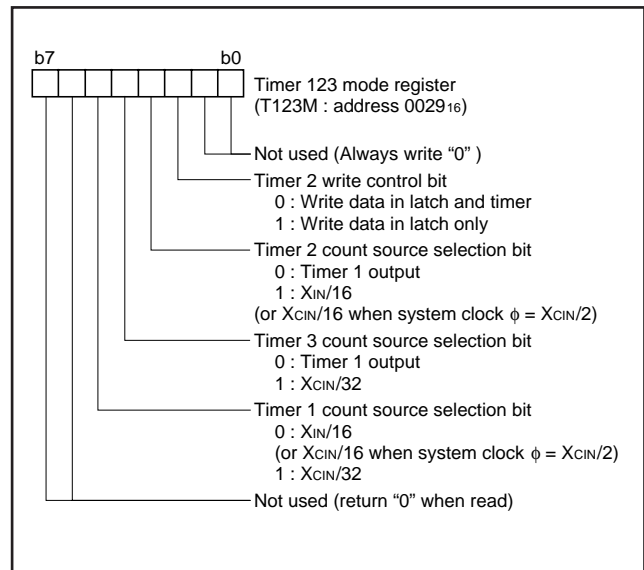


Fig. 12 Structure of timer 123 mode register

SERIAL I/O

The 7510 group has two built-in serial I/O channels (serial I/O1 and serial I/O2). Both serial I/O ports are functionally identical. Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the mode selection bit of the serial I/O control register (addresses 001A₁₆ and 0032₁₆) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB (addresses 0018₁₆ and 0030₁₆).

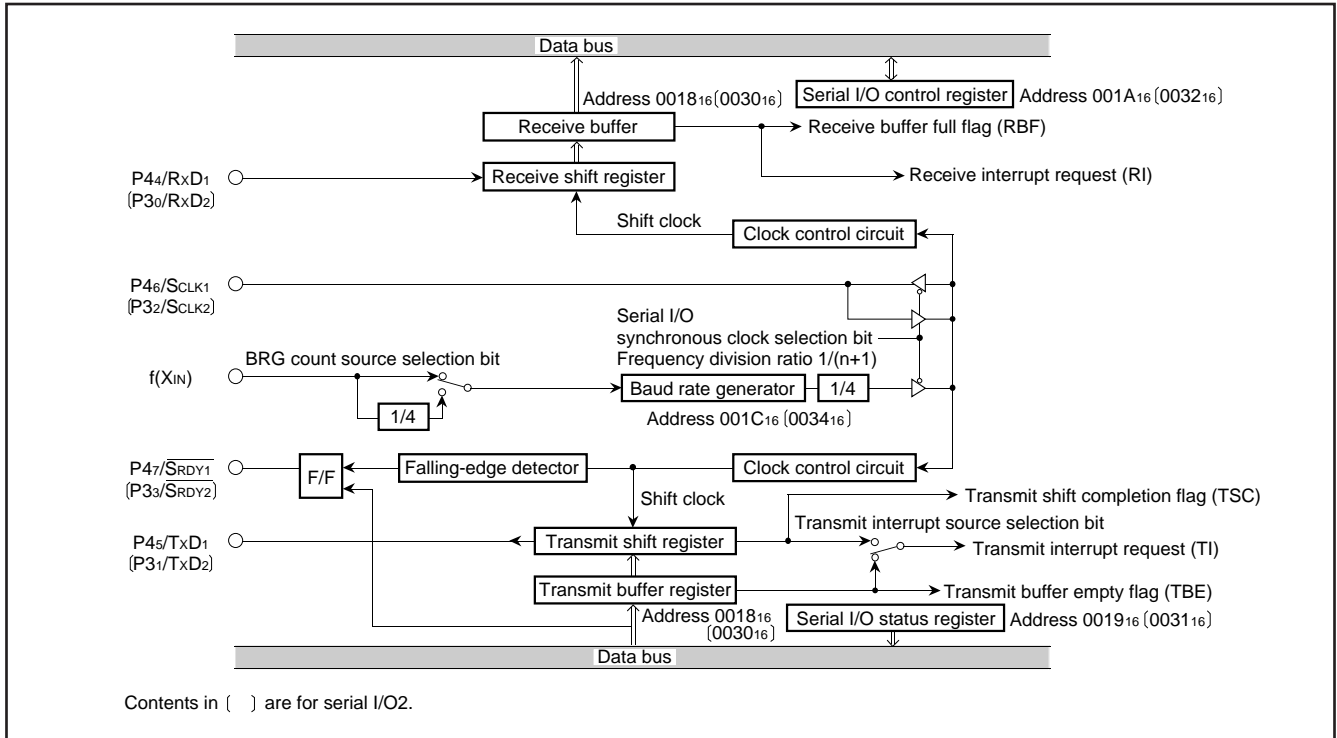


Fig. 13 Block diagram of clock synchronous serial I/O

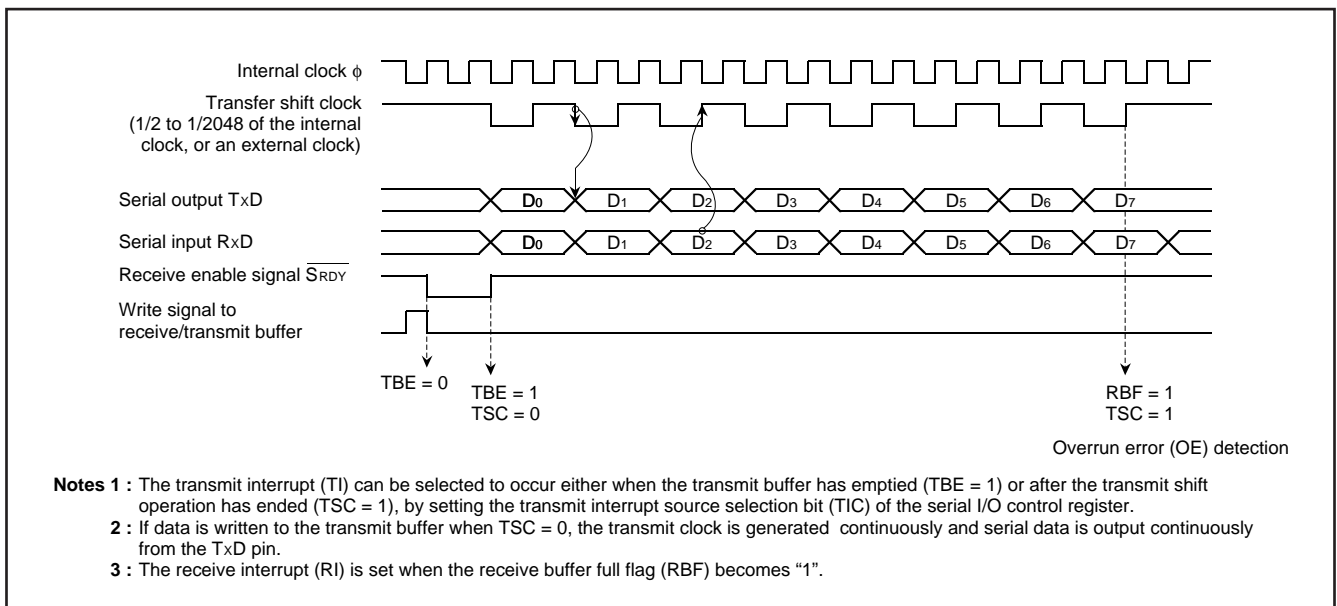


Fig. 14 Operation of clock synchronous serial I/O function

Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer,

but the two buffers have the same address in memory.

Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

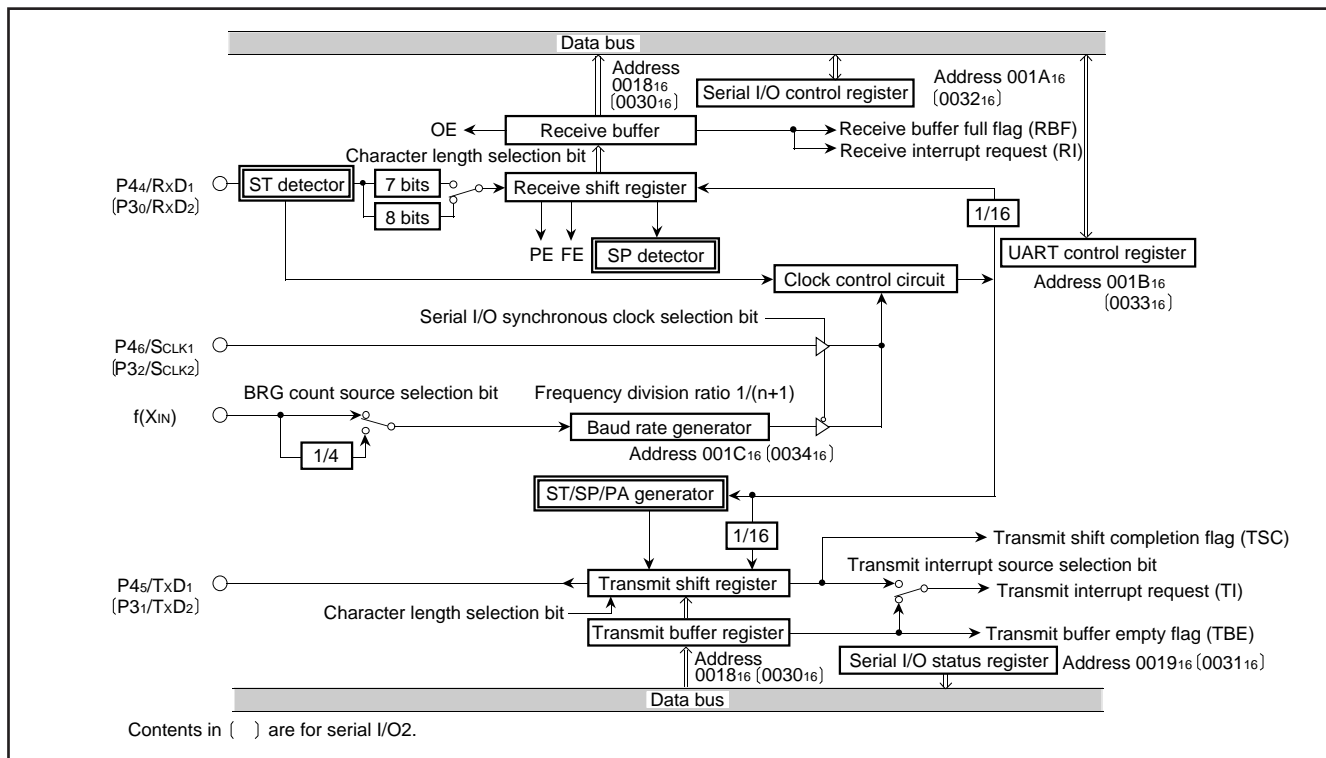
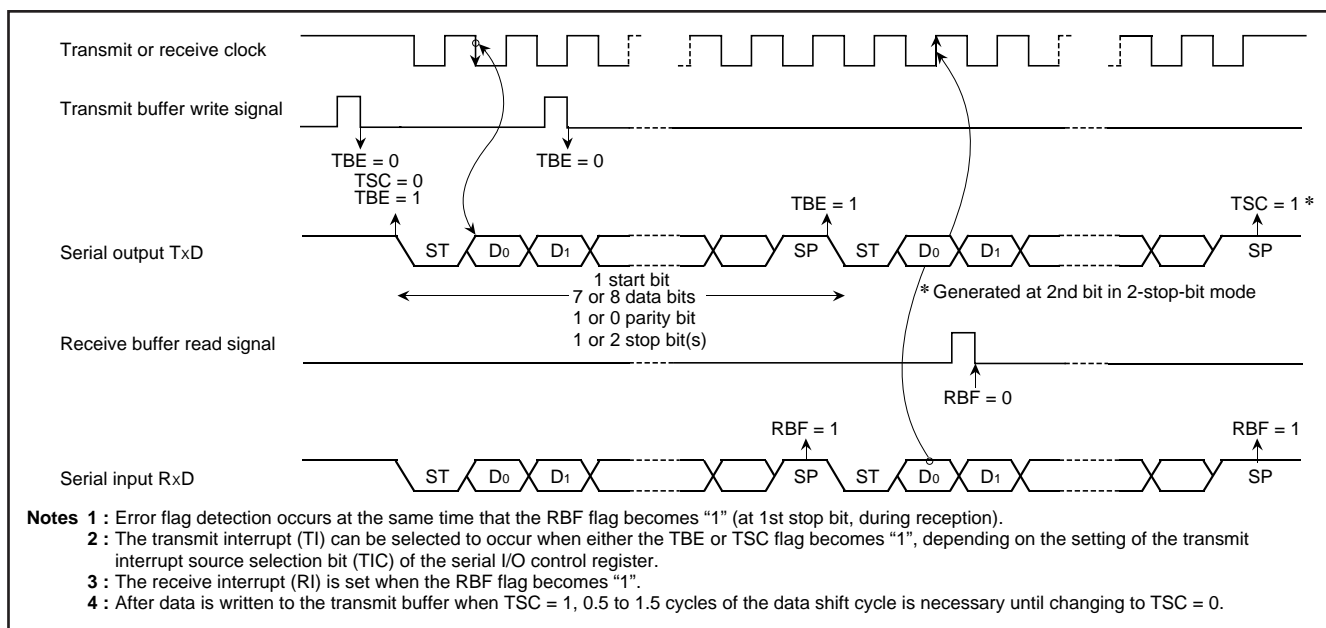


Fig. 15 Block diagram of UART serial I/O



- Notes 1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
- 2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
- 3 : The receive interrupt (RI) is set when the RBF flag becomes "1".
- 4 : After data is written to the transmit buffer when TSC = 1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC = 0.

Fig. 16 Operation of UART serial I/O function

Serial I/O Control Register
SIO1CON (001A16), SIO2CON (003216)

The serial I/O control register consists of eight control bits for the serial I/O function.

UART Control Register
UART1CON (001B16), UART2CON (003316)

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P45/TxD1 (P31/TxD2) pin.

Serial I/O Status Register
SIO1STS (001916), SIO2STS (003116)

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. Writing to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the serial I/O control register) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

Transmit Buffer Register/Receive Buffer Register
TB1/RB1 (001816), TB2/RB2 (003016)

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only.

If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is "0".

Baud Rate Generator
BRG1 (001C16), BRG2 (003416)

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n+1)$, where n is the value written to the baud rate generator.

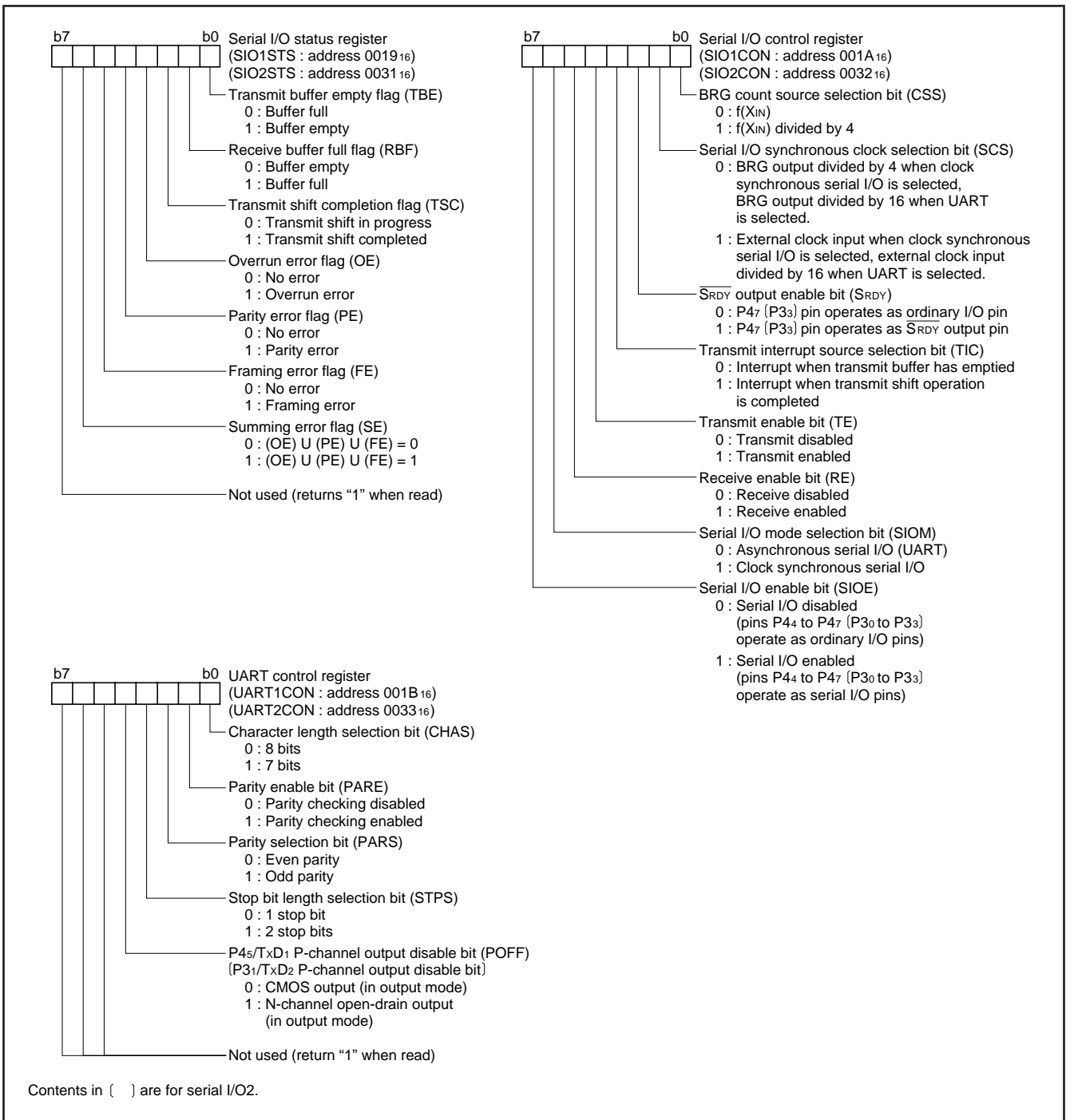


Fig. 17 Structure of serial I/O control registers

LCD CONTROLLER/DRIVER

The 7510 group has a built-in Liquid Crystal Display (LCD) controller/driver consisting of the following.

- A 160-byte LCD display RAM
- Segment drivers
- Common drivers
- A timing generator
- A built-in bias resistor

- A timing controller
- An LCD mode register
- An LCD contrast control register
- An LCD contrast controller

A maximum of eighty segment output pins (SEG0–SEG79) and sixteen common output pins (COM0–COM15) can be used to control an external LCD display controller.

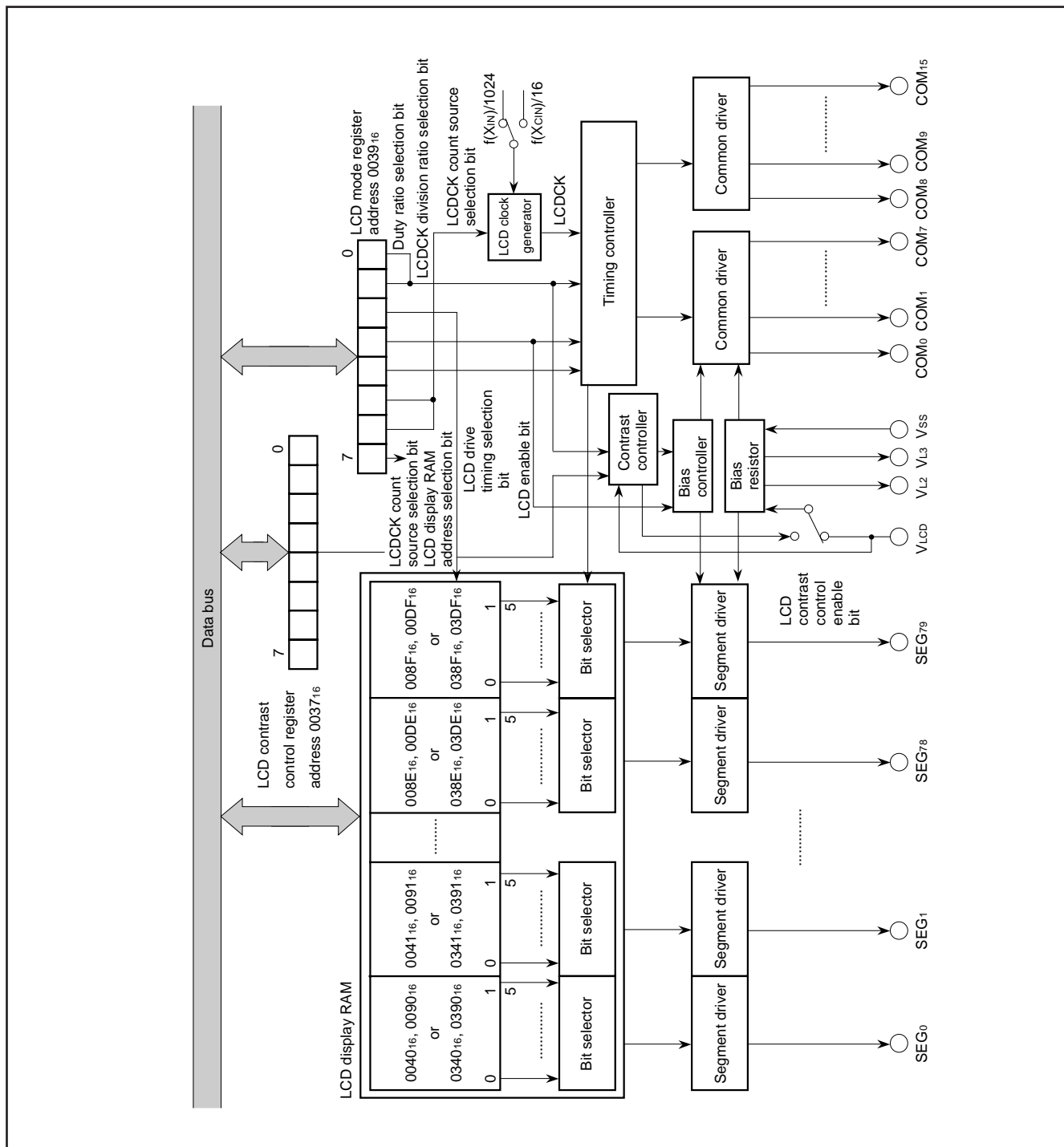


Fig. 18 Block diagram of LCD controller/driver

LCD Controller/Driver Function

The controller/driver reads the display data, performs bias and duty ratio control, and outputs the correct LCD timing signals on the segment and common pins according to the data in LCD display RAM.

LCD Mode Register LM (0039₁₆)

The LCD mode register is an 8-bit register. This register is used to match the characteristics of the controller/driver to the LCD panel used.

Table 2 Maximum number of display pixels for each duty ratio

| Duty ratio | Maximum number of display pixels |
|------------|-----------------------------------------------------------------------------|
| 1/8 | 8 X 80 dots (16 characters (5 X 7 dots/1 character) + cursor) X 1 line |
| 1/11 | 11 X 80 dots (16 characters (5 X 10 dots/1 character) + cursor) X 1 line |
| 1/16 | 16 X 80 dots (16 characters (5 X 7 dots/1 character) + cursor) X 2 line |

Note: Prior to executing an STP instruction, the LCD must be disabled by clearing the bit 3 of the LCD mode register to "0".

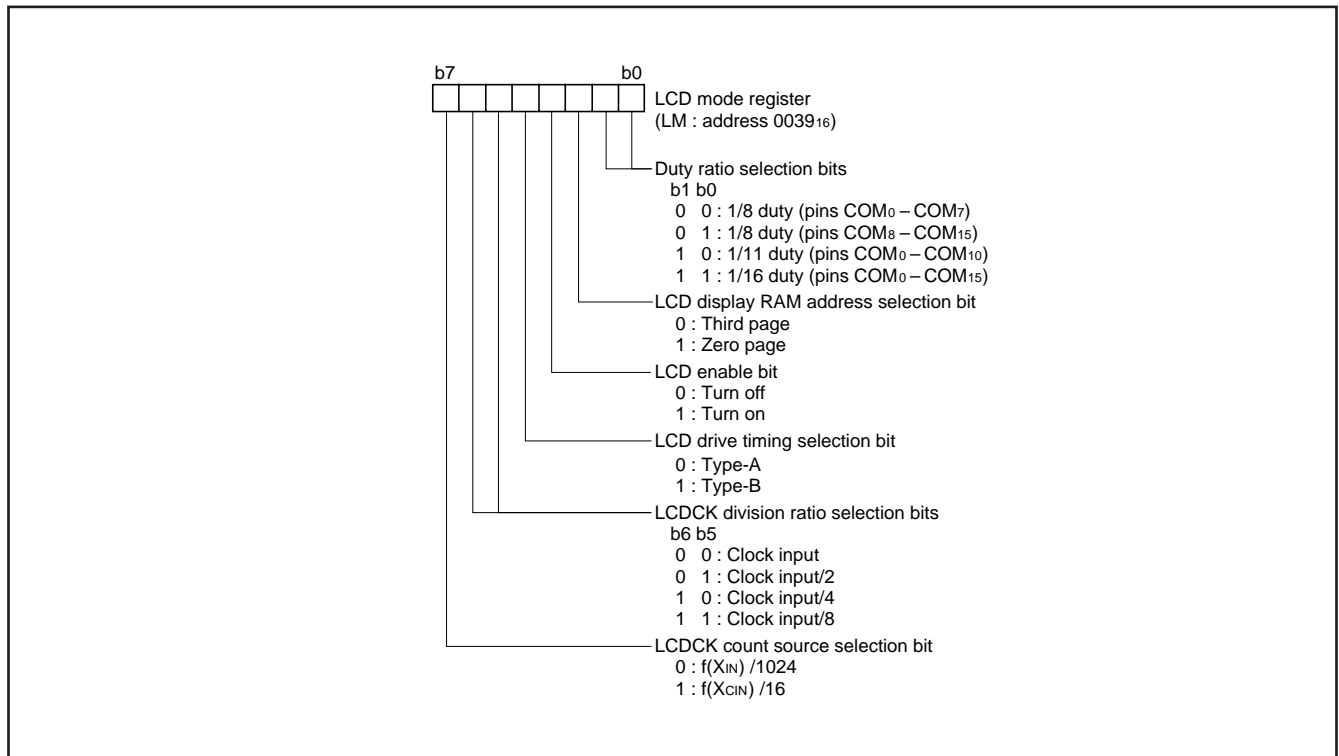


Fig. 19 Structure of LCD mode register

Bias Control and Time Division Control

The LCD controller/driver has built-in bias resistor and supports 1/4 bias or 1/5 bias. The bias setting is made by either floating pins VL2 and VL3 (1/5 bias) or shorting them together externally (1/4 bias). The number of common pins driven is determined by the duty ratio selected. Bits 0 and 1 of the LCD mode register are used to set the duty ratio.

Table 3 Time division control

| Duty ratio | Duty ratio selection bit | | Common pins used |
|------------|--------------------------|-------|------------------|
| | Bit 1 | Bit 0 | |
| 1/8 | 0 | 0 | COM0–COM7 |
| | 0 | 1 | COM8–COM15 |
| 1/11 | 1 | 0 | COM0–COM10 |
| 1/16 | 1 | 1 | COM0–COM15 |

Note: For all duty ratios, the unused common pins output the non-select waveform.

Contrast Controller

The contrast controller is a circuit generating 32 steps of voltages using the voltage applied to the VLCD pin as the reference voltage. The voltage generated varies depending on the values given to bit 0–bit 4 with the LCD contrast control register. When bit 7 of the LCD contrast control register is set to “1”, the voltage generated by the contrast controller is applied to VL5. Given below is the relation between the values set to bit 0–bit 4 of LCD contrast control register and the voltages applied to VL5.

Voltage applied to VL5
 = Voltage applied to the VLCD pin X (n+33)/64

Where:
 n = Value set to bit 0–bit 4 of the LCD contrast control register (in decimal values)

When the contrast controller is used, it becomes possible to apply 32 steps of voltage to VL5 from 1/2 VLCD through VLCD. Consequently, 32 steps of contrast adjustment by the software becomes possible.

Note: Supply power to the contrast controller from an external source through the VLCD pin. Also, when bit 7 of the LCD contrast control register is set to “0”, VLCD pin is coupled directly to VL5 (the contrast controller and VL5 become separated). In this case, perform contrast adjustment using an external circuit.

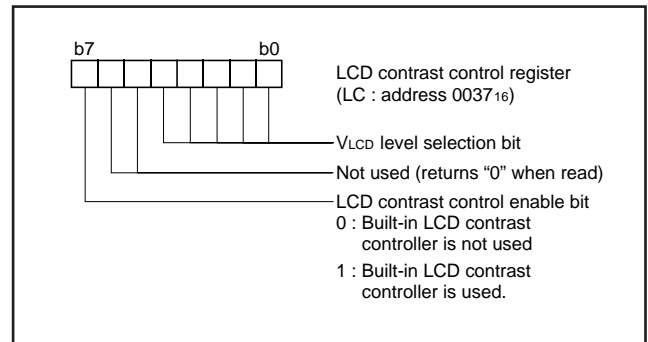


Fig. 22 Structure of LCD contrast control register

LCD Drive Timing

The LCD controller/driver supports both type-A and type-B drive timing.

The desired type is selected by setting the LCD drive timing selection bit (bit 4 of the LCD mode register).

If the LCD drive timing selection bit is set to “0”, type-A is selected, and if this bit is set to “1”, type-B is selected. After reset, type-A is selected for the drive timing.

The frame frequency can be determined by the following equation:

$$\text{Frame frequency} = \frac{\text{LCDCK count source frequency}}{\text{LCDCK division ratio} \times \text{duty ratio}}$$

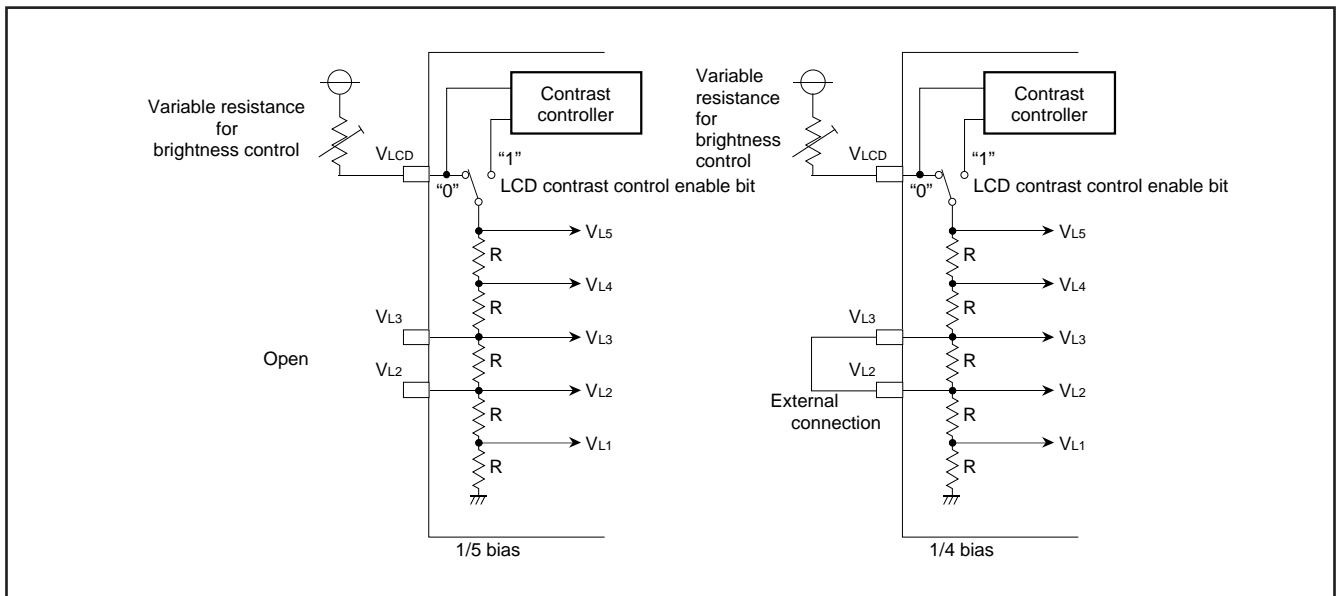


Fig. 21 Example of circuit at 1/5 and 1/4 bias

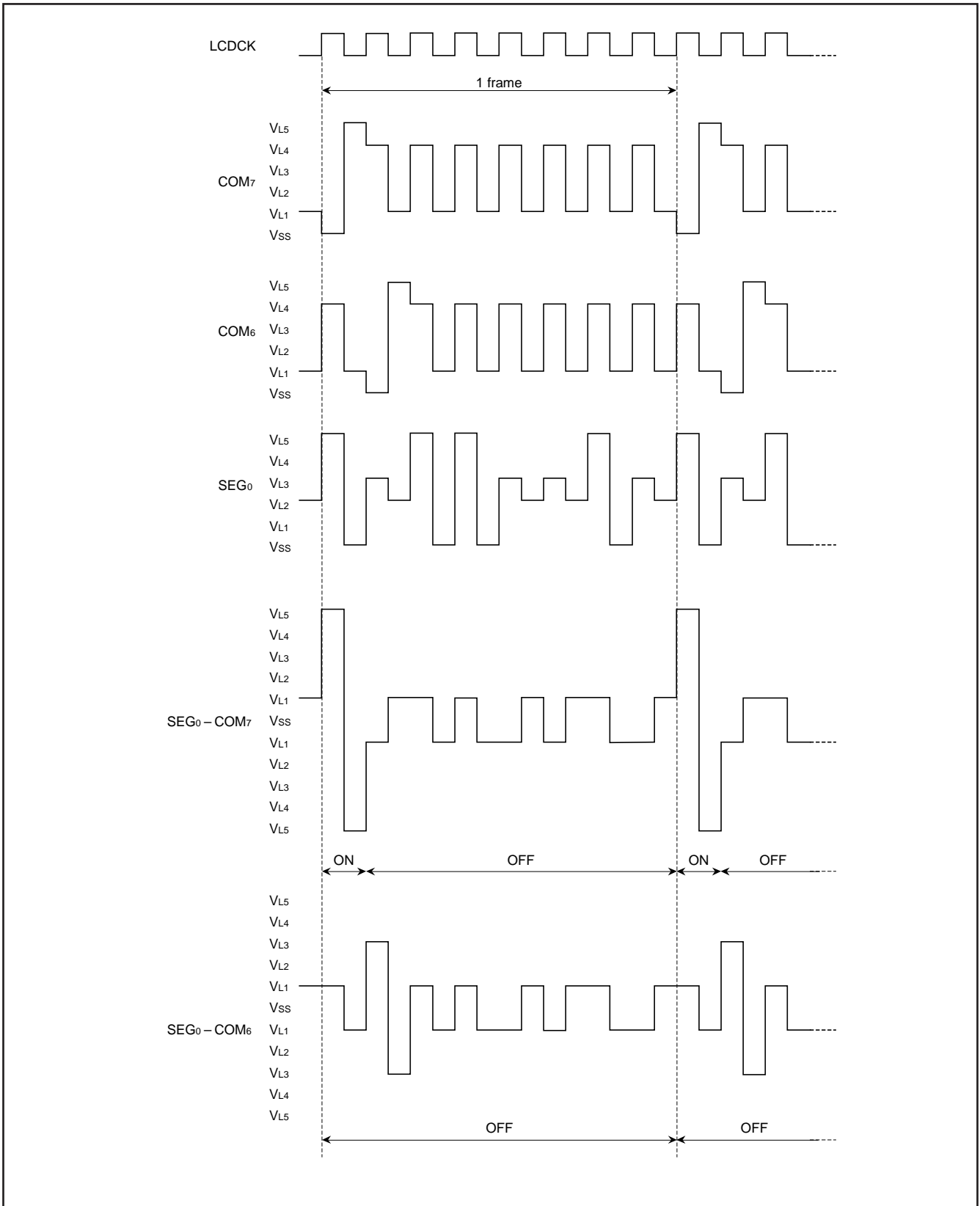


Fig. 23 1/8 duty, 1/5 bias, type-A LCD wave diagram

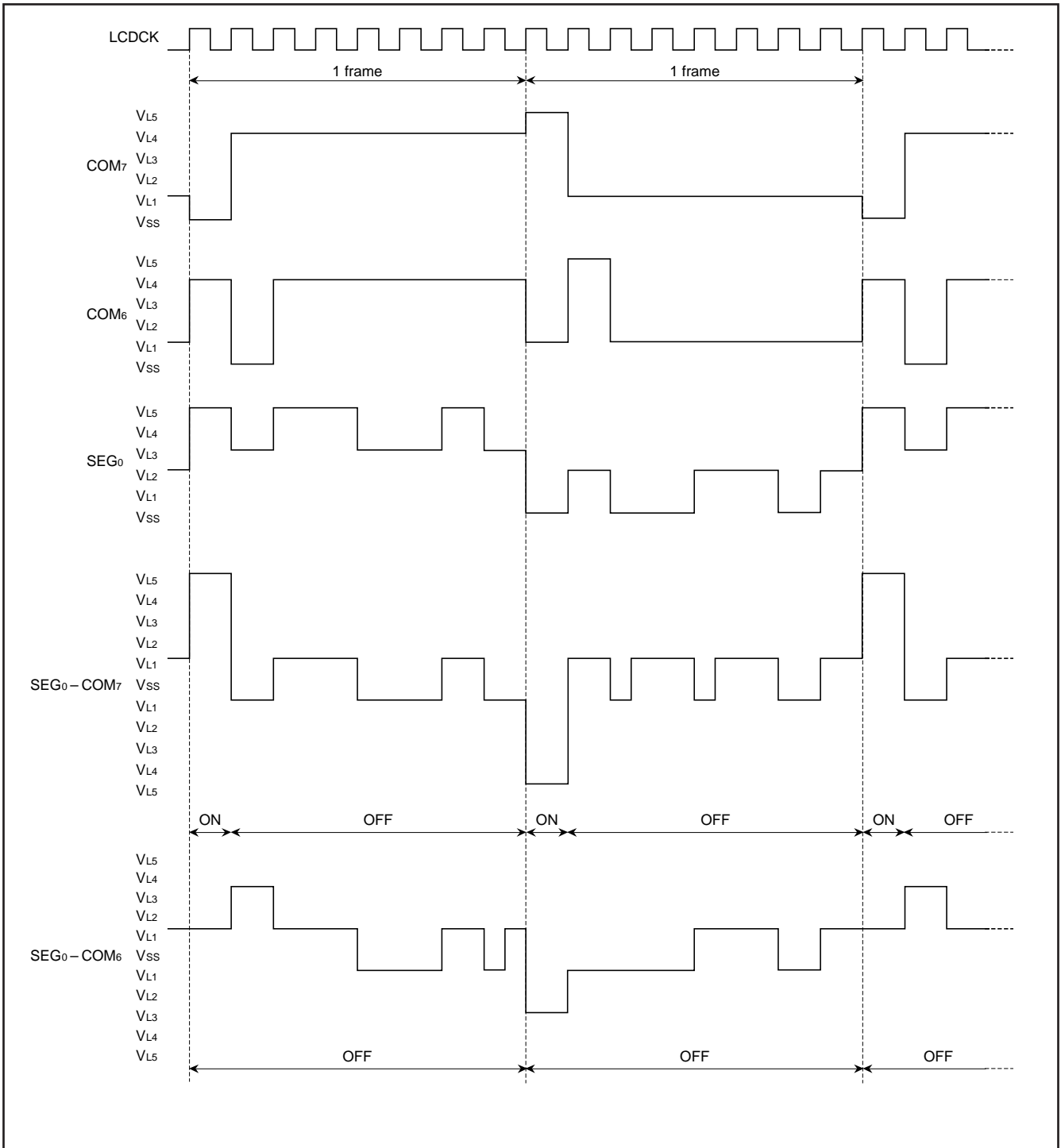


Fig. 24 1/8 duty, 1/5 bias, type-B LCD wave diagram

KEY-ON WAKE UP

The 7510 group contains a key-on wake up interrupt function. The key-on wake up interrupt function is one way of returning from a power down state caused by the STP or WIT instruction.

This interrupt is generated by applying "L" level to any pin of port P2 and the microcomputer is returned to the normal operating state. If a key matrix is connected to port P2₀ to P2₃ as shown in Figure 25, the microcomputer can be returned to a normal state by pressing any one of the keys.

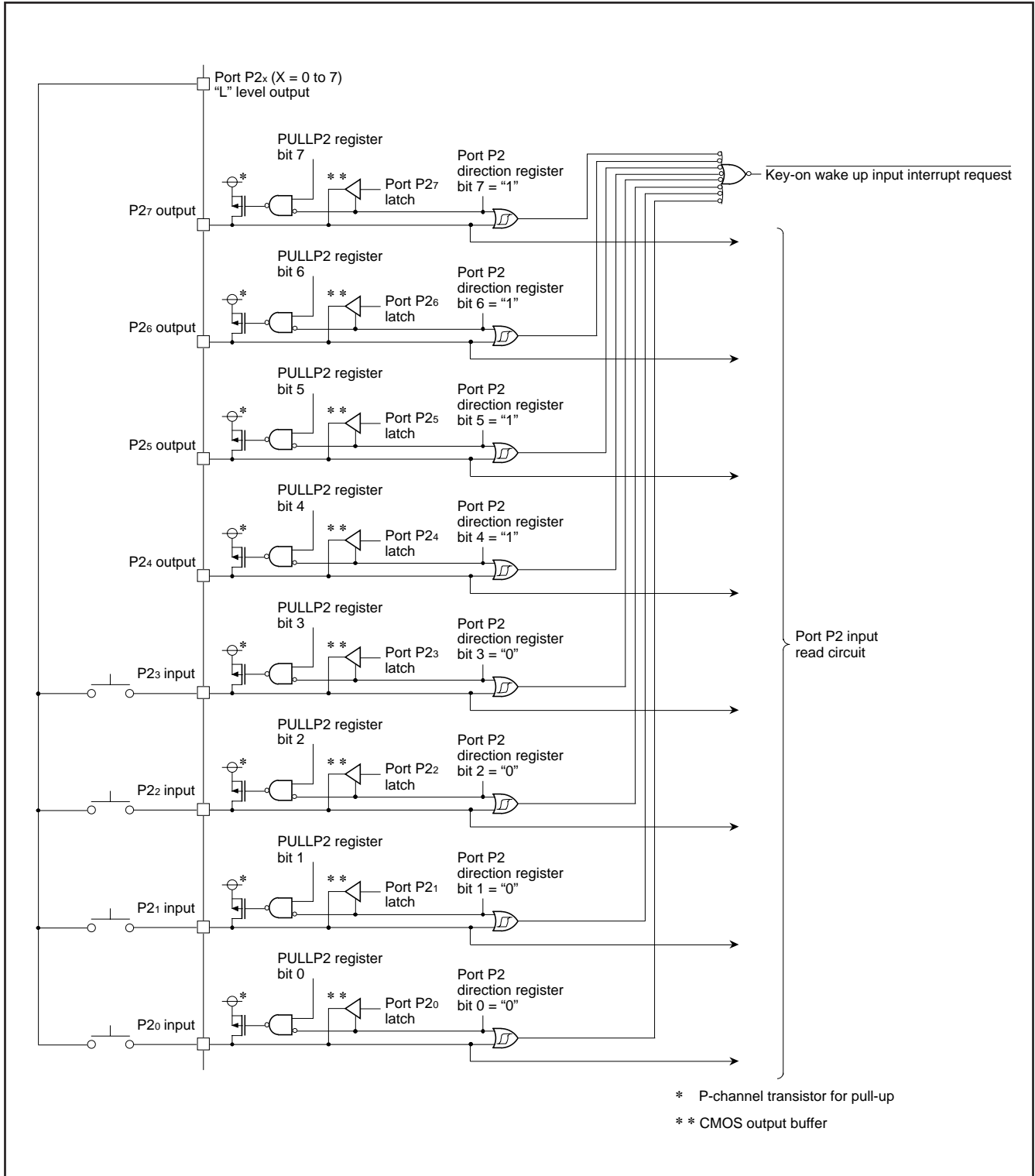


Fig. 25 Block diagram of port P2, and example of wired at used key-on wake up

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at "L" level for 2 μs or more. Then $\overline{\text{RESET}}$ pin is returned to "H" level (the power source voltage should be between 2.5 V and 5.5 V, and X_{IN} oscillation width is stable), reset is released. In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after about 8000 X_{IN} clock cycles are complete. After the reset is completed, the program starts from the address contained in address FFFD_{16} (high-order) and address FFFC_{16} (low-order). Make sure that the reset input voltage is less than 0.5 V for V_{CC} of 3.0 V at $f(X_{\text{IN}}) = 8.0 \text{ MHz}$.

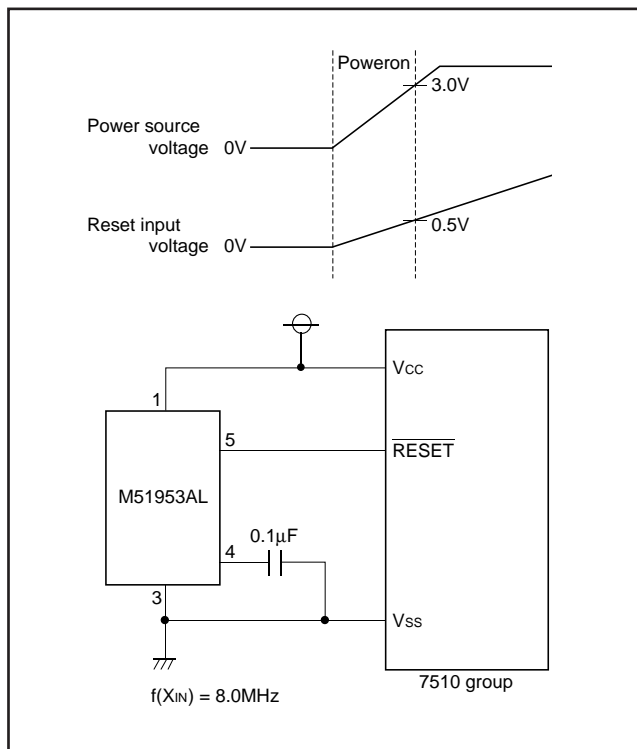


Fig. 26 Example of reset circuit

| | Address | Register contents |
|----------------------------------------|--------------------|-------------------------------------------|
| (1) Port P0 direction register | 0001 ₁₆ | 00 ₁₆ |
| (2) Port P1 direction register | 0003 ₁₆ | 00 ₁₆ |
| (3) Port P2 direction register | 0005 ₁₆ | 00 ₁₆ |
| (4) Port P3 direction register | 0007 ₁₆ | 00 ₁₆ |
| (5) Port P4 direction register | 0009 ₁₆ | 00 ₁₆ |
| (6) Port P5 direction register | 000B ₁₆ | 00 ₁₆ |
| (7) Port P0 pull-up control register | 000C ₁₆ | 00 ₁₆ |
| (8) Port P1 pull-up control register | 000D ₁₆ | 00 ₁₆ |
| (9) Port P2 pull-up control register | 000E ₁₆ | 00 ₁₆ |
| (10) Port P3 pull-up control register | 000F ₁₆ | 00 ₁₆ |
| (11) Port P4 pull-up control register | 0010 ₁₆ | 00 ₁₆ |
| (12) Port P5 pull-up control register | 0011 ₁₆ | 00 ₁₆ |
| (13) Serial I/O1 status register | 0019 ₁₆ | 1 0 0 0 0 0 0 0 |
| (14) Serial I/O1 control register | 001A ₁₆ | 00 ₁₆ |
| (15) UART1 control register | 001B ₁₆ | 1 1 1 0 0 0 0 0 |
| (16) Timer X (low) | 0020 ₁₆ | FF ₁₆ |
| (17) Timer X (high) | 0021 ₁₆ | FF ₁₆ |
| (18) Timer Y (low) | 0022 ₁₆ | FF ₁₆ |
| (19) Timer Y (high) | 0023 ₁₆ | FF ₁₆ |
| (20) Timer 1 | 0024 ₁₆ | FF ₁₆ |
| (21) Timer 2 | 0025 ₁₆ | 01 ₁₆ |
| (22) Timer 3 | 0026 ₁₆ | FF ₁₆ |
| (23) Timer X mode register | 0027 ₁₆ | 00 ₁₆ |
| (24) Timer Y mode register | 0028 ₁₆ | 00 ₁₆ |
| (25) Timer 123 mode register | 0029 ₁₆ | 00 ₁₆ |
| (26) Serial I/O2 status register | 0031 ₁₆ | 1 0 0 0 0 0 0 0 |
| (27) Serial I/O2 control register | 0032 ₁₆ | 00 ₁₆ |
| (28) UART2 control register | 0033 ₁₆ | 1 1 1 0 0 0 0 0 |
| (29) LCD contrast control register | 0037 ₁₆ | 00 ₁₆ |
| (30) LCD mode register | 0039 ₁₆ | 00 ₁₆ |
| (31) Interrupt edge selection register | 003A ₁₆ | 00 ₁₆ |
| (32) CPU mode register | 003B ₁₆ | 0 1 0 0 1 1 0 0 |
| (33) Interrupt request register 1 | 003C ₁₆ | 00 ₁₆ |
| (34) Interrupt request register 2 | 003D ₁₆ | 00 ₁₆ |
| (35) Interrupt control register 1 | 003E ₁₆ | 00 ₁₆ |
| (36) Interrupt control register 2 | 003F ₁₆ | 00 ₁₆ |
| (37) Processor status register | (PS) | X X X X X 1 X X |
| (38) Program counter | (PC _H) | Contents of address FFFD ₁₆ |
| | (PC _L) | Contents of address FFFC ₁₆ |

Note : The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.
X : Undefined

Fig. 27 Internal status of microcomputer after reset

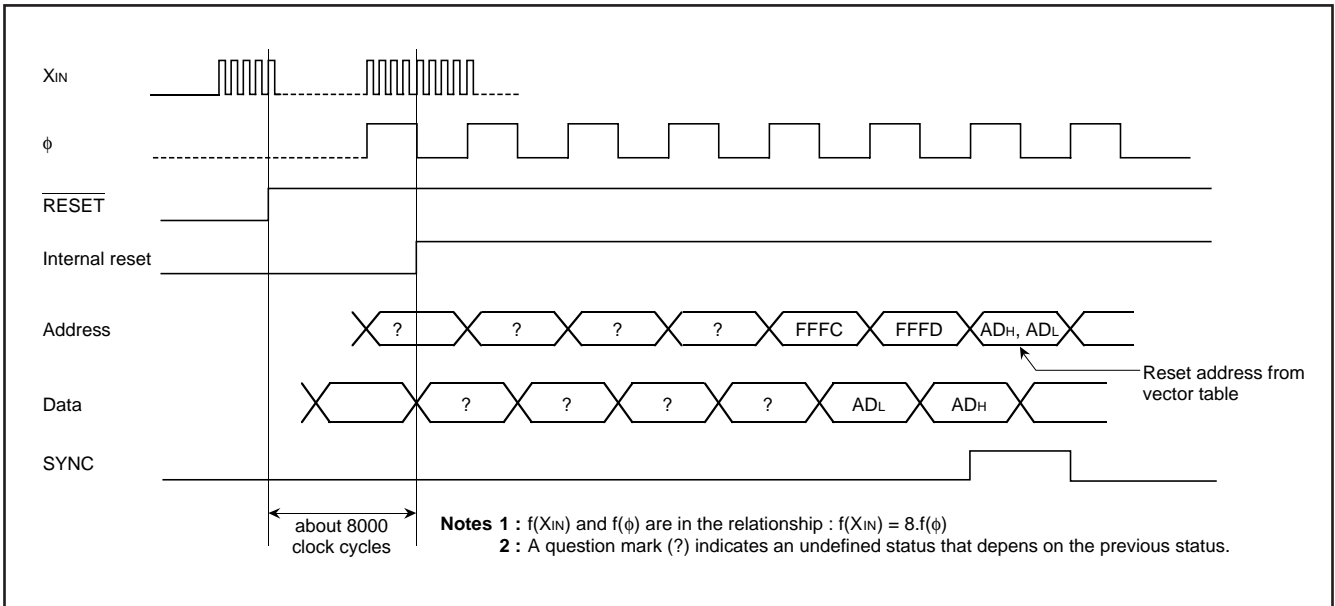


Fig. 28 Reset sequence

CLOCK GENERATING CIRCUIT

The 7510 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O port. The pull-up resistor of XCIN and XCOUT pins must be made invalid to use the XCIN oscillating circuit.

Frequency Control

Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset, this mode is selected.

High-speed mode

The internal clock ϕ is half the frequency of XIN.

Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

Note: If you switch the mode between middle/high-speed and low-speed, both of XIN and XCIN oscillation must be stabilized. The sufficient time is required for the XCIN oscillation to stabilize, especially immediately after power-on and at returning from stop mode. The mode must be switched on condition that $f(XIN) > 3f(XCIN)$.

Low-power consumption mode

In low-speed mode, a low-power consumption operation can be entered by stopping the main clock XIN. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock XIN is restarted, the program must allow enough time for oscillation to stabilize.

In low-power consumption mode, the XCIN-XCOUT drive performance can be reduced, allowing lower power consumption (8 μ A or less with XCIN = 32 kHz). To reduce the XCIN-XCOUT drive performance, clear bit 3 of the CPU mode register to "0". At reset or when the STP instruction is executed, this bit is set to "1" and strong drive is selected to help the oscillation to start.

Oscillation Control

Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level. Timer 1 is set to "FF16" and timer 2 is set to "0116".

Either XIN or XCIN divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The bits of the timer 123 mode register are cleared to "0" except for bit 4.

The timer 1 and timer 2 interrupt enable bits must be set to disabled ("0"), so a program must set these bits before executing a STP instruction. Oscillation restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. XIN and XCIN are the same state with that before the execution of the WIT instruction. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

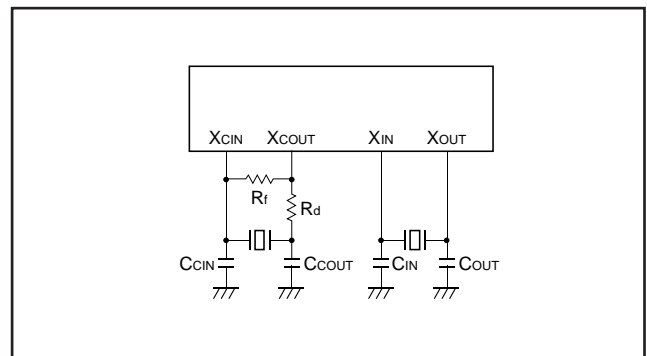


Fig. 29 Ceramic resonator circuit

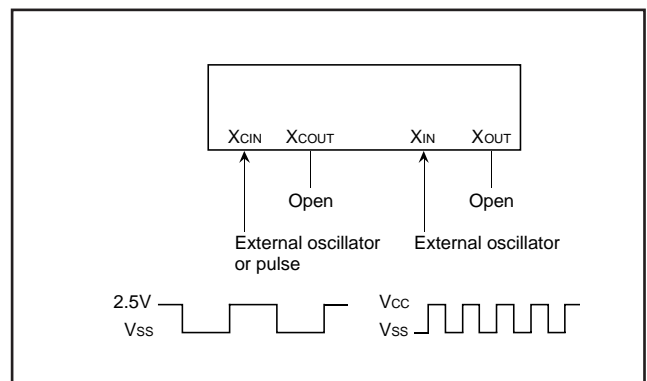


Fig. 30 External clock input circuit

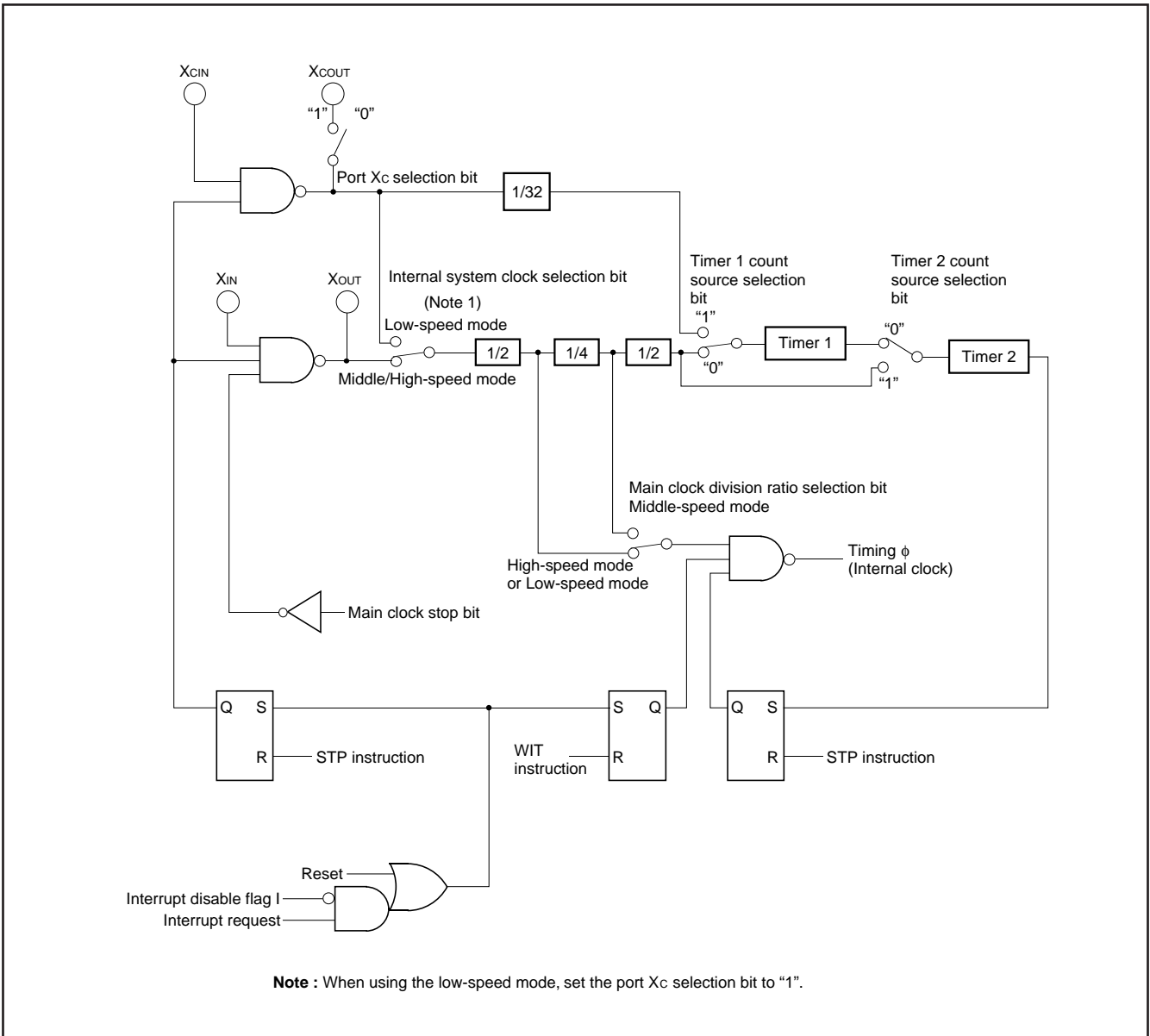


Fig. 31 System clock generating circuit block diagram

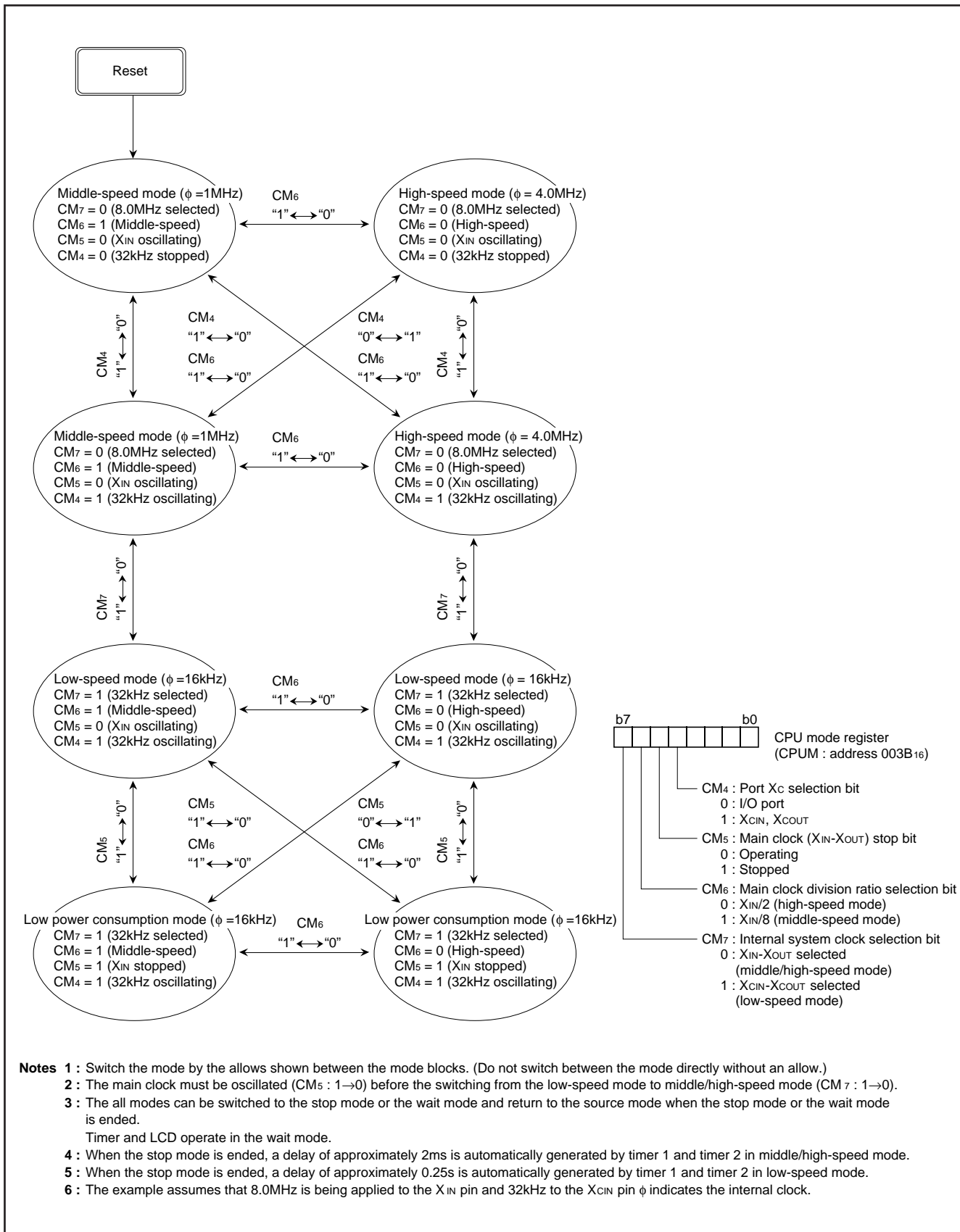


Fig. 32 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal operation mode (D) flag because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written.

After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal operation mode flag (D) to "1", then execute the ADC or the SBC instruction. Only the ADC and the SBC instruction yield proper decimal results. After executing the ADC or SBC instruction, execute at least one instruction before executing the SEC, the CLC, or the CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flag are invalid. The carry flag can be used to indicate whether a carry or borrow has occurred.

Initialize the carry flag before each calculation. Clear the carry flag before the ADC instruction and set the flag before the SBC instruction.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

The index X mode (T) and the decimal mode (D) flag do not affect the MUL and DIV instruction.

The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.

The following cannot be used:

- the data transfer instruction (LDA, etc.)
- the operation instruction when the index X mode flag (T) is "1"
- the addressing mode which uses the value of a direction register as an index
- the bit-test instruction (BBC or BBS, etc.) to a direction register
- the read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".

Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

In high-speed mode, the frequency of the internal clock ϕ is half of the X_{IN} frequency.

In middle-speed mode, the frequency of the internal clock ϕ is one eighth the X_{IN} frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form
2. Mask Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

PROM Programming Method

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Set the address of PROM programmer in the user ROM area.

| Package | Name of Programming Adapter |
|----------|-----------------------------|
| 176P6D-A | PCA4738F-176A |

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 33 is recommended to verify programming.

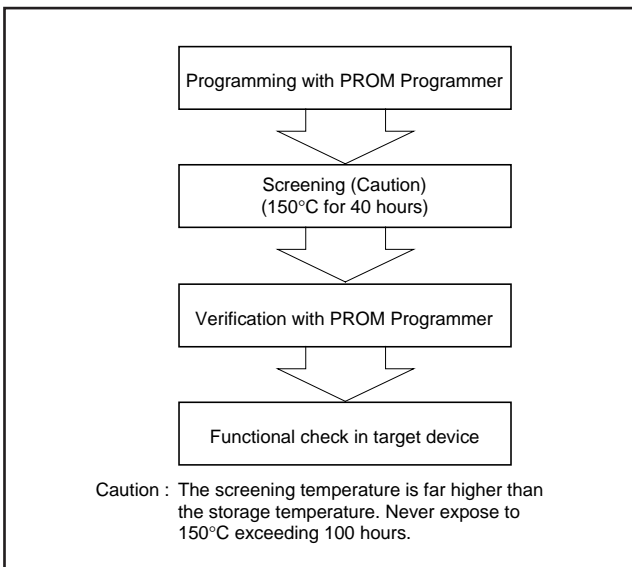


Fig. 33 Programming and testing of One Time PROM version

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Retings | Unit |
|--------|----------------------------------------------------------------------------|------------------------------------------------------------------|-----------------|------|
| VCC | Power source voltage | | -0.3 to 7.0 | V |
| VI | Input voltage P00-P07, P10-P17, P20-P27, P30-P37, P41-P47, P50, P51 | All voltage are based on Vss. Output transistors are cut off. | -0.3 to VCC+0.3 | V |
| VI | Input voltage P40 | | -0.3 to 13 | V |
| VI | Input voltage VLCD | | -0.3 to VCC+0.3 | V |
| VI | Input voltage RESET, XIN, XCIN | | -0.3 to VCC+0.3 | V |
| VO | Output voltage P00-P07, P10-P17, P20-P27, P30-P37, P41-P47, P50, P51, XOUT | | -0.3 to VCC+0.3 | V |
| VO | Output voltage SEG0-SEG79, COM0-COM15 | | -0.3 to VLCD | V |
| VO | Output voltage XCOU | | -0.3 to VCC | V |
| Pd | Power dissipation | | Ta = 25°C | 300 |
| Topr | Operating temperature | | -20 to 85 | °C |
| Tstg | Storage temperature | | -40 to 125 | °C |

RECOMMENDED OPERATING CONDITIONS (VCC = 4.0 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit | |
|----------------------|----------------------------------------------------------------------------------------------|------------------------------------------------------------|--------|--------|------|---|
| | | Min. | Typ. | Max. | | |
| VCC | Power source voltage | High-speed mode $f(\phi) \geq 2.5$ MHz | 4.0 | 5.0 | 5.5 | V |
| | | Middle-speed mode $1.0 \text{ MHz} \leq f(\phi) < 2.5$ MHz | 3.0 | 5.0 | 5.5 | V |
| | | Low-speed mode $f(\phi) \leq 650$ kHz | 2.5 | 5.0 | 5.5 | V |
| VLCD | Power source voltage for LCD driver | | | VCC | V | |
| VSS | Power source voltage | | 0 | | V | |
| VIH | "H" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50, P51 | 0.8VCC | | VCC | V | |
| VIH | "H" input voltage RESET, XIN | 0.8VCC | | VCC | V | |
| VIH | "H" input voltage XCIN | | | 2.5 | V | |
| VIL | "L" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50, P51 | 0 | | 0.2VCC | V | |
| VIL | "L" input voltage RESET, XIN | 0 | | 0.2VCC | V | |
| VIL | "L" input voltage XCIN | 0 | | 0.4 | V | |
| Σ IOH(peak) | "H" total peak output current (Note 1) P00-P07, P10-P17, P20-P27, P30-P37, P41-P47, P50, P51 | | | -80 | mA | |
| Σ IOL(peak) | "L" total peak output current P00-P07, P10-P17, P20-P27, P30-P37, P41-P47, P50, P51 | | | 80 | mA | |
| Σ IOH(avg) | "H" total average output current P00-P07, P10-P17, P20-P27, P30-P37, P41-P47, P50, P51 | | | -40 | mA | |
| Σ IOL(avg) | "L" total average output current P00-P07, P10-P17, P20-P27, P30-P37, P41-P47, P50, P51 | | | 40 | mA | |
| IOH(peak) | "H" peak output current (Note 2) P00-P07, P10-P17, P20-P27, P30-P37, P41-P47, P50, P51 | | | -10 | mA | |
| IOL(peak) | "L" peak output current P00-P07, P10-P17, P20-P27, P30-P37, P41-P47, P50, P51 | | | 10 | mA | |
| IOH(avg) | "H" average output current (Note 3) P00-P07, P10-P17, P20-P27, P30-P37, P41-P47, P50, P51 | | | -5 | mA | |
| IOL(avg) | "L" average output current P00-P07, P10-P17, P20-P27, P30-P37, P41-P47, P50, P51 | | | 5 | mA | |
| f(CNTR0) f(CNTR1) | Timer X, Timer Y input frequency (at 50% duty) | | | 2.6 | MHz | |
| f(XIN) | Main clock input oscillation frequency (Note 4) | | | 8.0 | MHz | |
| f(XCIN) | Sub-clock input oscillation frequency (Note 4, 5) | | 32.768 | 50 | kHz | |

- Notes**
- 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
 - 2: The peak output current is the peak current flowing in each port.
 - 3: The average output current is an average value measured over 100 ms.
 - 4: The oscillating frequency has a 50% duty cycle.
 - 5: In low-speed mode, the sub-clock input oscillation frequency must be used on condition that $f(XCIN) < f(XIN)/3$.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit | |
|-----------------|--------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|------|---------------|---------------|---------------|
| | | | Min. | Typ. | Max. | | |
| V_{OH} | "H" output voltage P00–P07, P10–P17, P20–P27, P30–P37, P41–P47, P50, P51 | $I_{OH} = -10$ mA | $V_{CC}-2.0$ | | | V | |
| V_{OL} | "L" output voltage P00–P07, P10–P17, P20–P27, P30–P37, P41–P47, P50, P51 | $I_{OL} = 10$ mA | | | 2.0 | V | |
| $V_{T+}-V_{T-}$ | Hysteresis INT0, INT1, CNTR0, CNTR1 | | | 0.4 | | V | |
| $V_{T+}-V_{T-}$ | Hysteresis SCLK1, SCLK2, RxD1, RxD2 | | | 0.5 | | V | |
| $V_{T+}-V_{T-}$ | Hysteresis $\overline{\text{RESET}}$ | | | 0.5 | | V | |
| I_{IH} | "H" input current P00–P07, P10–P17, P20–P27, P30–P37, P41–P47, P50, P51 | | | | 5.0 | μA | |
| I_{IH} | "H" input current $\overline{\text{RESET}}$, P40 | $V_i = V_{CC}$ | | | 5.0 | μA | |
| I_{IH} | "H" input current X_{IN} | $V_i = V_{CC}$ | | 4.0 | | μA | |
| I_{IH} | "H" input current X_{CIN} | $V_i = 2.5$ V | | 2.0 | | μA | |
| I_{IL} | "L" input current P00–P07, P10–P17, P20–P27, P30–P37, P41–P47, P50, P51 | $V_i = 0$ V Pull-ups "off" | | | -5.0 | μA | |
| | | $V_{CC} = 5$ V, $V_i = 0$ V Pull-ups "on" | -30 | -70 | -140 | μA | |
| | | $V_{CC} = 3$ V, $V_i = 0$ V Pull-ups "on" | -6 | -25 | -45 | μA | |
| I_{IL} | "L" input current $\overline{\text{RESET}}$, P40 | $V_i = V_{SS}$ | | | -5.0 | μA | |
| I_{IL} | "L" input current X_{IN} | $V_i = V_{SS}$ | | -4.0 | | μA | |
| I_{IL} | "L" input current X_{CIN} | $V_i = V_{SS}$ | | -2.0 | | μA | |
| V_{RAM} | RAM hold voltage | With clock stopped | 2.0 | | 5.5 | V | |
| R_{bias} | LCD bias resistance (Note) | | | 3 | | k Ω | |
| R_{COM5} | COM on-resistance with VL5 output from COM | $I_o = -0.1$ mA | | | 0.5 | k Ω | |
| R_{COM4} | COM on-resistance with VL4 output from COM | $I_o = \pm 0.1$ mA | | | 4.5 | k Ω | |
| R_{COM1} | COM on-resistance with VL1 output from COM | $I_o = \pm 0.1$ mA | | | 4.5 | k Ω | |
| R_{COM0} | COM on-resistance with VL0 output from COM | $I_o = 0.1$ mA | | | 0.5 | k Ω | |
| R_{SEG5} | SEG on-resistance with VL5 output from SEG | $I_o = -0.1$ mA | | | 0.5 | k Ω | |
| R_{SEG3} | SEG on-resistance with VL3 output from SEG | $I_o = \pm 0.1$ mA | | | 6.5 | k Ω | |
| R_{SEG2} | SEG on-resistance with VL2 output from SEG | $I_o = \pm 0.1$ mA | | | 6.5 | k Ω | |
| R_{SEG0} | SEG on-resistance with VL0 output from SEG | $I_o = 0.1$ mA | | | 0.5 | k Ω | |
| I_{CC} | Power source current | In high-speed mode, $V_{CC} = 5$ V Output transistors are isolated. | $f(X_{IN}) = 8.0$ MHz | | 6.4 | 13 | mA |
| | | | $f(X_{IN}) = 5.0$ MHz | | 4.0 | 8.0 | mA |
| | | In low-speed mode, $V_{CC} = 3$ V $f(X_{IN}) =$ stopped $f(X_{CIN}) = 32$ kHz Low-power consumption mode Output transistors are isolated. | | | 20 | | μA |
| | | In low-speed mode, $V_{CC} = 3$ V $f(X_{IN}) =$ stopped $f(X_{CIN}) = 32$ kHz (in wait mode) Low-power consumption mode Output transistors are isolated. | | | 4.5 | 9.0 | μA |
| | | All oscillation are stopped. (in stop mode) Output transistors are isolated. | $T_a = 25^\circ\text{C}$ | | 0.1 | 1.0 | μA |
| | $T_a = 85^\circ\text{C}$ | | | 10 | μA | | |

Note: This is the value of bias resistance for one stage.

LCD CONTRAST CONTROLLER CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|------------------|-------------------------------|--------------------------------------|--------|------|-----------|------|
| | | | Min. | Typ. | Max. | |
| - | Resolution | | | | 5 | Bits |
| - | Accuracy | | | | 2.0 | % |
| - | linearity | | | | ± 0.5 | LSB |
| V _{CCH} | Maximum output voltage (Note) | $V_{CC} = 5.0$ V, $V_{LCD} = V_{CC}$ | 4.9 | | V_{LCD} | V |

Note: When the value in the LCD contrast control register (address 003716) is "9F16".

TIMING REQUIREMENTS 1 ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-------------------------------------|-------------------------------------------------------------|--------|------|------|---------------|
| | | Min. | Typ. | Max. | |
| $t_{w(\overline{\text{RESET}})}$ | Reset input "L" pulse width | 2 | | | μs |
| $t_c(X_{IN})$ | External clock input cycle time | 125 | | | ns |
| $t_{wH}(X_{IN})$ | External clock input "H" pulse width | 50 | | | ns |
| $t_{wL}(X_{IN})$ | External clock input "L" pulse width | 50 | | | ns |
| $t_c(\text{CNTR})$ | CNTR ₀ , CNTR ₁ input cycle time | 200 | | | ns |
| $t_{wH}(\text{CNTR})$ | CNTR ₀ , CNTR ₁ input "H" pulse width | 80 | | | ns |
| $t_{wH}(\text{INT})$ | INT ₀ , INT ₁ input "H" pulse width | 80 | | | ns |
| $t_{wL}(\text{CNTR})$ | CNTR ₀ , CNTR ₁ input "L" pulse width | 80 | | | ns |
| $t_{wL}(\text{INT})$ | INT ₀ , INT ₁ input "L" pulse width | 80 | | | ns |
| $t_c(\text{SCLK1})$ | Serial I/O1 clock input cycle time (Note) | 800 | | | ns |
| $t_c(\text{SCLK2})$ | Serial I/O2 clock input cycle time (Note) | 800 | | | ns |
| $t_{wH}(\text{SCLK1})$ | Serial I/O1 clock input "H" pulse width (Note) | 370 | | | ns |
| $t_{wH}(\text{SCLK2})$ | Serial I/O2 clock input "H" pulse width (Note) | 370 | | | ns |
| $t_{wL}(\text{SCLK1})$ | Serial I/O1 clock input "L" pulse width (Note) | 370 | | | ns |
| $t_{wL}(\text{SCLK2})$ | Serial I/O2 clock input "L" pulse width (Note) | 370 | | | ns |
| $t_{su}(\text{Rx}D1\text{--SCLK1})$ | Serial I/O1 input set up time | 220 | | | ns |
| $t_{su}(\text{Rx}D2\text{--SCLK2})$ | Serial I/O2 input set up time | 220 | | | ns |
| $t_h(\text{SCLK1--Rx}D1)$ | Serial I/O1 input hold time | 100 | | | ns |
| $t_h(\text{SCLK2--Rx}D2)$ | Serial I/O2 input hold time | 100 | | | ns |

Note: When $f(\phi) = 4$ MHz and bit 6 of address 001A₁₆ or 0032₁₆ is "1" (clock synchronous). Divide this value by four when $f(\phi) = 4$ MHz and bit 6 of address 001A₁₆ or 0032₁₆ is "0" (clock asynchronous).

TIMING REQUIREMENTS 2 ($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-------------------------------------|-------------------------------------------------------------|--------|------|------|---------------|
| | | Min. | Typ. | Max. | |
| $t_{w(\overline{\text{RESET}})}$ | Reset input "L" pulse width | 2 | | | μs |
| $t_c(X_{IN})$ | External clock input cycle time | 500 | | | ns |
| $t_{wH}(X_{IN})$ | External clock input "H" pulse width | 200 | | | ns |
| $t_{wL}(X_{IN})$ | External clock input "L" pulse width | 200 | | | ns |
| $t_c(\text{CNTR})$ | CNTR ₀ , CNTR ₁ input cycle time | 500 | | | ns |
| $t_{wH}(\text{CNTR})$ | CNTR ₀ , CNTR ₁ input "H" pulse width | 230 | | | ns |
| $t_{wH}(\text{INT})$ | INT ₀ , INT ₁ input "H" pulse width | 230 | | | ns |
| $t_{wL}(\text{CNTR})$ | CNTR ₀ , CNTR ₁ input "L" pulse width | 230 | | | ns |
| $t_{wL}(\text{INT})$ | INT ₀ , INT ₁ input "L" pulse width | 230 | | | ns |
| $t_c(\text{SCLK1})$ | Serial I/O1 clock input cycle time (Note) | 2000 | | | ns |
| $t_c(\text{SCLK2})$ | Serial I/O2 clock input cycle time (Note) | 2000 | | | ns |
| $t_{wH}(\text{SCLK1})$ | Serial I/O1 clock input "H" pulse width (Note) | 950 | | | ns |
| $t_{wH}(\text{SCLK2})$ | Serial I/O2 clock input "H" pulse width (Note) | 950 | | | ns |
| $t_{wL}(\text{SCLK1})$ | Serial I/O1 clock input "L" pulse width (Note) | 950 | | | ns |
| $t_{wL}(\text{SCLK2})$ | Serial I/O2 clock input "L" pulse width (Note) | 950 | | | ns |
| $t_{su}(\text{Rx}D1\text{--SCLK1})$ | Serial I/O1 input set up time | 400 | | | ns |
| $t_{su}(\text{Rx}D2\text{--SCLK2})$ | Serial I/O2 input set up time | 400 | | | ns |
| $t_h(\text{SCLK1--Rx}D1)$ | Serial I/O1 input hold time | 200 | | | ns |
| $t_h(\text{SCLK2--Rx}D2)$ | Serial I/O2 input hold time | 200 | | | ns |

Note: When $f(\phi) = 1$ MHz and bit 6 of address 001A₁₆ or 0032₁₆ is "1" (clock synchronous). Divide this value by four when $f(\phi) = 1$ MHz and bit 6 of address 001A₁₆ or 0032₁₆ is "0" (clock asynchronous).

SWITCHING CHARACTERISTICS 1 ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|----------------------|------------------------------------------|-----------------|-------------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_{wH}(S_{CLK1})$ | Serial I/O1 clock output "H" pulse width | CL = 100 pF | $t_c(S_{CLK1})^{/2-30}$ | | | ns |
| $t_{wH}(S_{CLK2})$ | Serial I/O2 clock output "H" pulse width | | $t_c(S_{CLK2})^{/2-30}$ | | | ns |
| $t_{wL}(S_{CLK1})$ | Serial I/O1 clock output "L" pulse width | | $t_c(S_{CLK1})^{/2-30}$ | | | ns |
| $t_{wL}(S_{CLK2})$ | Serial I/O2 clock output "L" pulse width | | $t_c(S_{CLK2})^{/2-30}$ | | | ns |
| $t_d(S_{CLK1}-TxD1)$ | Serial I/O1 output delay time (Note 1) | | | | 140 | ns |
| $t_d(S_{CLK2}-TxD2)$ | Serial I/O2 output delay time (Note 1) | | | | 140 | ns |
| $t_v(S_{CLK1}-TxD1)$ | Serial I/O1 output valid time (Note 1) | | | -30 | | ns |
| $t_v(S_{CLK2}-TxD2)$ | Serial I/O2 output valid time (Note 1) | | | -30 | | ns |
| $t_r(S_{CLK1})$ | Serial I/O1 clock output rise time | | | | 30 | ns |
| $t_f(S_{CLK1})$ | Serial I/O1 clock output fall time | | | | 30 | ns |
| $t_r(S_{CLK2})$ | Serial I/O2 clock output rise time | | | | 30 | ns |
| $t_f(S_{CLK2})$ | Serial I/O2 clock output fall time | | | | 30 | ns |
| $t_r(CMOS)$ | CMOS output rise time (Note 2) | | | | 10 | ns |
| $t_f(CMOS)$ | CMOS output fall time (Note 2) | | | | 10 | ns |

Notes 1: When bit 4 of the UART control register (address 001B16 or 003316) is "0".
2: XOUT pin is excluded.

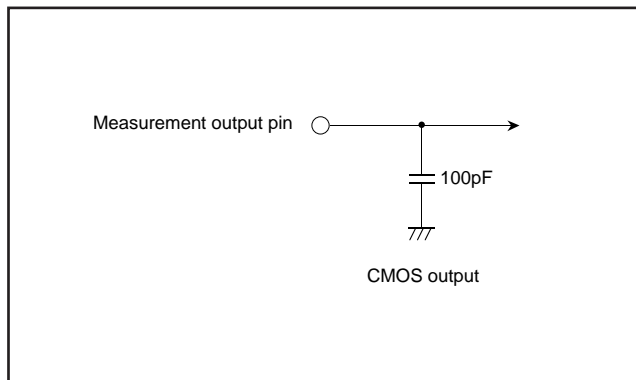


Fig. 34 Circuit for measuring output switching characteristics (1)

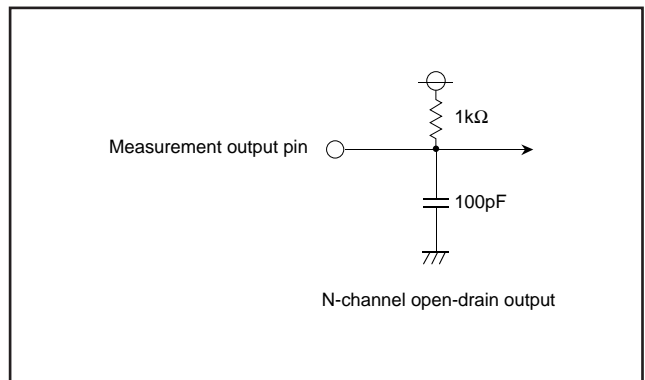


Fig. 35 Circuit for measuring output switching characteristics (2)

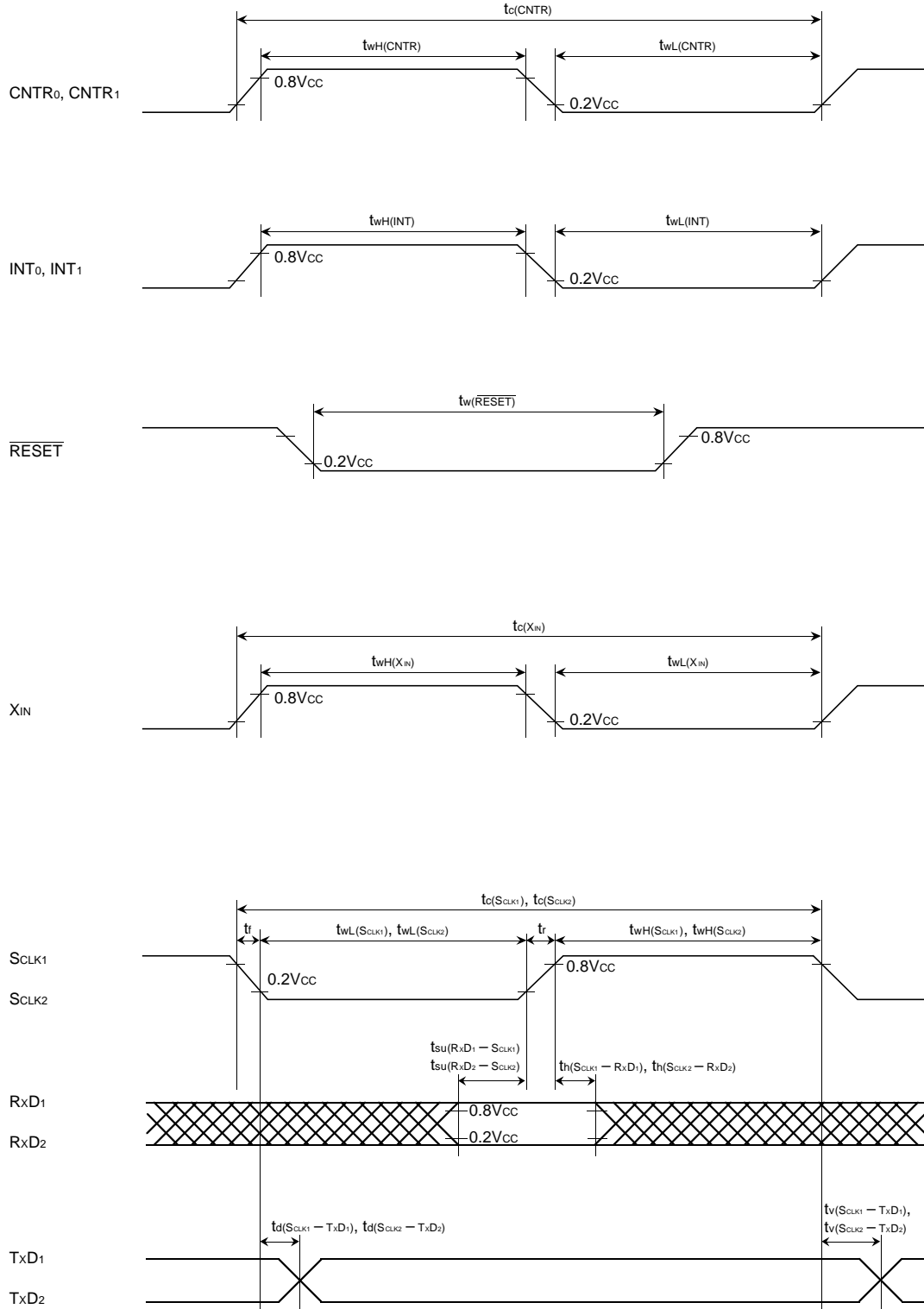
Note: When bit 4 of the UART control register (address 001B16 or 003316) is "1" (N-channel open-drain output), and bit 7 of the serial I/O control register (address 001A16 or 003216) is "1".

SWITCHING CHARACTERISTICS 2 ($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|----------------------|------------------------------------------|-----------------|-------------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_{wH}(S_{CLK1})$ | Serial I/O1 clock output "H" pulse width | CL = 100 pF | $t_c(S_{CLK1})^{/2-50}$ | | | ns |
| $t_{wH}(S_{CLK2})$ | Serial I/O2 clock output "H" pulse width | | $t_c(S_{CLK2})^{/2-50}$ | | | ns |
| $t_{wL}(S_{CLK1})$ | Serial I/O1 clock output "L" pulse width | | $t_c(S_{CLK1})^{/2-50}$ | | | ns |
| $t_{wL}(S_{CLK2})$ | Serial I/O2 clock output "L" pulse width | | $t_c(S_{CLK2})^{/2-50}$ | | | ns |
| $t_d(S_{CLK1}-TxD1)$ | Serial I/O1 output delay time (Note 1) | | | | 350 | ns |
| $t_d(S_{CLK2}-TxD2)$ | Serial I/O2 output delay time (Note 1) | | | | 350 | ns |
| $t_v(S_{CLK1}-TxD1)$ | Serial I/O1 output valid time (Note 1) | | | -30 | | ns |
| $t_v(S_{CLK2}-TxD2)$ | Serial I/O2 output valid time (Note 1) | | | -30 | | ns |
| $t_r(S_{CLK1})$ | Serial I/O1 clock output rise time | | | | 50 | ns |
| $t_f(S_{CLK1})$ | Serial I/O1 clock output fall time | | | | 50 | ns |
| $t_r(S_{CLK2})$ | Serial I/O2 clock output rise time | | | | 50 | ns |
| $t_f(S_{CLK2})$ | Serial I/O2 clock output fall time | | | | 50 | ns |
| $t_r(CMOS)$ | CMOS output rise time (Note 2) | | | | 20 | ns |
| $t_f(CMOS)$ | CMOS output fall time (Note 2) | | | | 20 | ns |

Notes 1: When bit 4 of the UART control register (address 001B16 or 003316) is "0".
2: XOUT pin excluded.

TIMING DIAGRAM



REVISION DESCRIPTION LIST

7510 GROUP DATA SHEET

| Rev. No. | Revision Description | Rev. date |
|----------|----------------------|-----------|
| 1.0 | First Edition | 980110 |
| | | |

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