

**DESCRIPTION**

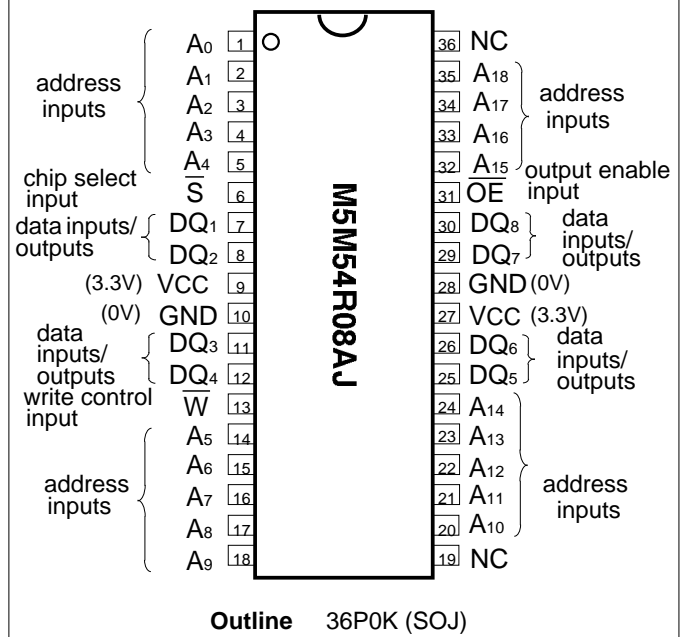
The M5M54R08AJ is a family of 524288-word by 8-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high speed application.

These devices operate on a single 3.3V supply, and are directly TTL compatible. They include a power down feature as well.

**FEATURES**

- Fast access time M5M54R08AJ-10 ... 10ns(max)  
M5M54R08AJ-12 ... 12ns(max)  
M5M54R08AJ-15 ... 15ns(max)
- Single +3.3V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by  $\bar{S}$
- Three-state outputs : OR-tie capability
- $\bar{OE}$  prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

**PIN CONFIGURATION (TOP VIEW)**



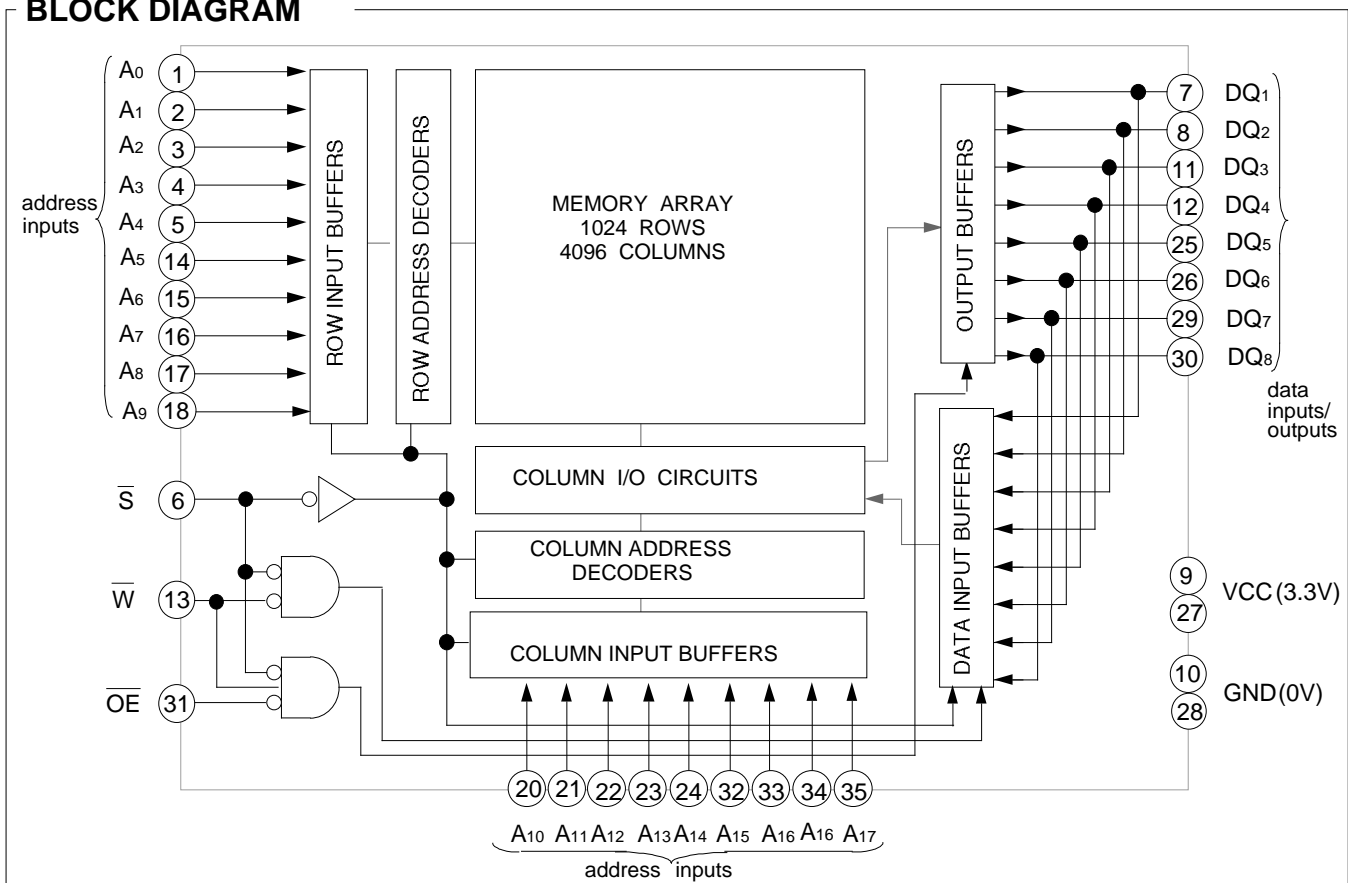
**APPLICATION**

High-speed memory units

**PACKAGE**

M5M54R08AJ : 36pin 400mil SOJ

**BLOCK DIAGRAM**



## FUNCTION

The operation mode of the M5M54R08AJ is determined by a combination of the device control inputs  $\bar{S}$ ,  $\bar{W}$  and  $\bar{OE}$ . Each mode is summarized in the function table.

A write cycle is executed whenever the low level  $\bar{W}$  overlaps with the low level  $\bar{S}$ . The address must be set-up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of  $\bar{W}$  or  $\bar{S}$ , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input  $\bar{OE}$  directly controls the output stage. Setting the  $\bar{OE}$  at a high level, the output stage is in a high impedance state, and the data bus

contention problem in the write cycle is eliminated.

A read cycle is executed by setting  $\bar{W}$  at a high level and  $\bar{OE}$  at a low level while  $\bar{S}$  are in an active state ( $\bar{S}=L$ ).

When setting  $\bar{S}$  at high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by  $\bar{S}$ .

Signal  $\bar{S}$  controls the power-down feature. When  $\bar{S}$  goes high, power dissipation is reduced extremely. The access time from  $\bar{S}$  is equivalent to the address access time.

## FUNCTION TABLE

| $\bar{S}$ | $\bar{W}$ | $\bar{OE}$ | Mode          | DQ             | I <sub>cc</sub> |
|-----------|-----------|------------|---------------|----------------|-----------------|
| H         | X         | X          | Non selection | High-impedance | Stand by        |
| L         | L         | X          | Write         | Din            | Active          |
| L         | H         | L          | Read          | Dout           | Active          |
| L         | H         | H          |               | High-impedance | Active          |

## ABSOLUTE MAXIMUM RATINGS

| Symbol                 | Parameter                 | Conditions           | Ratings                       | Unit |
|------------------------|---------------------------|----------------------|-------------------------------|------|
| V <sub>cc</sub>        | Supply voltage            | With respect to GND  | - 2.0* ~ 4.6                  | V    |
| V <sub>I</sub>         | Input voltage             |                      | - 2.0* ~ V <sub>CC</sub> +0.5 | V    |
| V <sub>O</sub>         | Output voltage            |                      | - 2.0* ~ V <sub>CC</sub>      | V    |
| P <sub>d</sub>         | Power dissipation         | T <sub>a</sub> =25°C | 1000                          | mW   |
| T <sub>opr</sub>       | Operating temperature     |                      | 0 ~ 70                        | °C   |
| T <sub>stg(bias)</sub> | Storage temperature(bias) |                      | - 10 ~ 85                     | °C   |
| T <sub>stg</sub>       | Storage temperature       |                      | - 65 ~ 150                    | °C   |

\* Pulse width\_3ns, In case of DC: - 0.5V

## DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=0 ~ 70°C, V<sub>cc</sub>=3.3V<sup>+10%</sup><sub>-5%</sub>, unless otherwise noted)

| Symbol           | Parameter                         | Condition   | Limits     |            |                      | Unit |    |
|------------------|-----------------------------------|---|------------|------------|----------------------|------|----|
|                  |                                   |   | Min        | Typ        | Max                  |      |    |
| V <sub>IH</sub>  | High-level input voltage          |   | 2.0        |            | V <sub>cc</sub> +0.3 | V    |    |
| V <sub>IL</sub>  | Low-level input voltage           |   |            |            | 0.8                  | V    |    |
| V <sub>OH</sub>  | High-level output voltage         | I <sub>OH</sub> = - 4mA   | 2.4        |            |                      | V    |    |
| V <sub>OL</sub>  | Low-level output voltage          | I <sub>OL</sub> = 8mA   |            |            | 0.4                  | V    |    |
| I <sub>I</sub>   | Input current                     | V <sub>I</sub> = 0 ~ V <sub>cc</sub>  |            |            | 2                    | uA   |    |
| I <sub>OZ</sub>  | Output current in off-state       | V <sub>I</sub> ( $\bar{S}$ )=V <sub>IH</sub><br>V <sub>I/O</sub> = 0 ~ V <sub>cc</sub>  |            |            | 2                    | uA   |    |
| I <sub>CC1</sub> | Active supply current (TTL level) | V <sub>I</sub> ( $\bar{S}$ )=V <sub>IL</sub><br>other inpus=V <sub>IH</sub> or V <sub>IL</sub><br>Output-open(duty 100%)            | AC         | 10ns cycle |                      | 230  | mA |
|                  |                                   |   |            | 12ns cycle |                      | 220  |    |
|                  |                                   |   | 15ns cycle |            | 200                  |      |    |
|                  |                                   |   | DC         |            | 100                  |      |    |
| I <sub>CC2</sub> | Stand by current (TTL level)      | V <sub>I</sub> ( $\bar{S}$ )=V <sub>IH</sub>  | AC         | 10ns cycle |                      | 90   | mA |
|                  |                                   |   |            | 12ns cycle |                      | 70   |    |
|                  |                                   |   | 15ns cycle |            | 60                   |      |    |
|                  |                                   |   | DC         |            | 40                   |      |    |
| I <sub>CC3</sub> | Stand by current                  | V <sub>I</sub> ( $\bar{S}$ )=V <sub>cc</sub> -0.2V<br>other inputs V <sub>I</sub> -0.2V<br>or V <sub>I</sub> -V <sub>cc</sub> -0.2V |            |            | 10                   | mA   |    |

Note 1: Direction for current flowing into an IC is positive (no mark).

**CAPACITANCE** ( $T_a=0\sim 70^\circ\text{C}$ ,  $V_{cc}=3.3\text{V}^{+10\%}_{-5\%}$ , unless otherwise noted)

| Symbol         | Parameter          | Test Condition  | Limit |     |     | Unit |
|----------------|--------------------|---|-------|-----|-----|------|
|                |                    |   | Min   | Typ | Max |      |
| C <sub>i</sub> | Input capacitance  | $V_I = \text{GND}, V_I = 25\text{mVrms}, f = 1\text{MHz}$ |       |     | 7   | pF   |
| C <sub>o</sub> | Output capacitance | $V_O = \text{GND}, V_O = 25\text{mVrms}, f = 1\text{MHz}$ |       |     | 8   | pF   |

Note 2: C<sub>i</sub>, C<sub>o</sub> are periodically sampled and are not 100% tested.

**AC ELECTRICAL CHARACTERISTICS** ( $T_a=0\sim 70^\circ\text{C}$ ,  $V_{cc}=3.3\text{V}^{+10\%}_{-5\%}$ , unless otherwise noted)

**(1) MEASUREMENT CONDITION**

- Input pulse levels .....  $V_{IH}=3.0\text{V}, V_{IL}=0.0\text{V}$
- Input rise and fall time ..... 3ns
- Input timing reference levels .....  $V_{IH}=1.5\text{V}, V_{IL}=1.5\text{V}$
- Output timing reference levels .....  $V_{OH}=1.5\text{V}, V_{OL}=1.5\text{V}$
- Output loads ..... Fig.1, Fig.2

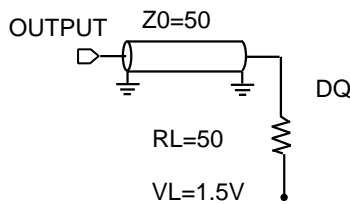


Fig.1 Output load

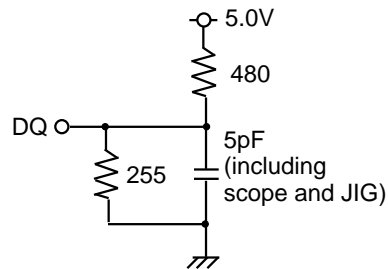


Fig.2 Output load for  $t_{en}, t_{dis}$

**MITSUBISHI LSIs**  
**M5M54R08AJ-10,-12,-15**

**4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM**

**(2)READ CYCLE**

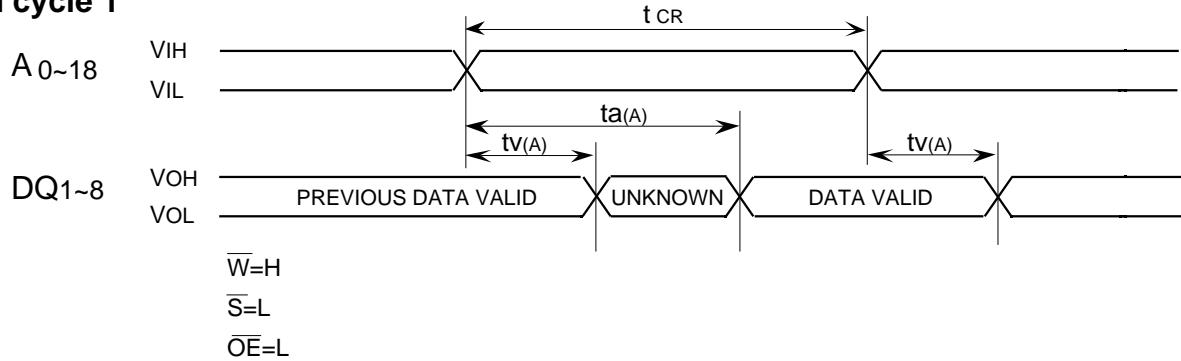
| Symbol               | Parameter                                      | Limits        |     |               |     |               |     | Unit |
|----------------------|--|---------------|-----|---------------|-----|---------------|-----|------|
|                      |  | M5M54R08AJ-10 |     | M5M54R08AJ-12 |     | M5M54R08AJ-15 |     |      |
|                      |  | Min           | Max | Min           | Max | Min           | Max |      |
| t <sub>CR</sub>      | Read cycle time                                | 10            |     | 12            |     | 15            |     | ns   |
| t <sub>a(A)</sub>    | Address access time                            |               | 10  |               | 12  |               | 15  | ns   |
| t <sub>a(S)</sub>    | Chip select access time                        |               | 10  |               | 12  |               | 15  | ns   |
| t <sub>a(OE)</sub>   | Output enable access time                      |               | 5   |               | 6   |               | 7   | ns   |
| t <sub>dis(S)</sub>  | Output disable time after $\overline{S}$ high  | 0             | 5   | 0             | 6   | 0             | 7   | ns   |
| t <sub>dis(OE)</sub> | Output disable time after $\overline{OE}$ high | 0             | 5   | 0             | 6   | 0             | 7   | ns   |
| t <sub>en(S)</sub>   | Output enable time after $\overline{S}$ low    | 2             |     | 3             |     | 3             |     | ns   |
| t <sub>en(OE)</sub>  | Output enable time after $\overline{OE}$ low   | 0             |     | 1             |     | 1             |     | ns   |
| t <sub>v(A)</sub>    | Data valid time after address change           | 2             |     | 3             |     | 3             |     | ns   |
| t <sub>PU</sub>      | Power-up time after chip selection             | 0             |     | 0             |     | 0             |     | ns   |
| t <sub>PD</sub>      | Power-down time after chip selection           |               | 10  |               | 12  |               | 15  | ns   |

**(3)WRITE CYCLE**

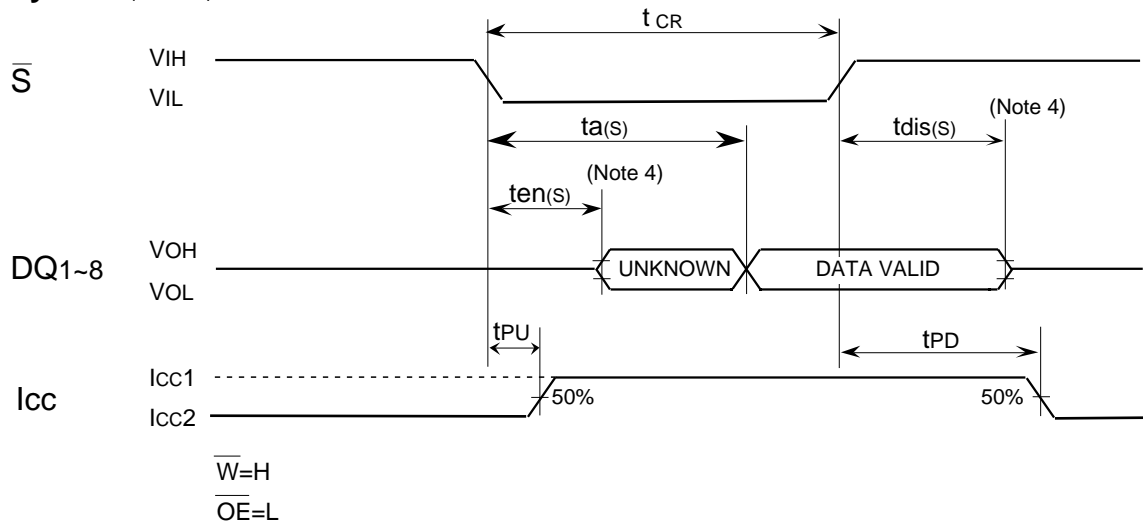
| Symbol                                       | Parameter                                      | Limits        |     |               |     |               |     | Unit |
|--|--|---------------|-----|---------------|-----|---------------|-----|------|
|  |  | M5M54R08AJ-10 |     | M5M54R08AJ-12 |     | M5M54R08AJ-15 |     |      |
|  |  | Min           | Max | Min           | Max | Min           | Max |      |
| t <sub>CW</sub>                              | Write cycle time                               | 10            |     | 12            |     | 15            |     | ns   |
| t <sub>w(W)</sub>                            | Write pulse width ( $\overline{OE}$ low)       | 10            |     | 12            |     | 15            |     | ns   |
| t <sub>w(W)</sub>                            | Write pulse width ( $\overline{OE}$ high)      | 8             |     | 10            |     | 10            |     | ns   |
| t <sub>su(A)1</sub>                          | Address setup time ( $\overline{W}$ )          | 0             |     | 0             |     | 0             |     | ns   |
| t <sub>su(A)2</sub>                          | Address setup time ( $\overline{S}$ )          | 0             |     | 0             |     | 0             |     | ns   |
| t <sub>su(S)</sub>                           | Chip select setup time                         | 8             |     | 10            |     | 10            |     | ns   |
| t <sub>su(D)</sub>                           | Data setup time                                | 5             |     | 6             |     | 7             |     | ns   |
| t <sub>h(D)</sub>                            | Data hold time                                 | 0             |     | 0             |     | 0             |     | ns   |
| t <sub>rec(W)</sub>                          | Write recovery time                            | 1             |     | 1             |     | 1             |     | ns   |
| t <sub>dis(W)</sub>                          | Output disable time after $\overline{W}$ low   | 0             | 5   | 0             | 6   | 0             | 7   | ns   |
| t <sub>dis(OE)</sub>                         | Output disable time after $\overline{OE}$ high | 0             | 5   | 0             | 6   | 0             | 7   | ns   |
| t <sub>en(W)</sub>                           | Output enable time after $\overline{W}$ high   | 0             |     | 0             |     | 0             |     | ns   |
| t <sub>en(OE)</sub>                          | Output enable time after $\overline{OE}$ low   | 0             |     | 0             |     | 0             |     | ns   |
| t <sub>su(A-<math>\overline{W}</math>)</sub> | Address to $\overline{W}$ High                 | 8             |     | 10            |     | 10            |     | ns   |

**(4)TIMING DIAGRAMS**

**Read cycle 1**



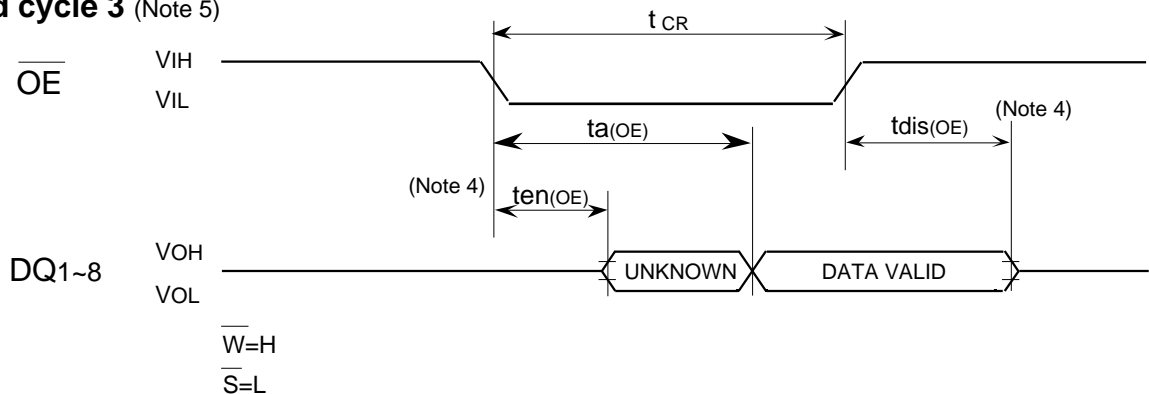
**Read cycle 2 (Note 3)**



Note 3. Addresses valid prior to or coincident with  $\bar{S}$  transition low.

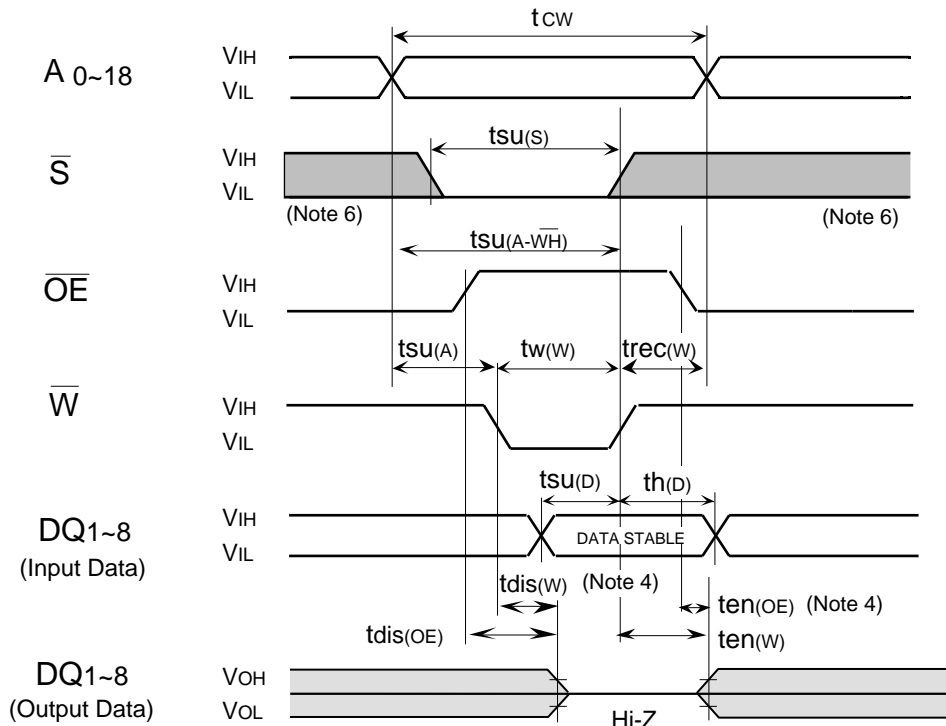
4. Transition is measured  $\pm 500\text{mv}$  from steady state voltage with specified loading in Figure 2.

**Read cycle 3 (Note 5)**

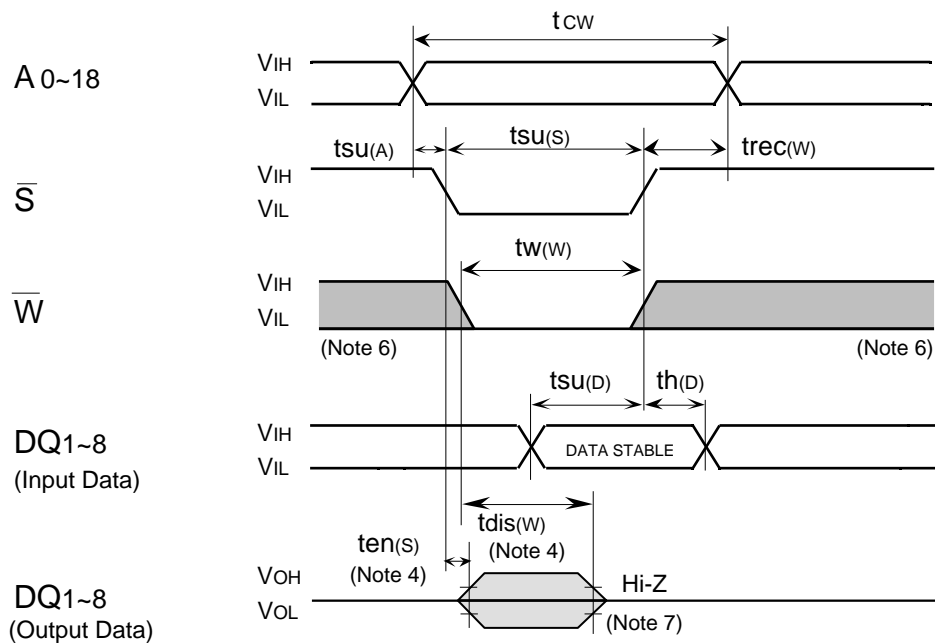


Note 5. Addresses and  $\bar{S}$  valid prior to  $\bar{OE}$  transition low by  $(ta(A)-ta(OE))$ ,  $(ta(S)-ta(OE))$

**Write cycle ( $\overline{W}$  control mode)**



**Write cycle ( $\overline{S}$  control)**



Note 6: Hatching indicates the state is don't care.

7: When the falling edge of  $\overline{W}$  is simultaneous or prior to the falling edge of  $\overline{S}$ , the output is maintained in the high impedance.

8:  $t_{en}, t_{dis}$  are periodically sampled and are not 100% tested.