

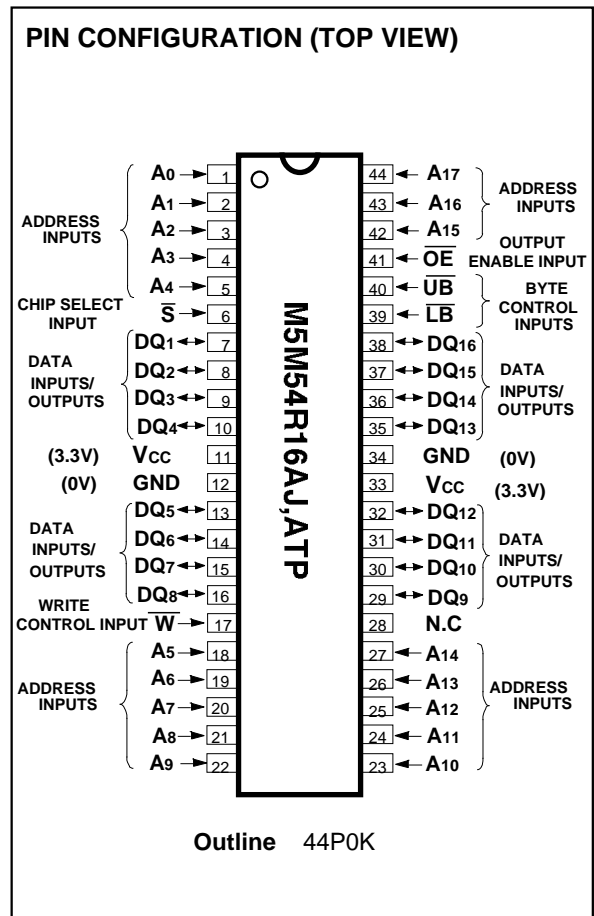
DESCRIPTION

The M5M54R16A is a family of 262144-word by 16-bit static RAMs, fabricated with the high performance CMOS process and designed for high speed application. These devices operate on a single 3.3V supply, and are directly TTL compatible.

They include a power down feature as well. In write and read cycles, the lower and upper bytes are able to be controlled either together or separately by \overline{LB} and \overline{UB} .

FEATURES

- Fast access time M5M54R16AJ,ATP-10 ... 10ns(max)
 M5M54R16AJ,ATP-12 ... 12ns(max)
 M5M54R16AJ,ATP-15 ... 15ns(max)
- Single +3.3V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by \overline{S}
- Three-state outputs : OR-tie capability
- OE prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs
- Separate control of lower and upper bytes by \overline{LB} and \overline{UB}



APPLICATION

High-speed memory system

FUNCTION

The operation mode of the M5M54R16A is determined by a combination of the device control inputs \overline{S} , \overline{W} , \overline{OE} , \overline{LB} , and \overline{UB} . Each mode is summarized in the function table.

A write cycle is executed whenever the low level \overline{W} overlaps with low level \overline{LB} and/or low level \overline{UB} and low level \overline{S} . The address must be set-up before write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of \overline{W} , \overline{LB} , \overline{UB} or \overline{S} , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while \overline{LB} and/or \overline{UB} and \overline{S} are in an active

PACKAGE

- M5M54R16AJ 44pin 400mil SOJ
- M5M54R16ATP 44pin 400mil TSOP(II)

state. (\overline{LB} and/or \overline{UB} =L, \overline{S} =L)

When setting \overline{LB} at a high level and other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enable, and lower-Byte are in a non-selectable mode. And when setting \overline{UB} at a high level and other pins are in an active state, lower-Byte are in a selectable mode in which both reading and writing are enable, and upper-Byte are in a non-selectable mode.

When setting \overline{LB} and \overline{UB} at a high level or \overline{S} at high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \overline{LB} , \overline{UB} and \overline{S} .

Signal- \overline{S} controls the power-down feature. When \overline{S} goes high, power dissipation is reduced extremely. The access time from \overline{S} is equivalent to the address access time.

MITSUBISHI LSIs

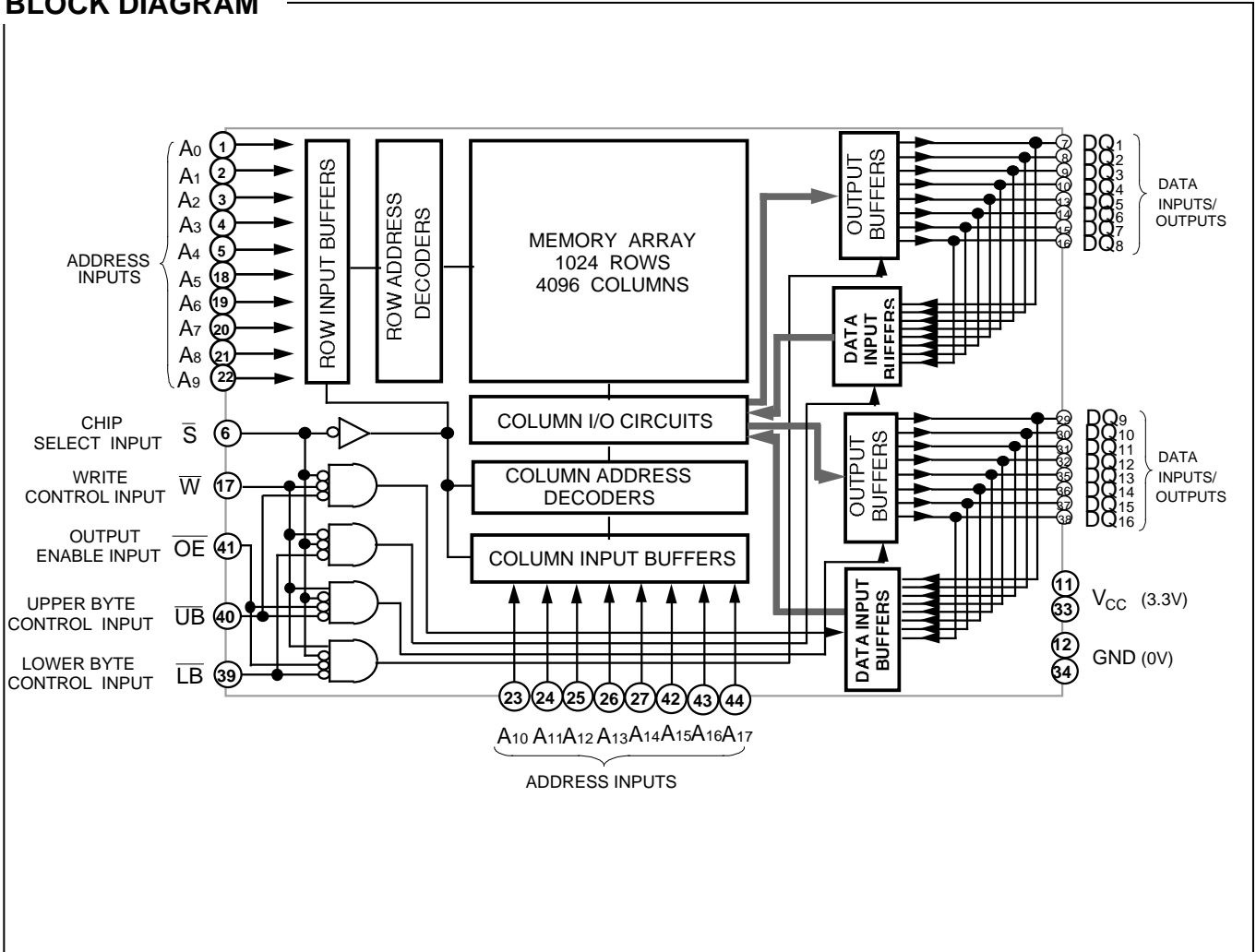
M5M54R16AJ, ATP-10, -12, -15

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

FUNCTION TABLE

S	\overline{W}	OE	\overline{LB}	UB	Mode	DQ1~8	DQ9~16	I _{cc}
L	H	L	L	L	Read cycle All Bytes	D _{OUT}	D _{OUT}	Active
L	H	L	H	L	Read cycle Upper Bytes	High-impedance	D _{OUT}	Active
L	H	L	L	H	Read cycle Lower Bytes	D _{OUT}	High-impedance	Active
L	L	X	L	L	Write cycle All Bytes	D _{IN}	D _{IN}	Active
L	L	X	H	L	Write cycle Upper Bytes	High-impedance	D _{IN}	Active
L	L	X	L	H	Write cycle Lower Bytes	D _{IN}	High-impedance	Active
L	H	H	X	X	Output disable	High-impedance	High-impedance	Active
L	X	X	H	H				
H	X	X	X	X	Non selection	High-impedance	High-impedance	Stand by

BLOCK DIAGRAM



MITSUBISHI LSIs

M5M54R16AJ,ATP-10,-12,-15

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		- 2.0* ~ 4.6	V
V _I	Input voltage	With respect to GND	- 2.0* ~ V _{CC} +0.5	V
V _O	Output voltage		- 2.0* ~ V _{CC}	V
P _d	Power dissipation		T _a =25°C	1000
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg(bias)}	Storage temperature(bias)		- 10 ~ 85	°C
T _{stg}	Storage temperature		- 65 ~ 150	°C

*Pulse width ≤ 3 ns, In case of DC: - 0.5V

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=3.3V ^{+10%} _{-5%}, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.0		V _{CC} +0.3	V
V _{IL}	Low-level input voltage				0.8	V
V _{OH}	High-level output voltage	I _{OH} = - 4mA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8mA			0.4	V
I _I	Input current	V _I = 0 ~ V _{CC}			2	µA
I _{OZ}	Output current in off-state	V _I (\bar{s}) = V _{IH} V _O = 0 ~ V _{CC}			2	µA
I _{CC1}	Active supply current (TTL level)	V _I (\bar{s}) = V _{IL} other inputs V _{IH} or V _{IL} Output-open(duty 100%)	AC(10ns cycle)		260	mA
			AC(12ns cycle)		250	
			AC(15ns cycle)		230	
			DC		120	
I _{CC2}	Stand-by supply current (TTL level)	V _I (\bar{s}) = V _{IH}	AC(10ns cycle)		90	mA
			AC(12ns cycle)		70	
			AC(15ns cycle)		60	
			DC		40	
I _{CC3}	Stand-by current (MOS level)	V _I (\bar{s}) = V _{CC} - 0.2V other inputs V _I 0.2V or V _I V _{CC} - 0.2V			10	mA

Note 1: Direction for current flowing into an IC is positive (no mark).

CAPACITANCE (T_a=0~70°C, V_{CC}=3.3V ^{+10%} _{-5%}, unless otherwise noted)

Symbol	Parameter	Test Condition	Limit			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _i =25mVrms, f=1MHz			7	pF
C _O	Output capacitance	V _O =GND, V _o =25mVrms, f=1MHz			8	pF

Note 2: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (T_a= 0~70 °C, V_{CC}=3.3V ^{+10%} _{-5%}, unless otherwise noted)

(1) MEASUREMENT CONDITION

Input pulse levels V_{IH}=3.0V, V_{IL}=0.0V
 Input rise and fall time 3ns
 Input timing reference levels V_{IH}=1.5V, V_{IL}=1.5V
 Output timing reference levels V_{OH}=1.5V, V_{OL}=1.5V
 Output loads Fig1, Fig2

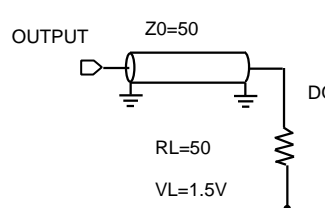


Fig.1 Output load

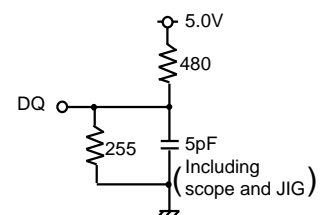


Fig.2 Output load for t_{en}, t_{dis}

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READ CYCLE

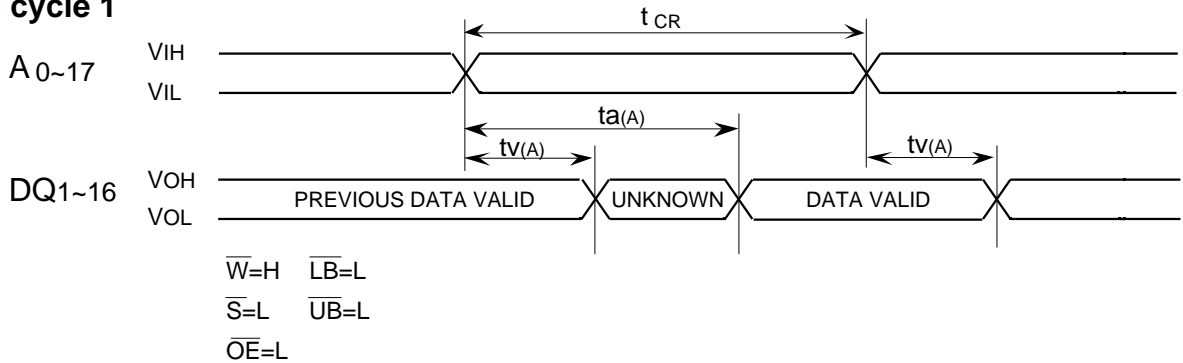
Symbol	Parameter	Limits						Unit
		M5M54R16AJ,ATP-10		M5M54R16AJ,ATP-12		M5M54R16AJ,ATP-15		
		Min	Max	Min	Max	Min	Max	
t _{CR}	Read cycle time	10		12		15		ns
t _{a(A)}	Address access time		10		12		15	ns
t _{a(S)}	Chip select access time		10		12		15	ns
t _{a(OE)}	Output enable access time		5		6		7	ns
t _{a(B)}	LB,UB access time		5		6		7	ns
t _{dis(S)}	Output disable time after \overline{S} high	0	5	0	6	0	7	ns
t _{dis(OE)}	Output disable time after \overline{OE} high	0	5	0	6	0	7	ns
t _{dis(B)}	Output disable time after $\overline{LB},\overline{UB}$ high	0	5	0	6	0	7	ns
t _{en(S)}	Output enable time after \overline{S} low	2		3		3		ns
t _{en(OE)}	Output enable time after \overline{OE} low	0		1		1		ns
t _{en(B)}	Output enable time after $\overline{LB},\overline{UB}$ low	0		1		1		ns
t _{v(A)}	Data valid time after address change	2		3		3		ns
t _{PU}	Power-up time after chip selection	0		0		0		ns
t _{PD}	Power-down time after chip selection		10		12		15	ns

Write cycle

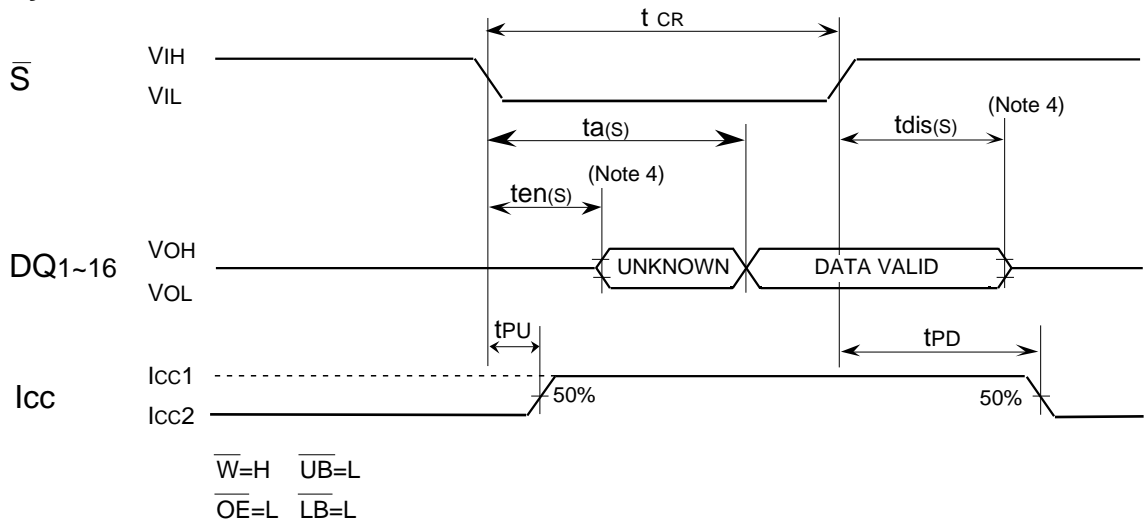
Symbol	Parameter	Limits						Unit
		M5M54R16AJ,ATP-10		M5M54R16AJ,ATP-12		M5M54R16AJ,ATP-15		
		Min	Max	Min	Max	Min	Max	
t _{cw}	Write cycle time	10		12		15		ns
t _{w(W)}	Write pulse width (\overline{OE} low)	10		12		15		ns
t _{w(W)}	Write pulse width (\overline{OE} high)	8		10		10		ns
t _{su(B)}	LB,UB setup time	8		10		10		ns
t _{su(A)1}	Address setup time (\overline{W})	0		0		0		ns
t _{su(A)2}	Address setup time (\overline{S})	0		0		0		ns
t _{su(S)}	Chip select setup time	8		10		10		ns
t _{su(D)}	Data setup time	5		6		7		ns
t _{h(D)}	Data hold time	0		0		0		ns
t _{rec(W)}	Write recovery time	1		1		1		ns
t _{dis(W)}	Output disable time after \overline{W} low	0	5	0	6	0	7	ns
t _{dis(OE)}	Output disable time after \overline{OE} high	0	5	0	6	0	7	ns
t _{en(W)}	Output enable time after \overline{W} high	0		0		0		ns
t _{en(OE)}	Output enable time after \overline{OE} low	0		0		0		ns
t _{en(B)}	Output enable time after $\overline{LB},\overline{UB}$ low	0		0		0		ns
t _{su(A-\overline{WH})}	Address to \overline{W} High	8		10		10		ns
t _{su(A-\overline{SH})}	Address to \overline{S} High	8		10		10		ns
t _{su(A-\overline{BH})}	Address to $\overline{LB},\overline{UB}$ High	8		10		10		ns

(4)TIMING DIAGRAMS

Read cycle 1



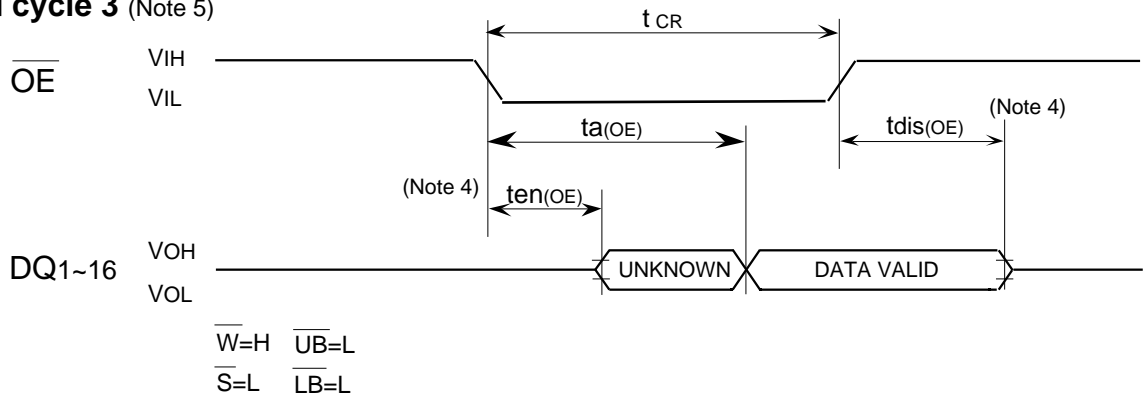
Read cycle 2 (Note 3)



Note 3. Addresses valid prior to or coincident with \overline{S} transition low.

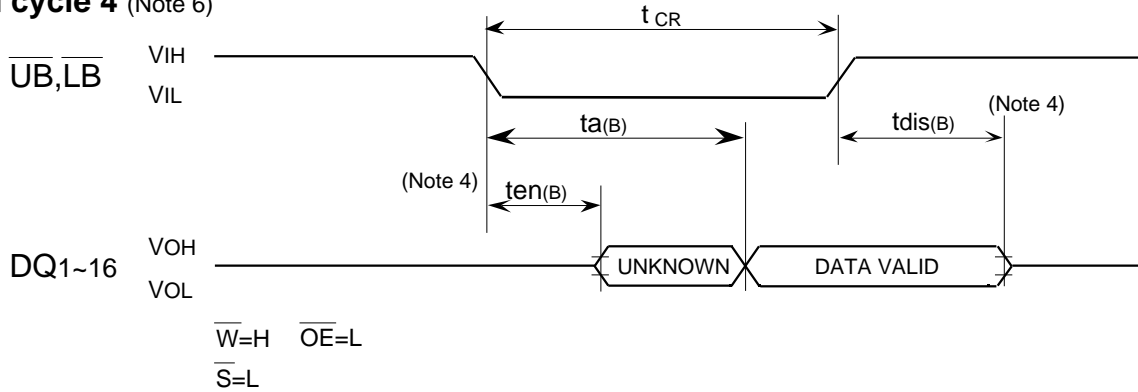
4. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 5)



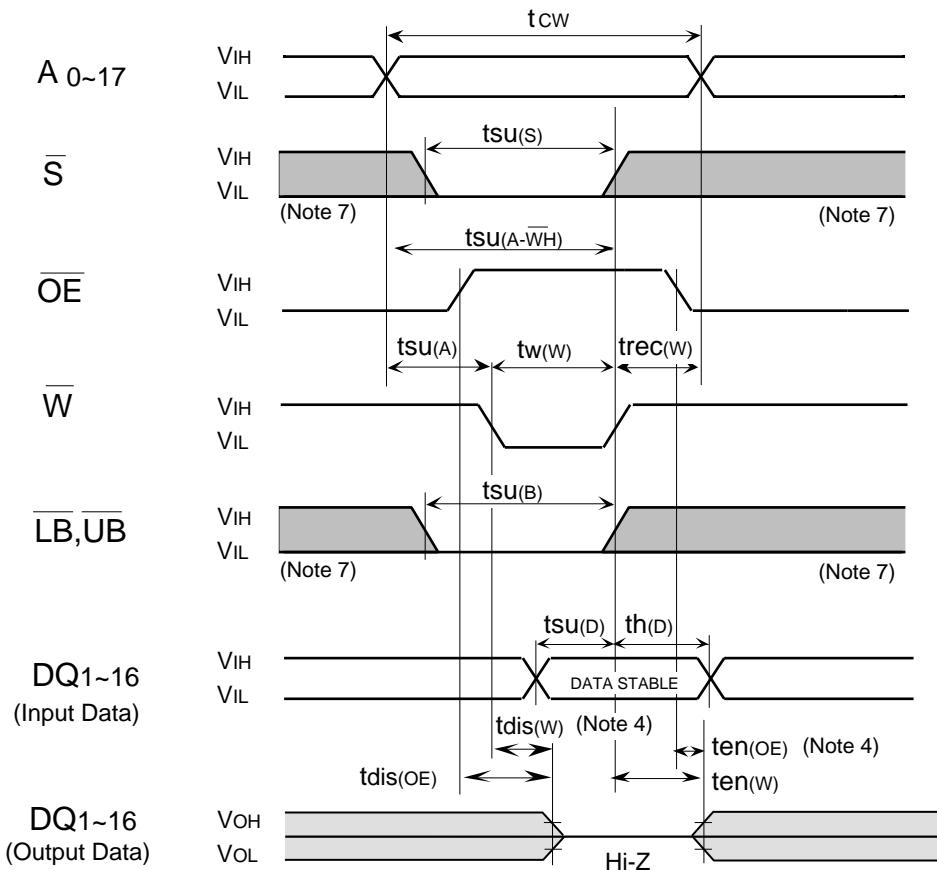
Note 5. Addresses and \overline{S} valid prior to \overline{OE} transition low by $(t_{a(A)}-t_{a(OE)})$, $(t_{a(S)}-t_{a(OE)})$

Read cycle 4 (Note 6)



Note 6. Addresses, \overline{S} and \overline{OE} valid prior to $\overline{LB}, \overline{UB}$ transition low by $(t_{a(A)}-t_{a(B)})$, $(t_{a(S)}-t_{a(B)})$, $(t_{a(OE)}-t_{a(B)})$.

Write cycle (\overline{W} control mode)

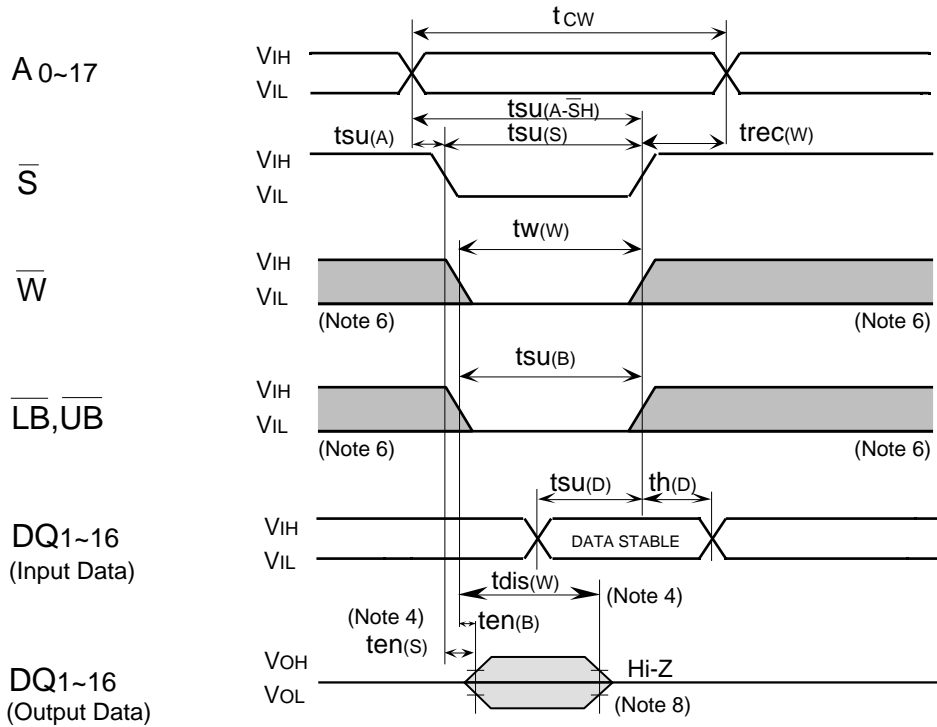


Note 7: Hatching indicates the state is don't care.

8: When the falling edge of \overline{W} is simultaneous or prior to the falling edge of \overline{S} , the output is maintained in the high impedance.

9: t_{en}, t_{dis} are periodically sampled and are not 100% tested.

Write cycle(\overline{S} control)



Write cycle($\overline{LB}, \overline{UB}$ control)

