NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC8100GR

SILICON UP/DOWN CONVERTERS IC
FOR 800 MHz to 900 MHz MOBILE COMMUNICATIONS

DESCRIPTION

μPC8100GR is a silicon monolithic integrated circuit designed as up/down converters for 800 MHz to 900 MHz mobile communications, mainly CT2. This IC consists of upconverter and downconverter, which are packaged in 20 pin SSOP. Quadrature modulator IC (μPC8101GR) is also available as for kit-use with this IC. So, these pair devices contribute to make RF block small, high-performance and low power-consumption.

This product is manufactured using NEC's 20 GHz f_T NESAT™III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion and migration. Thus, this product has excellent performance, uniformity and reliability.

FEATURES

- Operating frequency – f_{RF} = 800 MHz to 900 MHz, f_{IF} = 50 MHz to 150 MHz, f_{LO} = 650 MHz to 1 050 MHz
- Upconverter and downconverter are integrated in 1 chip.
- 20 pin SSOP suitable for high-density surface mounting.
- Wide operating voltage V_{CC} = 2.7 to 4.5 V
- Equipped with Power Save Function.
- Excellent linearity

APPLICATIONS

- Typical application – Digital cordless phone CT2.
- Further application – Digital cellular, etc.

ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μPC8100GR-E2	20 pin plastic SSOP (225 mil)	Embossed tape 12 mm wide. QTY 2.5 kp/Reel. Pin 1 indicates roll-in direction of tape.

Remark To order evaluation samples, please contact your local NEC sales office. (Order number: μPC8100GR)

Caution electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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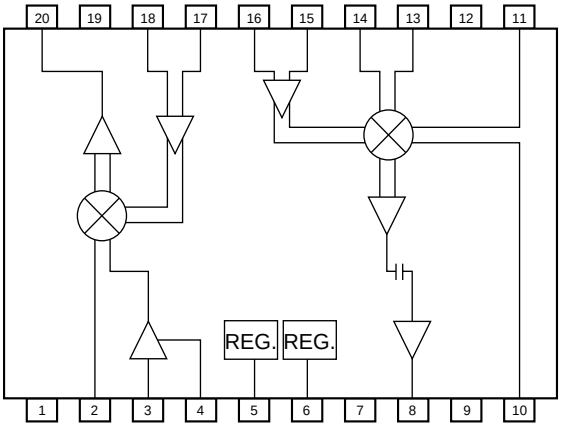
Printed in Japan

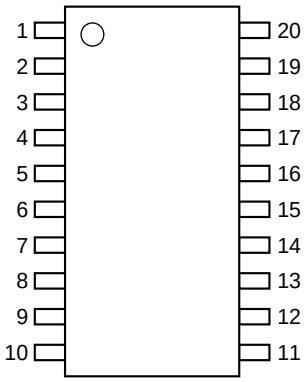
The mark ★ shows major revised points.

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS

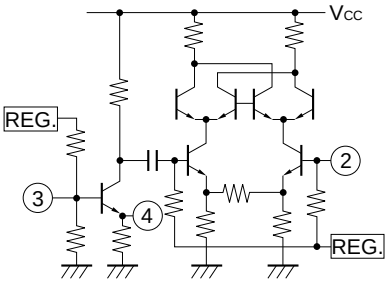
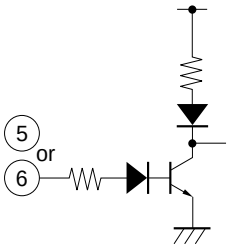
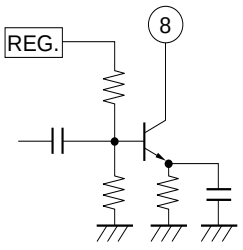


1. GND
2. RF BYPASS
3. RF INPUT
4. PEAKING OUT
5. P/S (for DOWN CONV.)
6. P/S (for UP CONV.)
7. V_{CC} (for UP CONV.)
8. RF OUTPUT
9. GND
10. MIX OUTPUT1
11. MIX OUTPUT2
12. GND
13. IF BYPASS
14. IF INPUT
15. OSC INPUT (for UP CONV.)
16. OSC BYPASS (for UP CONV.)
17. OSC BYPASS (for DOWN CONV.)
18. OSC INPUT (for DOWN CONV.)
19. V_{CC} (for DOWN CONV.)
20. IF OUTPUT

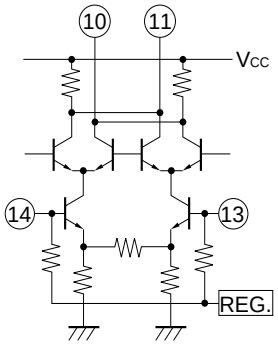
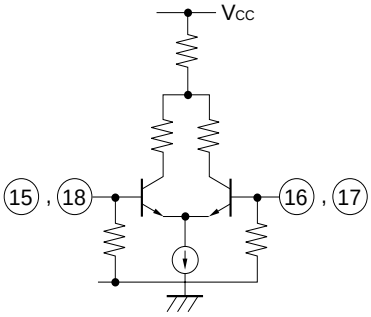
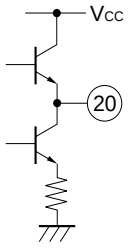
(Top View)



PIN EXPLANATION

<table>
<tr><th>PIN NO.</th><th>ASSIGNMENT</th><th>APPLIED VOLTAGE (V)</th><th>PIN VOLTAGE (V)</th><th>FUNCTION AND APPLICATION</th><th>EQUIVALENT CIRCUIT</th></tr>
<tr><td>1</td><td>GND</td><td>0.0</td><td>–</td><td>Ground for downconverter.
Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible.
(Track length should be kept as short as possible.)</td><td></td></tr>
<tr><td>2</td><td>RF bypass</td><td>–</td><td>1.1</td><td>Bypass of RF input for downconverter.</td><td rowspan="3"> 
</td></tr>
<tr><td>3</td><td>RF input</td><td>–</td><td>0.9</td><td>This pin is RF input for downconverter designed as double balanced mixer. This high-impedance input should be matched with external chip inductor. (eg 4.7 nH).</td></tr>
<tr><td>4</td><td>Peaking out</td><td>–</td><td>0.12</td><td>Open emitter pin of low noise amplifier. Grounded with capacitor (eg 3 pF) and register (eg 22 Ω) serially.</td></tr>
<tr><td>5</td><td>Power-save pin for downconverter</td><td>0 to 4.5</td><td>–</td><td>This pin can control downconverter's ON/OFF operation with bias as follows;
<table><tr><th></th><th>Bias: V</th><th>Operation</th></tr><tr><td rowspan="2">VPS</td><td>≥1.8</td><td>ON</td></tr><tr><td>0 to 1.0</td><td>OFF</td></tr></table></td><td rowspan="2"> 
</td></tr>
<tr><td>6</td><td>Power-save pin for upconverter</td><td>0 to 4.5</td><td>–</td><td>This pin can control upconverter's ON/OFF operation with bias as follows;
<table><tr><th></th><th>Bias: V</th><th>Operation</th></tr><tr><td rowspan="2">VPS</td><td>≥1.8</td><td>ON</td></tr><tr><td>0 to 1.0</td><td>OFF</td></tr></table></td></tr>
<tr><td>7</td><td>Vcc for upconverter</td><td>2.7 to 4.5</td><td>–</td><td>Supply voltage for upconverter.
Must be connected bypass capacitor (e.g 1 000 pF) to minimize ground impedance.</td><td rowspan="3"> 
</td></tr>
<tr><td>8</td><td>RF output</td><td>same as Vcc through intactor</td><td>–</td><td>F output from upconverter.
Connect the Vcc through inductor (eg 15 nH).</td></tr>
<tr><td>9</td><td>GND</td><td>0.0</td><td>–</td><td>Ground for RF amplifier of upconverter.</td></tr>
</table>

PIN EXPLANATION

PIN NO.	ASSIGNMENT	PIN VOLTAGE (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
10	MIX OUT 1	2.3	Mixer output from upconverter.	
11	MIX OUT 2	2.3	Mixer output from upconverter. (10) and (11) pins should be externally equipped with tank circuit of inductor (eg 4.7 nH) and capacitor (eg 3.5 pF).	
12	GND	0*	Ground for oscillator buffer amplifier and mixer of upconverter. Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. (Track length should be kept as short as possible.)	
13	IF bypass	1.03	Bypass of IF input for upconverter.	
14	IF input	1.03	This pin is IF input for upconverter designed as double balanced mixer. This high-impedance input should be externally equipped with matching circuit of inductor (eg 220 nH) and capacitor (eg 1.5 pF).	
15	OSC input (for upconverter)	1.8	Local oscillator input for upconverter. Required for matching with register 51 Ω.	
16	OSC bypass (for upconverter)	1.8	Bypass of local oscillator input for upconverter.	
17	OSC bypass (for down-converter)	1.85	Bypass of local oscillator input for downconverter.	
18	OSC input (for down-converter)	1.85	Local oscillator input for down-converter. Required for matching with register 51 Ω.	
19	VCC supply for for down-converter	2.7 to 4.5*	Supply voltage for downconverter. It must be connected bypass capacitor (e.g 1 000 pF) to minimize ground impedance.	
20	IF output	1.45	IF output from downconverter.	

***** Externally supply voltage

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	T_A = +25 °C	5.0	V
Power Dissipation of package allowance	P_D	Mounted on 50 × 50 × 1.6 mm double copper clad epoxy glass board at T_A = +70 °C	530	mW
Operating Temperature	T_{opt}		–20 to +70	°C
Storage Temperature	T_{stg}		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	2.7	3.0	4.5	V
Operating Temperature	T_{opt}	–20	+25	+70	°C

ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = 2.7 V, Z_L = Z_S = 50 Ω, unless otherwise specified; $V_{P/S}$ ≥ 1.8 V)

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
UPCONVERTER BLOCK*1						
Circuit current	I_{CC}	13.0	25.0	35.0	mA	No input signal
Conversion gain	CG	17.5	20.5	25.5	dB	P_{IFin} = –40 dBm
RF output level	P_{RFout}	0	3		dBm	P_{IFin} = –10 dBm, 50 Ω load
Noise figure	NF		13	18	dB	DSB mode
Local leakage at RF_{out}	Lo_{rf}		–25.0	–10.0	dBm	P_{IFin} = –10 dBm
IF leakage at RF_{out}	IF_{rf}		–12.0	–5.0	dBm	P_{IFin} = –10 dBm
Circuit current in power-save mode*3	I_{CC}(P/S)		220	350	μA	6PIN(P/S) ≤ 1.0 V
Power-save control voltage	$V_{P/S}$(ON)	1.8		4.5	V	
	$V_{P/S}$(OFF)			1.0	V	
Rise up time	T_{up}		2.5	5.0	μs	
DOWNCONVERTER BLOCK*2						
Circuit current	I_{CC}	8.0	15.0	22.0	mA	No input signal
Conversion gain	CG	15.0	18.0	23.0	dB	P_{RFin} = –40 dBm
IF output level	P_{IFout}	–4.5	–2.0		dBm	P_{RFin} = –10 dBm, 50 Ω load
3rd order intermodulation distortion	IM3	–45.0	–49.0		dBc	$f_{RFin}1$ = 866.4 MHz, $P_{RFin}1$ = –40 dBm $f_{RFin}2$ = 866.8 MHz, $P_{RFin}2$ = –40 dBm
Noise figure	NF		7.5	10	dB	DSB mode
Circuit current in power-save mode*3	I_{CC}(P/S)		220	350	μA	5PIN(P/S) ≤ 1.0 V
Power-save control voltage	$V_{P/S}$(ON)	1.8		4.5	V	
	$V_{P/S}$(OFF)			1.0	V	
Rise up time	T_{up}		2.5	5.0	μs	

*1 : f_{IFin} = 150.05 MHz, f_{RFout} = 864.05 to 868.05 MHz
f_{Loin} = 1014.10 to 1018.1 MHz (–9 dBm)

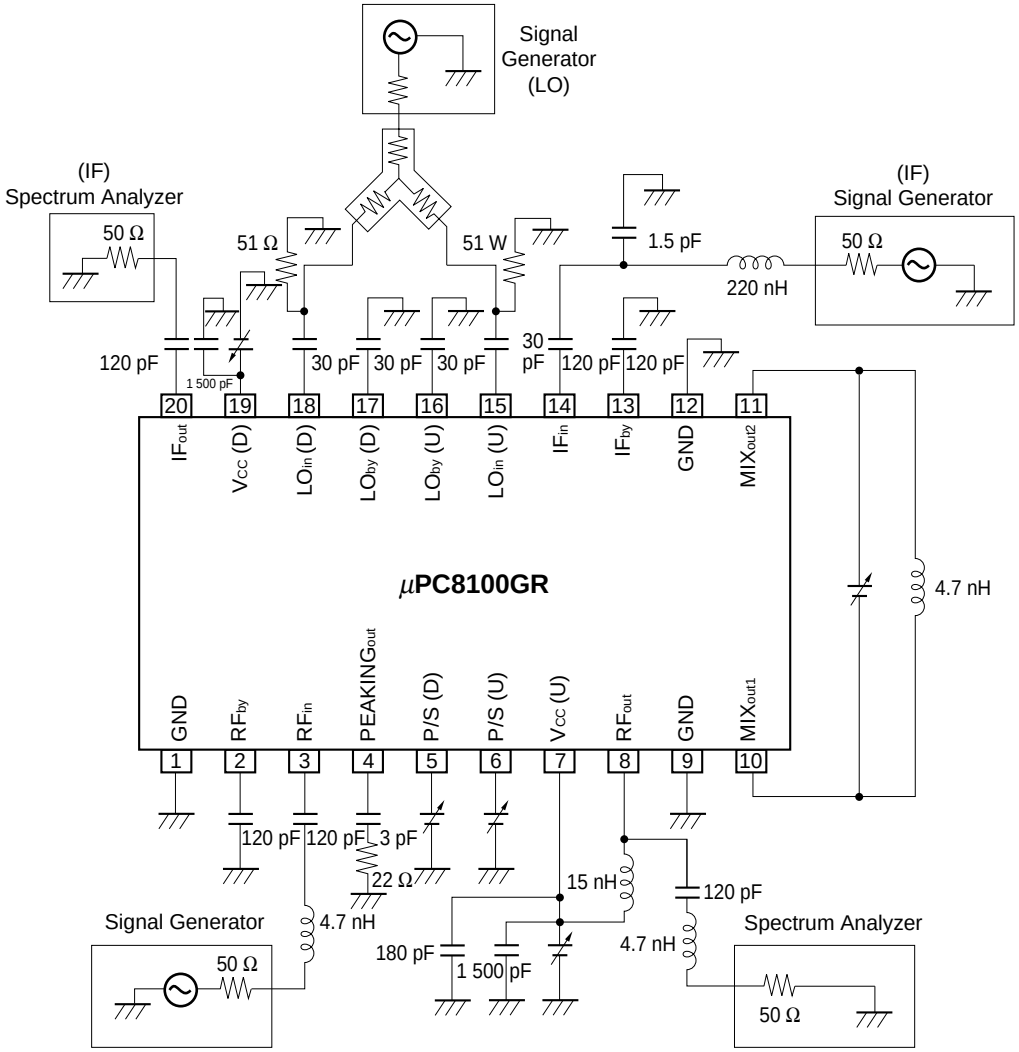
*2 : f_{RFin} = 864.05 to 868.05 MHz, f_{IFout} = 150.05 MHz
f_{Loin} = 1014.10 to 1018.1 MHz (–9 dBm)

*3 : Circuit current in power-save mode is total value of upconverter+downconverter

STANDARD CHARACTERISTIC FOR REFERENCE (T_A = 25 °C, V_{CC} = 2.7 V, Z_L = Z_S = 50 Ω, unless otherwise specified; $V_{P/S}$ ≥ 1.8 V)

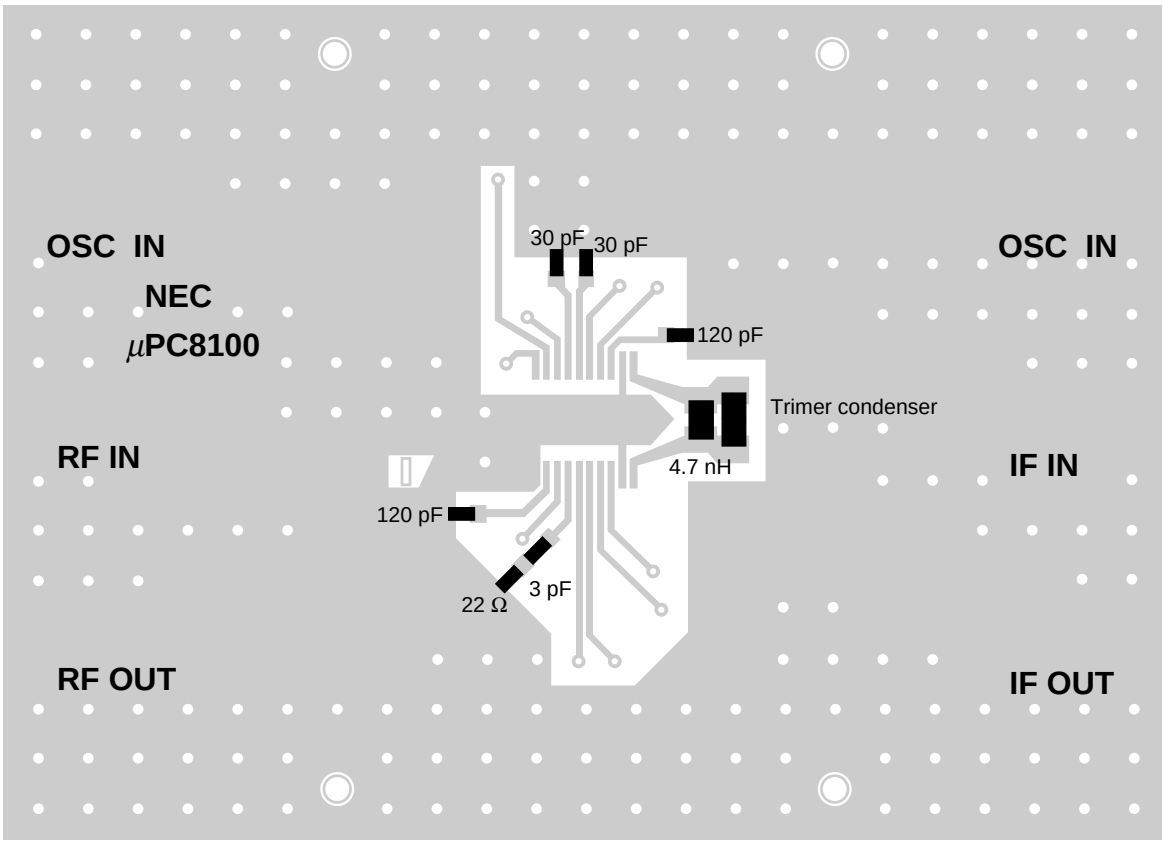
PARAMETERS	SYMBOL	REFERENCE	UNIT	TEST CONDITIONS
UPCONVERTER BLOCK				
3rd order intermodulation distortion	IM3	–39.0	dBc	$f_{IFin}1$ = 150.4 MHz, $P_{IF}1$ = –30 dBm $f_{IFin}2$ = 150.8 MHz, $P_{IF}2$ = –30 dBm
DOWNCONVERTER BLOCK				
IF output 1 dB compression	P_{1dB}	–7.0	dBm	
Local leakage at IF_{out} Pin	Lo_{if}	–29.0	dBm	P_{in} = –40 dBm
RF leakage at IF_{out} Pin	RF_{if}	–44.0	dBm	P_{in} = –40 dBm

TEST CIRCUIT

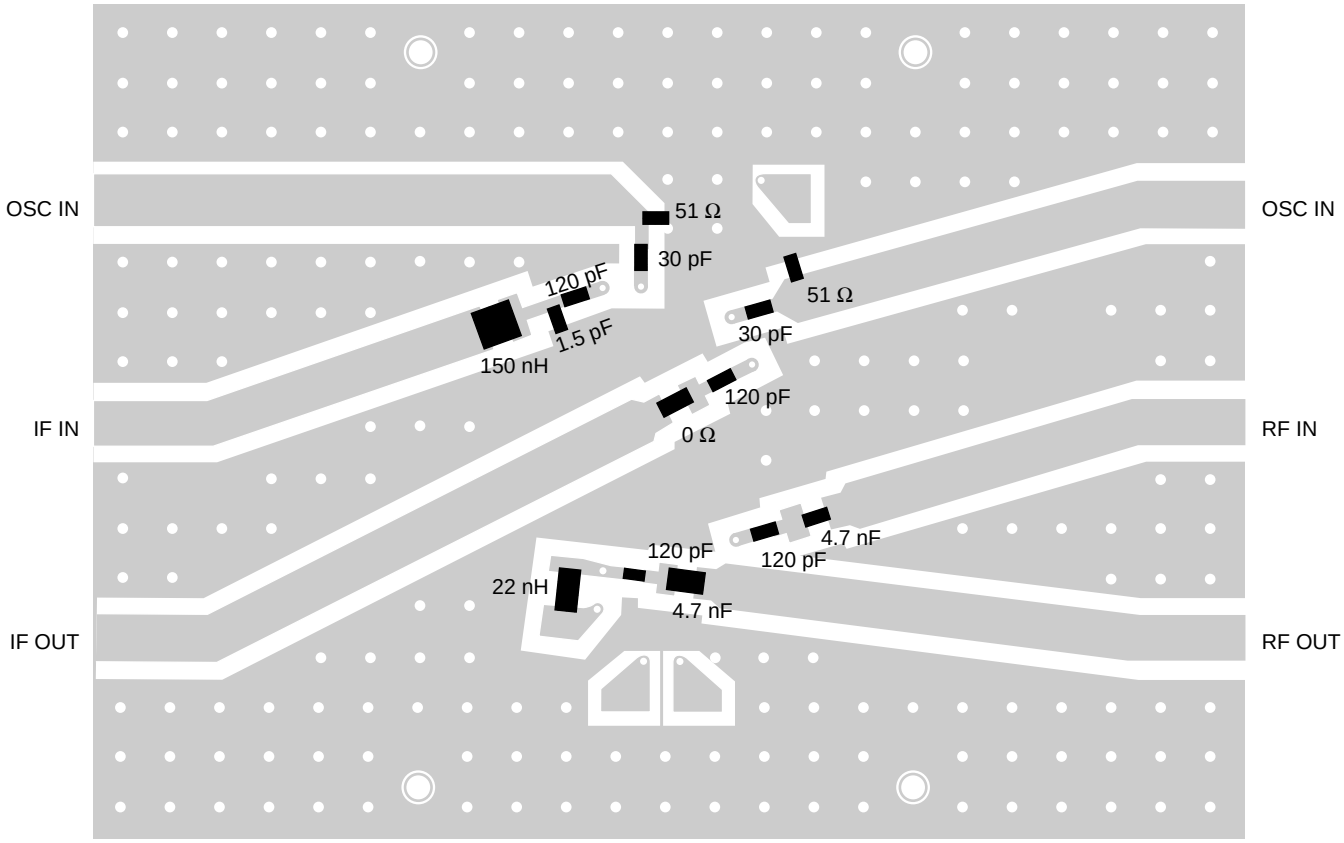


TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD

IC MOUNTED SIDE



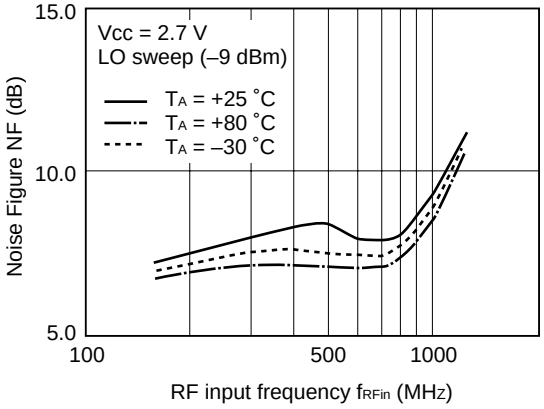
COMPONENT MOUNTED SIDE



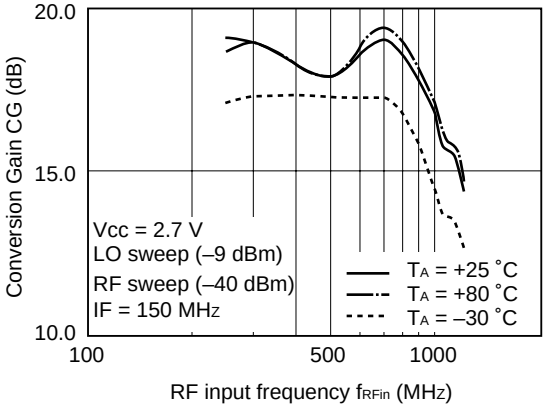
TYPICAL PERFORMANCE (Unless otherwise specified V_{CC} = 2.7 V Vps ≥ 1.8 V)

– Downconverter block –

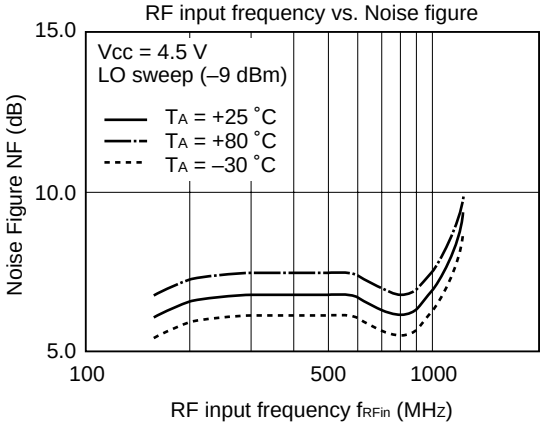
RF input frequency vs. Noise figure



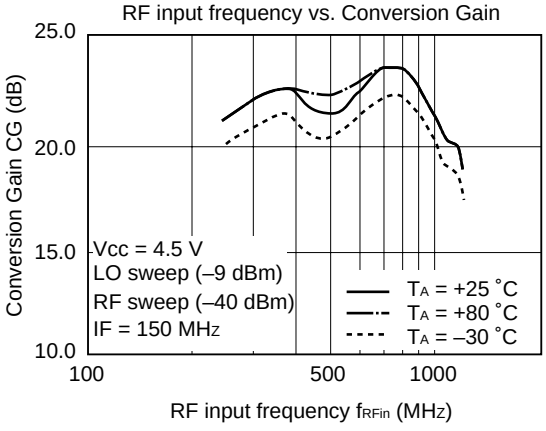
RF input frequency vs. Conversion Gain



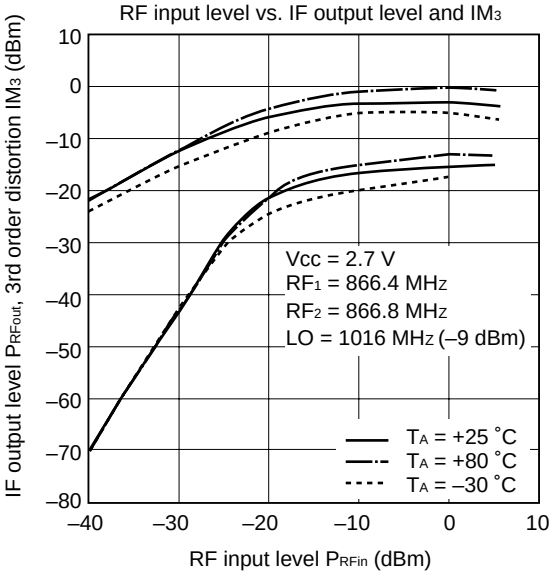
RF input frequency vs. Noise figure



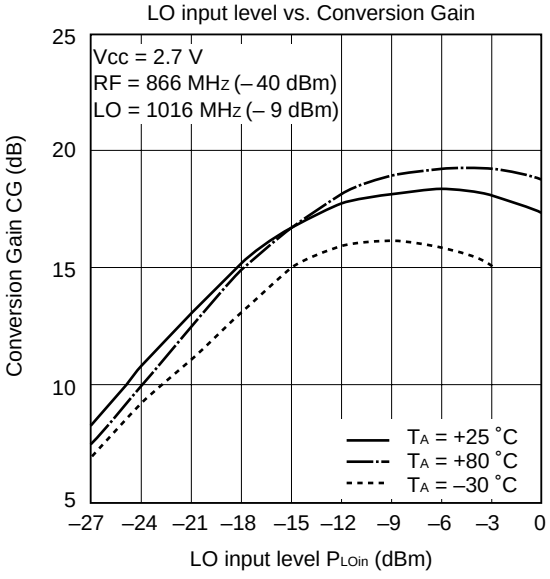
RF input frequency vs. Conversion Gain



RF input level vs. IF output level and IM3

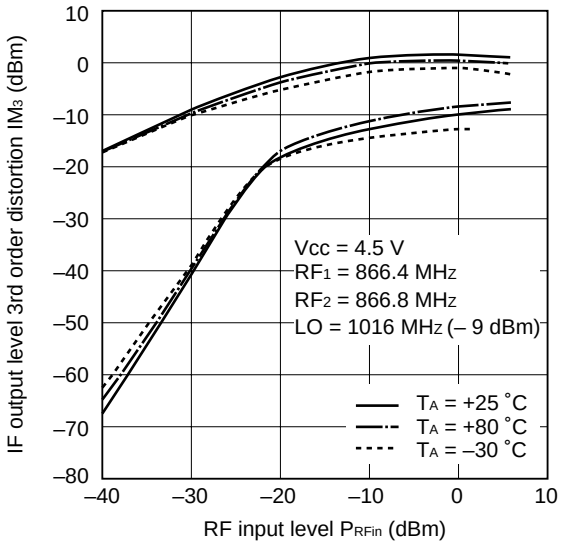


LO input level vs. Conversion Gain

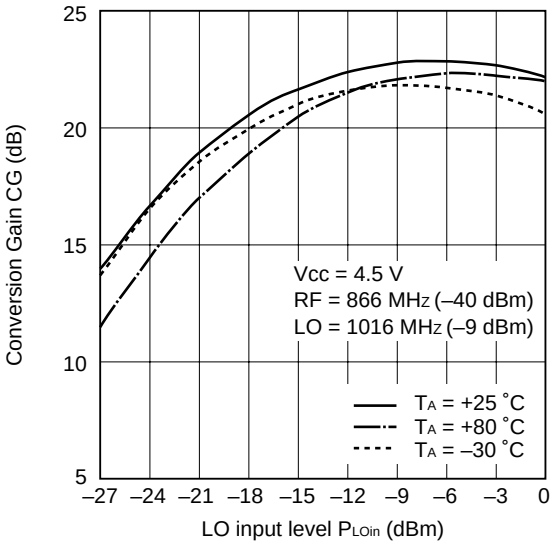


– Downconverter block –

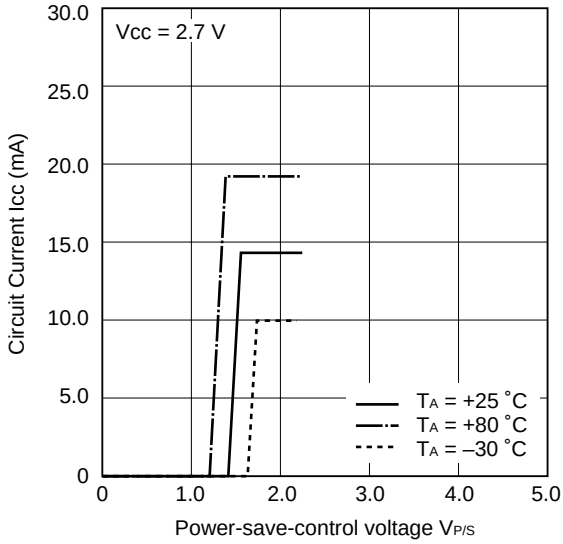
RF input level vs. IF output level and IM_3



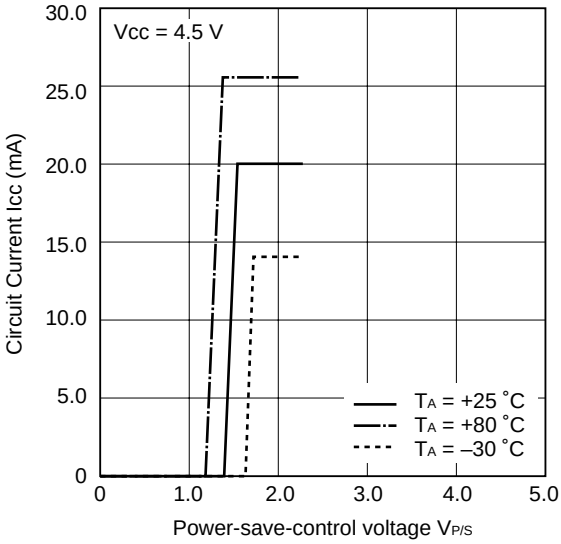
LO input level vs. Conversion Gain



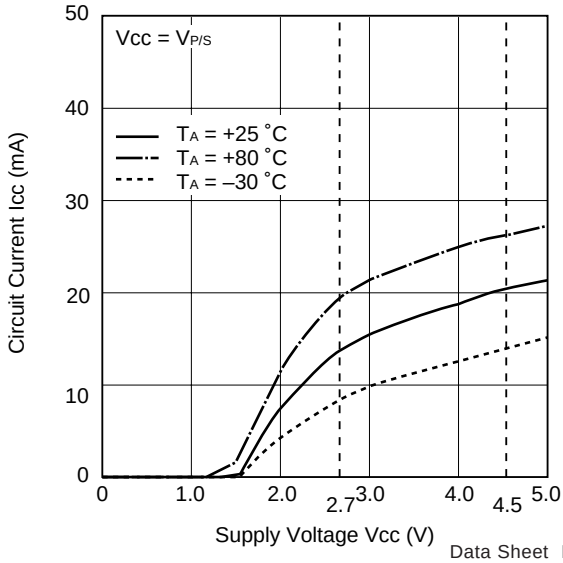
P/S control voltage vs. Circuit Current



P/S control voltage vs. Circuit Current

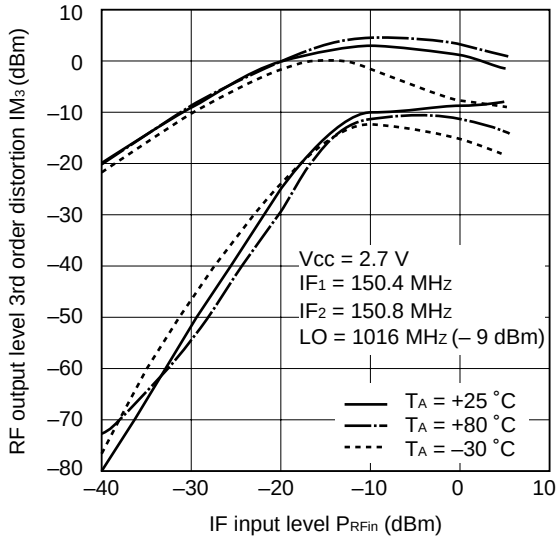


Supply voltage vs. Circuit Current

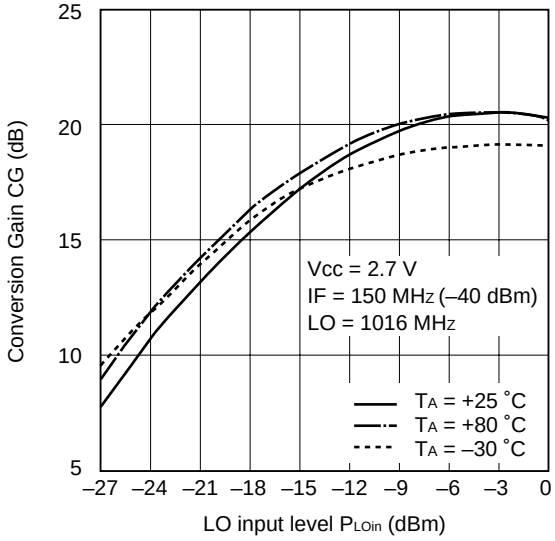


– Upconverter block –

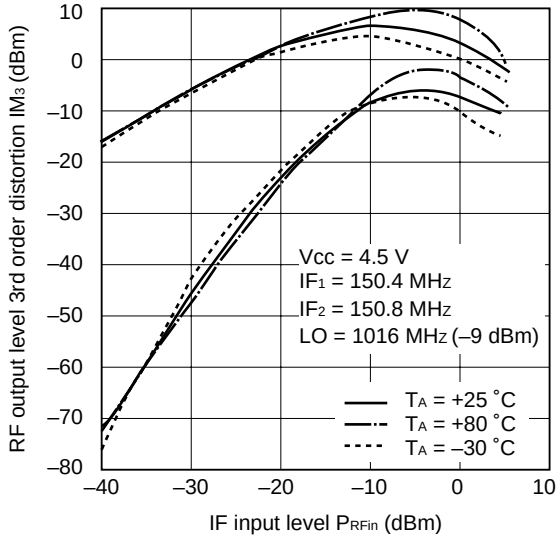
F input level vs. RF outpint level and IM_3



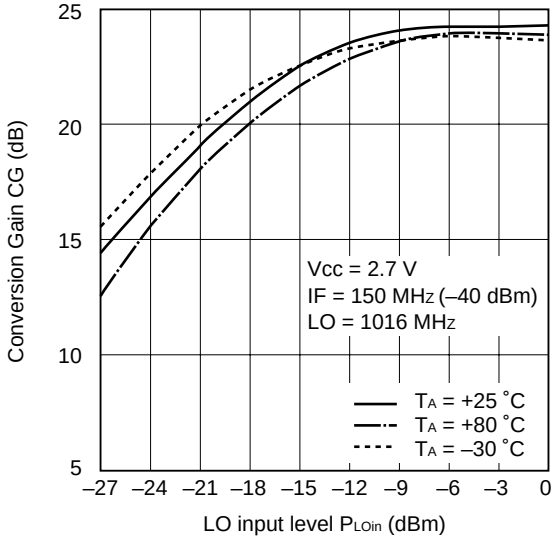
LC input level vs. Conversion Gain



Pin - Pout, IM_3

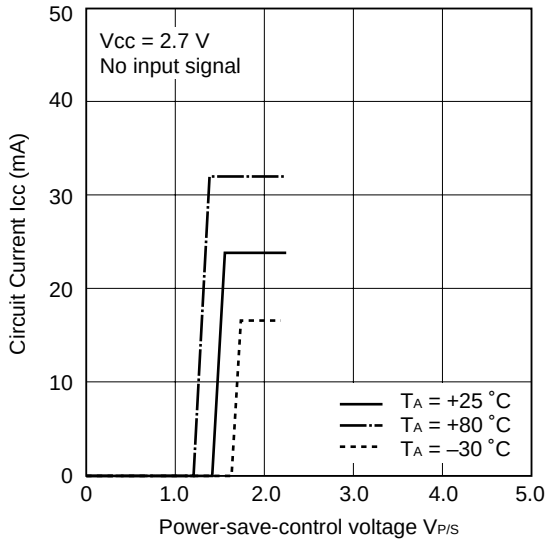


LO input level - CG

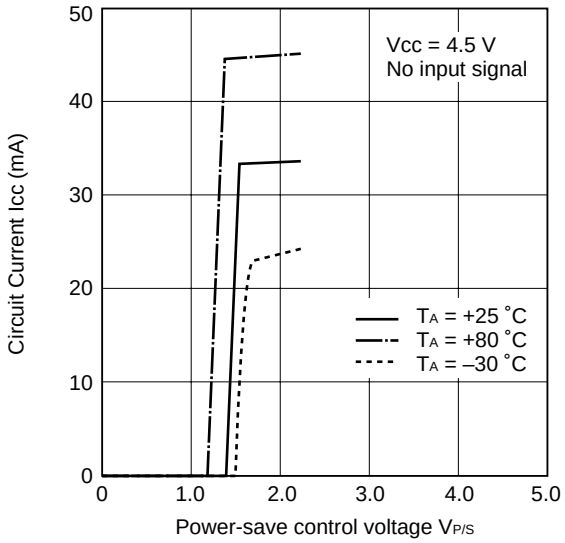


– Downconverter block –

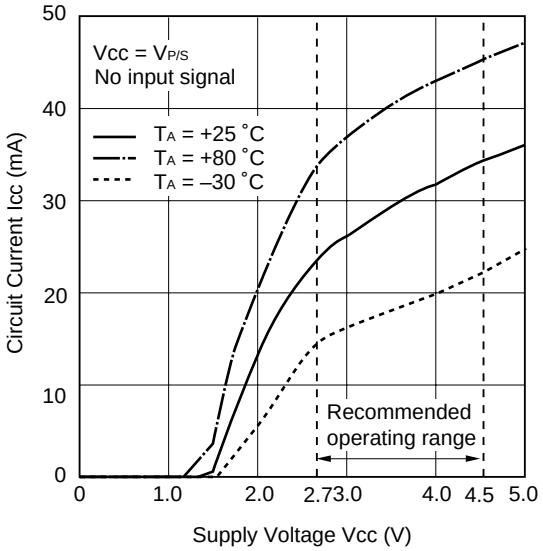
P/S control voltage vs. Circuit Current



P/S control voltage vs. Circuit Current

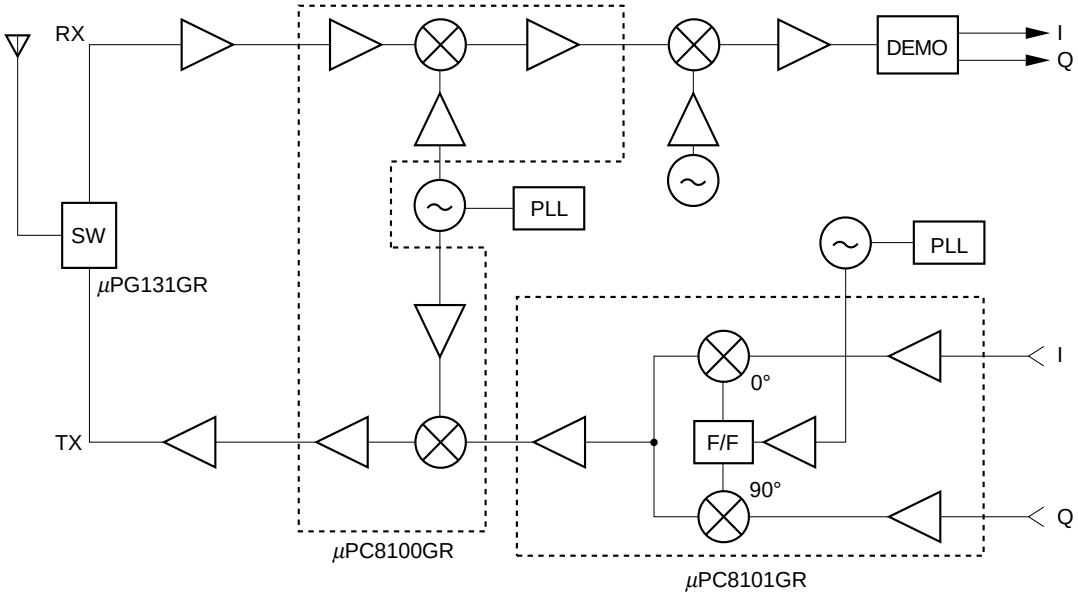


Supply voltage vs. Circuit Current



TYPICAL APPLICATION

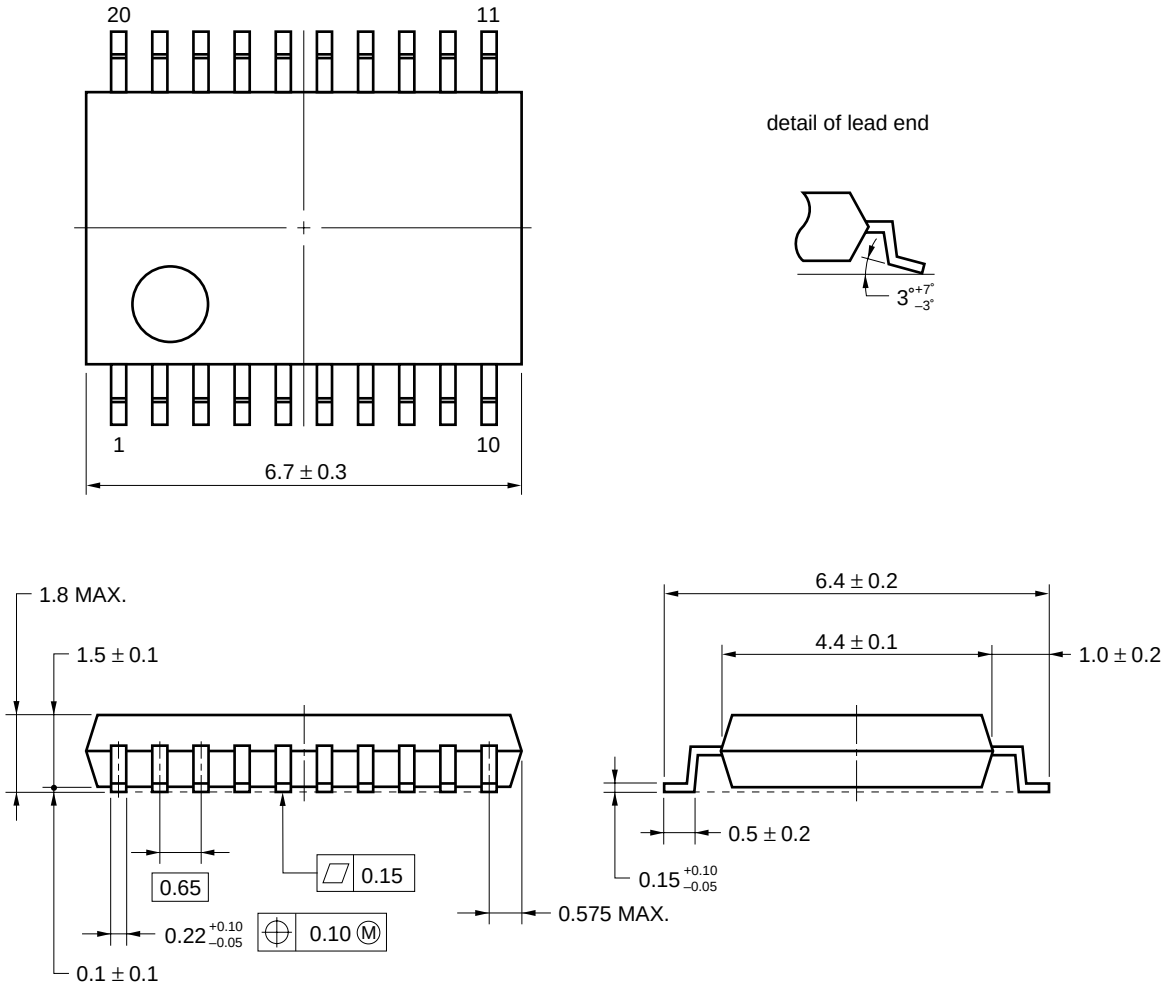
CT2 BLOCK DIAGRAM



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

PACKAGE DIMENSIONS

★ **20 PIN PLASTIC SSOP (225 mil) (UNIT: mm)**



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (e.g. 1 000 pF) to the V_{CC} pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering method and conditions than the recommended conditions are to be consulted with our sales representatives.

μPC8100GR

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 2, Exposure limit*: None	IR35–00-2
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 2, Exposure limit*: None	VP15–00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below Number of flow process: 1, Exposure limit*: None	WS60–00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

***:** Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Apply only a single process at once, except for "Partial heating method".

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
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