

AN6494NSA

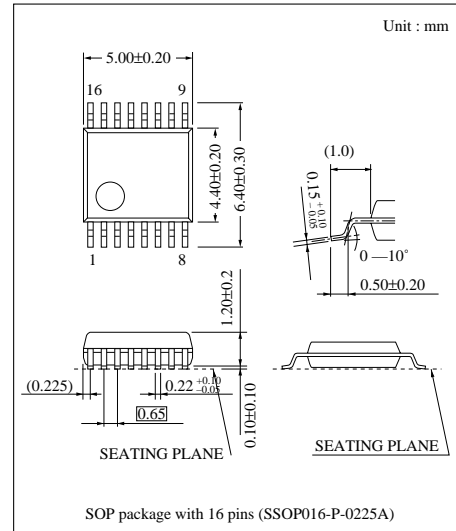
Digital Communication Orthogonal Modulator IC

Overview

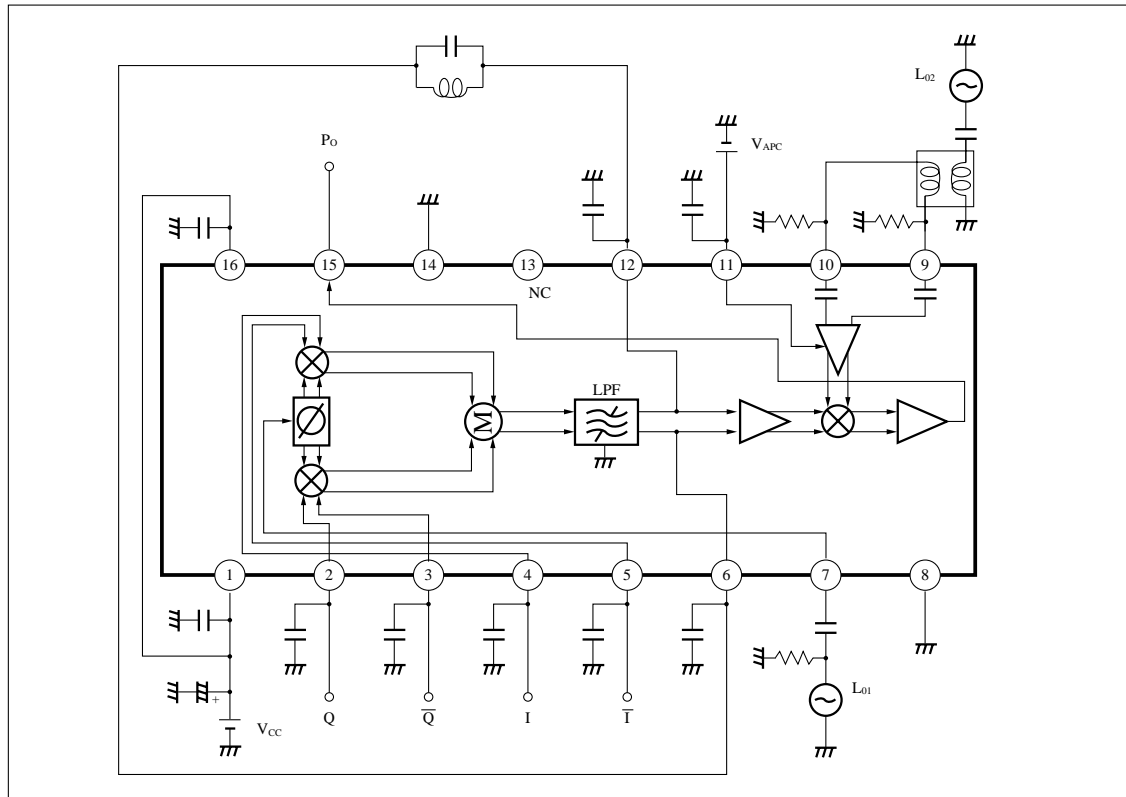
The AN6494NSA is an orthogonal modulator IC for digital cellular telephones. It incorporates a phase shifter and an APC circuit for indirect modulation in the 1.5GHz band. It efficiently prevents power from leaking to adjacent channels. When provided with an LC filter, it can efficiently suppress IF-band local harmonic spurious.

Features

- Operating supply voltage range : 2.7V to 4.0V
- 1.5GHz indirect modulation
- LO1's eighth-order harmonic suppression : -65dBc or better
- Output power level : -13dBm
- Variable range : APC = typ. 38dB (at f_{out}=1.5GHz)
- Phase shifter frequency : 178MHz
- Package : SSOP016-P-0225A with 0.65mm pitch



Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	V _{CC} (mod)	9	LO2R
2	Q input	10	LO2
3	\bar{Q} input	11	APC/BS
4	I input	12	LC2
5	\bar{I} input	13	NC
6	LC1	14	GND
7	LO1	15	RFoutput
8	GND	16	V _{CC} (UP-MIX)

■ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	4.2	V
Supply current	I _{CC}	60	mA
Power dissipation	P _D	252 (Ta=80°C)	mW
Operating ambient temperature	T _{opr}	-30 to + 80	°C
Storage temperature	T _{stg}	-55 to + 125	°C

■ Recommended Operating Range

Parameter	Symbol	Range
Operating supply voltage range	V _{CC}	2.7V to 4.0V

■ Electrical Characteristics (Ta=25±2°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Output level (1)	P _{O1}	L _{O1} =178MHz, -20dBm L _{O2} =1607MHz, -25dBm V _{APC} =2.5V	-16	-13	-10	dBm
Output level (2)	P _{O2}	L _{O1} =178MHz, -20dBm L _{O2} =1631MHz, -25dBm V _{APC} =2.5V	-16	-13	-10	dBm
Current consumption	I _{CC}	L _{O1} =178MHz, -20dBm L _{O2} =1619MHz, -25dBm V _{APC} =2.5V	—	38	48	mA
Sleep current	I _{SL}	L _{O1} =178MHz, -20dBm L _{O2} =1619MHz, -25dBm V _{APC} =0V	—	0	10	μA
Minimum output level	P _{min}	L _{O1} =178MHz, -20dBm L _{O2} =1619MHz, -25dBm V _{APC} =1.0V	—	-52	-45	dBm

Note) V_{CC}=3.7V

IQ signal : 0.5V_{p-p} (single phase), π/4 QPSK modulated

P_{O1} output frequency : 1428.0025MHz

P_{O2} output frequency : 1453.0025MHz

P_{min} output frequency : 1441.0025MHz

■ Electrical Characteristics (Design Values for Reference) (Ta=25±2°C)

The following are design values for reference only (not guaranteed).

Parameter	Symbol	Condition	min	typ	max	Unit
Carrier leak suppression (fLO2–fLO1) *1	CL	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=2.5V, IQ: V _{DC} offset adjust	—	–35	–30	dBc
Image leak suppression *1	IL	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=2.5V, IQ: V _{AC} level adjust	—	–40	–35	dBc
Adjacent spurious suppression *1	DU	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=2.5V	—	–70	–65	dBc
Base-band distortion suppression *1	BD	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=2.5V	—	–40	—	dBc
3rd intermodulation distortion suppression *2 (P _o = –10dBm)	IM3	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=2.5V	—	–35	—	dBc
Adjacent channel power leak suppression (50kHz separation) *3	BL1	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=2.5V	—	—	–60	dBc
Adjacent channel power leak suppression (100 kHz separation) *3	BL2	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=2.5V	—	—	–65	dBc
APC variation range *1	L _{APC}	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=1.0 –2.5V	30	38	—	dB
APC output level control sensitivity *1	S _{APC}	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=1.0 –2.5V	—	47	—	dB/V
In-band output level deviation *1	ΔP	L _{O1} =178MHz, –20dBm L _{O2} =1607MHz–1631MHz, –25dBm VAPC=2.5V	–1.5	—	+1.5	dB
Direct conversion modulation current consumption *1	I _{MD}	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=2.5V	—	17	22	mA
Up-mixer current consumption *	I _{UM}	L _{O1} =178MHz, –20dBm L _{O2} =1619MHz, –25dBm VAPC=2.5V	—	21	26	mA

Note) V_{CC}= 3.7V

IQ_{signal} : 0.5V_{P-P} (single phase), 1.85V_{DC}

*1 : π/4 QPSK modulation

*2 : 3π/4 QPSK modulation

*3 : PN9-stage modulation

APC output level sensitivity was measured with V_{APC}=1.0V and V_{APC}=1.6V.

■ Usage Note

Surge breakdown levels

The following are design values for reference only (not guaranteed).

Condition : C=200pF, and R=0Ω

Pin No.	Positive breakdown level (V)	Negative breakdown level (V)
2	90	60
3	90	50
4	70	60
5	80	70
11	80	70
12	170	—

Pin Descriptions

Pin No.	Symbol	I/O	Description	Equivalent circuit				
1	V_{CC}	I	This is the supply voltage pin for the direct conversion modulator. The IC incorporates a band-gap regulator to provide a regulated bias independent of V_{CC} or temperature change.					
2	I	I	I signal input. The relationship between input DC bias and amplitude is as follows : <table border="1" style="margin: 5px auto;"> <thead> <tr> <th>DC bias (V)</th> <th>Amplitude V_{P-P}</th> </tr> </thead> <tbody> <tr> <td>$1.7 - (V_{CC} - 0.9)$</td> <td>0.5 (single phase)</td> </tr> </tbody> </table> Input impedance is 100k Ω or more.	DC bias (V)	Amplitude V_{P-P}	$1.7 - (V_{CC} - 0.9)$	0.5 (single phase)	
DC bias (V)	Amplitude V_{P-P}							
$1.7 - (V_{CC} - 0.9)$	0.5 (single phase)							
3	\bar{I}	I	Inverted- \bar{I} signal input. Apply 1.5— $(V_{CC} - 0.9)$ V for single-phase input mode.					
4	Q	I	Q signal input. The relationship between input DC bias and amplitude is as follows : <table border="1" style="margin: 5px auto;"> <thead> <tr> <th>DC bias (V)</th> <th>Amplitude V_{P-P}</th> </tr> </thead> <tbody> <tr> <td>$1.7 - (V_{CC} - 0.9)$</td> <td>0.5 (single phase)</td> </tr> </tbody> </table> Input impedance is 100k Ω or more.	DC bias (V)	Amplitude V_{P-P}	$1.7 - (V_{CC} - 0.9)$	0.5 (single phase)	
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5	\bar{Q}	I	Inverted- \bar{Q} signal input. Apply 1.5— $(V_{CC} - 0.9)$ V for single-phase input mode.					
6	LC1	—	An external LC connected to this pin removes spurious from the transmission band by raising up the Lo1 input frequency band. The output is an emitter follower.					

Pin Descriptions (cont.)

Pin No.	Symbol	I/O	Description	Equivalent circuit						
7	Lo1	I	This is the local input to the orthogonal modulator. The input impedance is 10kΩ.							
8	GND	—	This is the ground for the orthogonal modulator. The ground foil pattern for this pin must be wide enough to provide a low impedance.							
9	Lo2 REF	I	This is a local input to the UP mixer. An external balance coil should be used to provide balanced input.							
10	Lo2	I	This is a local input to the UP mixer. An external balance coil should be used to provide balanced input.							
11	APC/BS	I	This is the battery save control for all circuits. It also controls RF output power. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>V_{APC} (V)</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td>0 — 0.5</td> <td>OFF</td> </tr> <tr> <td>1.0 — V_{CC}</td> <td>ON (APC control)</td> </tr> </tbody> </table> <p>The input impedance is 5kΩ or more.</p>	V_{APC} (V)	Status	0 — 0.5	OFF	1.0 — V_{CC}	ON (APC control)	
V_{APC} (V)	Status									
0 — 0.5	OFF									
1.0 — V_{CC}	ON (APC control)									
12	LC2	—	An external LC connected to this pin removes spurious from the transmission band by raising up the Lo1 input frequency band. The output is an emitter follower.							

Pin Descriptions (cont.)

Pin No.	Symbol	I/O	Description	Equivalent circuit
13	NC	—	—	—
14	GND	—	This is the ground for the UP mixer and the output amplifier. The ground foil pattern for this pin must be wide enough to provide a low impedance for high frequencies.	—
15	RF output	O	This is the RF output from the output amplifier circuit (emitter follower).	
16	V _{CC}	I	This is the power supply for the UP mixer and the output amplifier circuit. It incorporates a regulating circuit to provide a regulated bias independent of V _{CC} or temperature change.	—

Characteristics Curve

